Novel 200 V MOSFET Technology Pushes Motor Drive Inverter Efficiency to an Unprecedented Level

Mark Thomas[1], Ralf Siemieniec[1], Elvir Kahrimanovic[1], Laszlo Juhasz[1], Michael Hutzler[1], Kapil Kelkar[2]

[1] Infineon Technologies Austria AG, Austria
[2] Infineon Technologies Americas Corp., USA

Corresponding author: Mark Thomas, mark.thomas@infineon.com
Speaker: Mark Thomas, mark.thomas@infineon.com

Abstract

This work introduces the latest 200 V trench MOSFET technology released to the market. Based on the advantages of 3D charge compensation, the new cell design combines the benefits of low conduction and switching losses with good ruggedness, excellent body diode properties and an extremely tight threshold voltage spread. These features result in a well-balanced all-round performer that will bring significant improvements to a broad range of target applications. They also make the devices an ideal fit especially for high power motor-drive applications, which require an easy paralleling of many devices. The presented results focus on the use of the new devices in such applications.

1 Introduction

New power MOSFET devices dedicated to motor-drive applications are required to provide improvements across a wide range of device parameters. Device losses in the application are primarily associated with on-state resistance (conduction losses), although charges are also significant (switching losses) as well as the body diode forward voltage drop (conduction losses during dead time). In addition, it is advantageous if the MOSFET shows a small reverse-recovery charge and an improved linearity of the output and Miller capacitances. This reduces unwanted oscillations and excessive voltage overshoots ensuring compliance with EMI limits. Furthermore, a small variation of the threshold voltage between different devices eases the paralleling of devices to serve a wide range of output current needs. A small reverse-recovery charge is also beneficial to

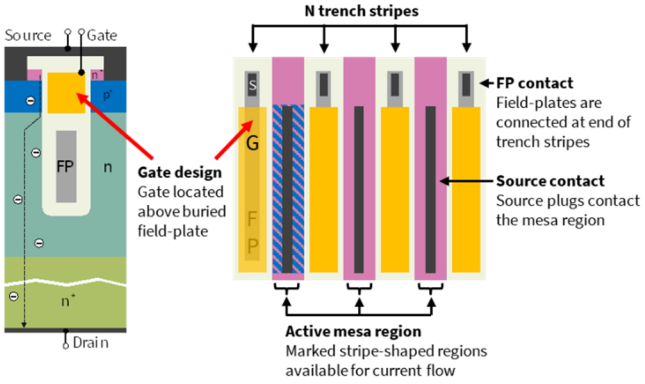

Fig. 1 Typical Trench MOSFET structure with lateral charge-compensation by an insulated field-plate connected to source (left) and commonly employed stripe layout approach in the chip design (right)

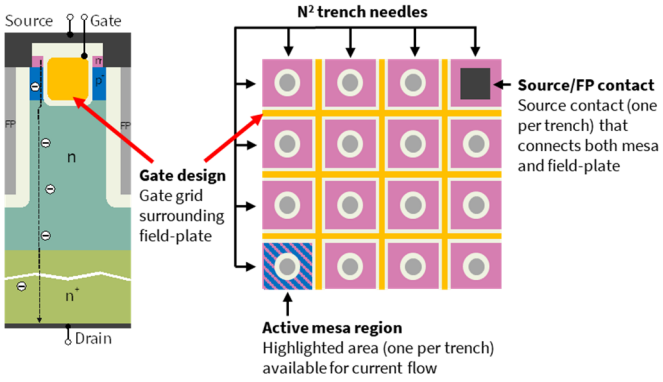

Fig. 2 Trench MOSFET structure with lateral charge-compensation by an insulated field-plate and separated gate trench (left) and the new grid-like layout approach in the improved chip design (right)

ensure a high commutation ruggedness. Finally, the MOSFET also needs to offer sufficient robustness to survive critical operation conditions that may occur occasionally.

2 New device approach

2.1 Advanced cell design

New MOSFET devices are required to provide improvements across all figures of merit. To meet these requirements, a novel cell-design approach has been developed which uses true three-dimensional charge compensation. Today's state-of-the-art MOSFET technologies use an insulated deep field plate underneath and separated from the gate electrode and employ a stripe layout as depicted in Fig. 1 [1]. This new generation separates the field plate trench, which is now formed with a needle-like structure, from a grid-like gate trench that surrounds the needles [2] as shown in Fig. 2. This increases the silicon area available for current conduction allowing for a further reduction in the overall on-resistance [2].

To reduce the two figure-of-merits (FOM) that are essential to achieve good switching properties, $FOM_G = R_{DS(on)} \times Q_G$ and $FOM_{GD} = R_{DS(on)} \times Q_{GD}$, the gate trench underwent a complete redesign to minimize its lateral extension.

The use of a gate grid additionally yields a far more even distribution of the gate resistance across the chip supporting faster switching of the device. This strongly improved homogeneity is also advantageous for device robustness, for example avalanche ruggedness, by reducing the probability that a part of the chip is affected by gate signal delays [3] or parasitic turn-on. In earlier transistor generations, both gate signal delay and parasitic turn-on degrade the device ruggedness as power dissipation is limited to just a part of the chip. In addition, the direct connection of the field-plate in the needle to the source metal supports a high avalanche ruggedness. In a striped layout, the local field-plate potential varies along a trench stripe and consequently may alter the local breakdown voltage [4]. This can lead to an inhomogeneous power dissipation over the chip area degrading device ruggedness.

2.2 Device properties

Fig. 3 summarizes the realized parameter improvements for the new OptiMOS™ 6 200 V technology [5] based on the new grid-like layout with trench needles. All key parameters show a significant improvement over the earlier OptiMOS™ 3 technology [6].

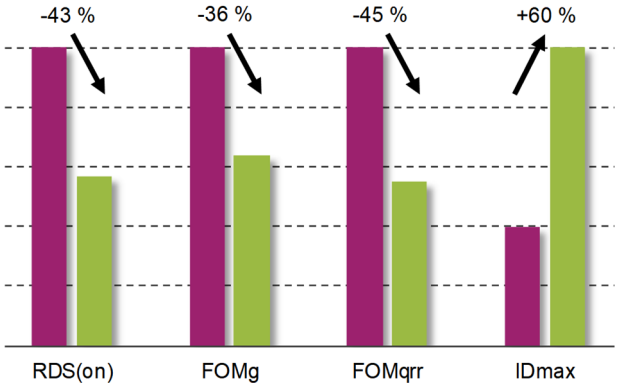

Fig. 3 Improvement in device performance for best-in-class 200 V devices in TO-263 package

As the new 200 V devices mainly target battery power and motor drive applications such as light-electric vehicles (LEVs) and forklifts, it was especially important to further reduce the reverse-recovery charge with respect to the previous generation with a fast diode [6]. This not only enables a further reduction of switching losses, but also improves the EMI behavior and ensures a high commutation ruggedness [7]. Thanks to the new advanced cell design, the on-resistance of the device is considerably reduced allowing the device to increase the drain current capability by a remarkable 60 % in the same package footprint.

3 Single switch in 3-phase motor-drives inverter test platform

3.1 Introduction of the test platform

This platform serves to compare the performance of the new OptiMOS™ 6 technology to its predecessor OptiMOS™ 3 using best-in-class single switches in a standard TO-263 package. This test platform represents a three-phase motor drive inverter and consists of three modules; gate drive board, power board and DC capacitor bank.

The power PCB employs a single layer insulated metal substrate (IMS) board with aluminum core to ensure an excellent thermal performance. The switching frequency of the inverter is 10 kHz with sinusoidal SVM modulation. The platform delivers a single phase current of 33 Arms at a DC bus voltage of 144 V. The dead time between high and low side switches is set to 600 ns. Fig. 4 shows the test platform.

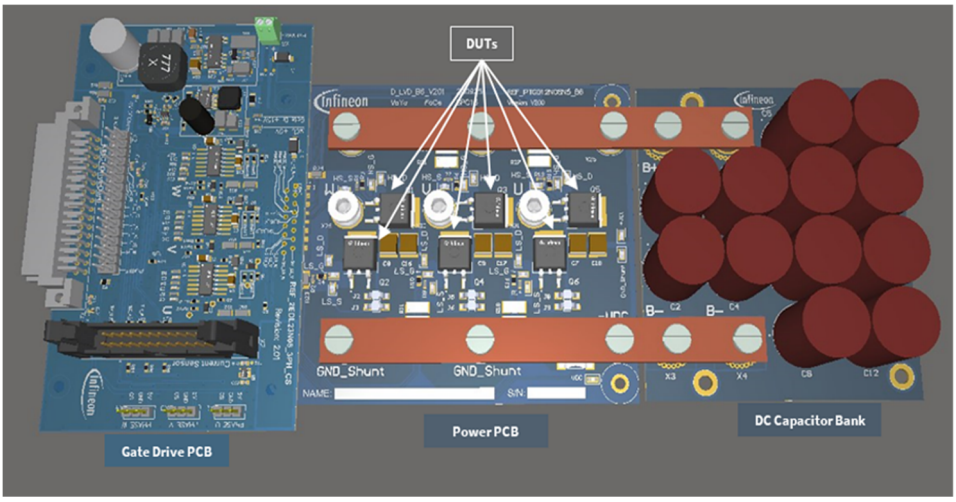

Fig. 4 3 phase motor-drives inverter test platform

3.2 Device performance comparison

Fig. 5 compares the switching behavior of devices from the previous and new generations of technology . The new OptiMOS™ 6 waveforms reveal a cleaner and more linear turn-on and turn-off, translating into lower switching losses. The total power losses are reduced by 45 %, with 39 % less switching losses and 49 % less conduction losses. Consequently the new devices run much cooler with a maximum temperature of 63.6 °C, compared to 95.8 °C in the case of the previous generation as indicated by the thermal images shown in Fig. 6. This enables a significant increase of the output power. For the same device temperature, the current per phase can be increased by an impressive 38 %.

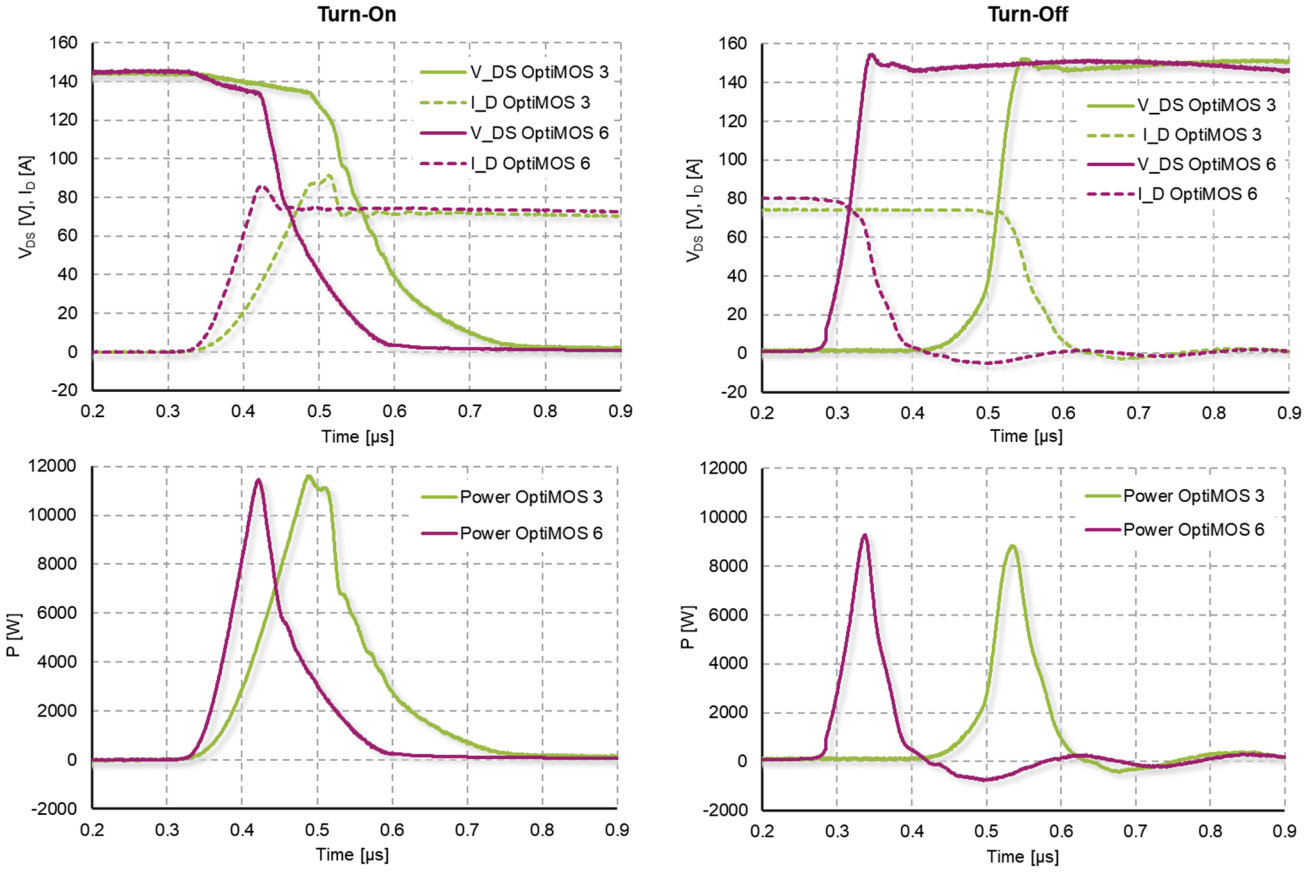

Fig. 5 Comparison of switching waveforms (top) and instantaneous power (bottom) for the new OptiMOS™ 6 and the predecessor OptiMOS™ 3 technology (I_D = 75 A)

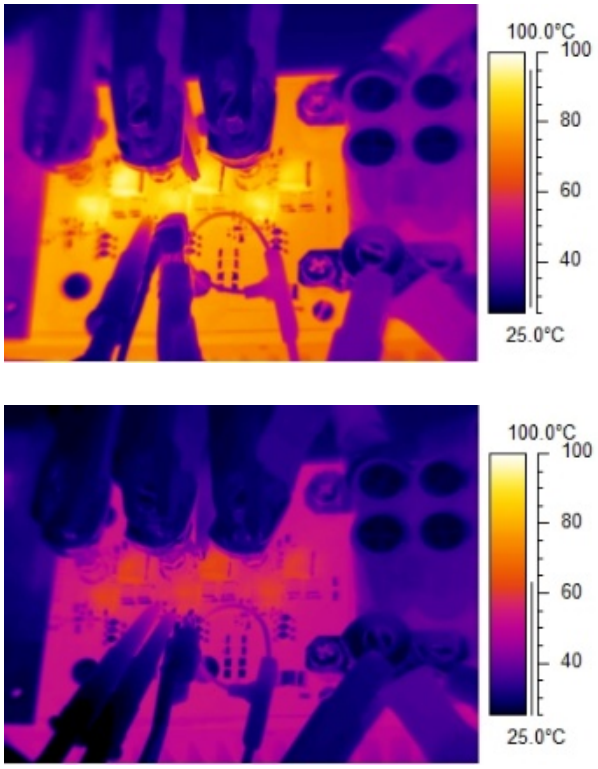

Fig. 6 Comparison of device temperature at identical power output between OptiMOS™ 3 (top) with 95.8°C and the new OptiMOS™ 6 (bottom) with 63.6°C

4 Device paralleling in a modified commercial 3-phase inverter

4.1 Introduction of the test platform

This application compares the performance of the latest 200 V technology with that of its predecessor under hard switching conditions in a motor drives application. The modified commercially available inverter employs a common B6 topology as depicted in Fig. 7, with a nominal input voltage of 144 V, an average current output of 135 Arms and a 1-minute phase RMS output current of 500 Arms. The inverter is sized to drive a 65 kW AC induction motor. In total the power board contains 96 MOSFETs, with 16 devices paralleled in each leg. The use of an insulated metal substrate power base provides superior heat transfer for increased reliability and performance. All tests are performed at a switching frequency of 10 kHz, with a dead time of approximately 1 µs. Fig. 8 illustrates the general functional block diagram of the test environment.

The inverter uses devices in standard TO-263-3 packages, making it relatively easy to swap between different generations. The investigation presented in this work focusses on the comparison of the new OptiMOS™ 6 200 V devices with the preceeding technology. The comparison uses best-in-class devices, where the new OptiMOS™ 6 devices have an on-resistance of 6.8 mΩ whist the previous OptiMOS™ 3 devices have an on-resistance of 11.7 mΩ.

In the presented measurements, the motor was running in a load condition with a phase current of 160 Arms. To enable the loss calculations, the measured values, among others, include low-side MOSFET current, high- and low-side drain-to-source and gate-to-source voltages and the phase current. All measurements extended over one complete electrical period of the motor.

4.2 Test results in the motor drives inverter

The first investigation determined the mean losses per MOSFET. The results are shown in Fig. 9. The comparison includes the overall mean losses per MOSFET as well as the separate conduction, turn-on and turn-off losses. The overall loss reduction accounts for a remarkable 36%. It is also worth mentioning that the new OptiMOS™ 6 200 V devices achieve a reduction in all of the loss contributors.

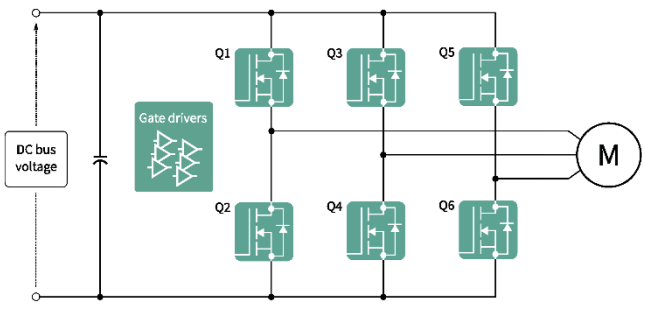

Fig. 7 Basic schematic of the B6 inverter

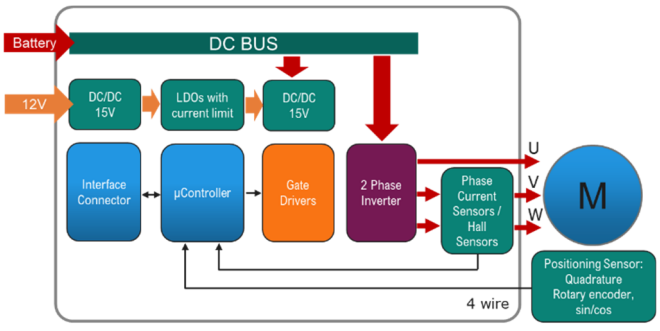

Fig. 8 General functional block diagram

Beside a reduction of the losses, it is important that the devices provide a clean switching behavior. Switching waveforms are measured for a single MOSFET. Fig. 10 gives an overview of the investigated device parameters, and at which positions in the circuit these values are measured. All gate-to-source and drain-to-source voltages are calculated from two separate measurements, taken from the respective electrode to ground. The current through the MOSFET is measured by a Rogowski coil at the source of the low-side device.

Fig. 11 shows the switching waveforms of the new generation of devices when the high-side switch is turned-on. Fig. 12 depicts the transients for the turn-off of the high-side switch, with the low-side MOSFET operating in synchronous rectification mode. In both cases, the use of the OptiMOS™ 6 devices result in clean waveforms. There is no visible ringing, and the slew rates are rather linear which is advantageous for the EMI behavior.

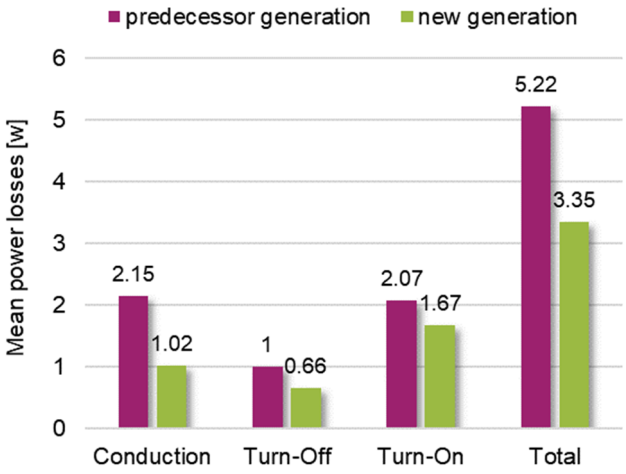

Fig. 9 Comparison of mean power losses per MOSFET

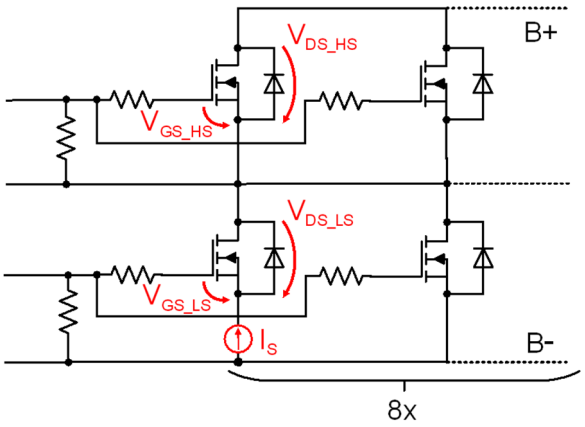

Fig. 10 Indication of test points for the waveform measurements

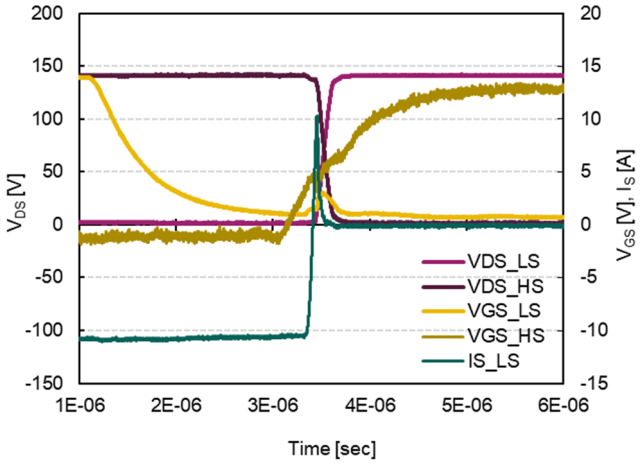

Fig. 11 New device switching waveforms at turn-on of the high-side switch

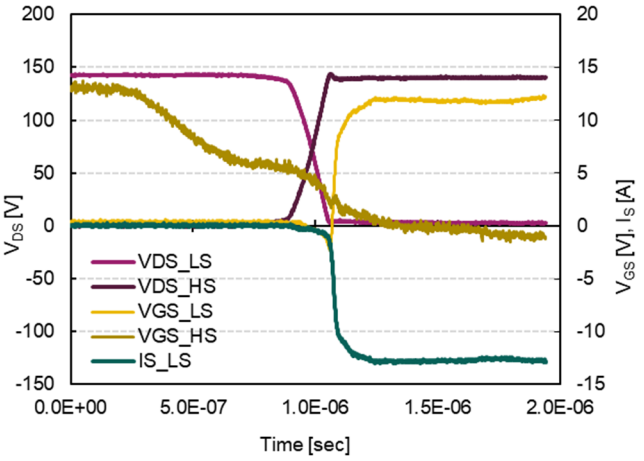

Fig. 12 New device switching waveforms at turn-off of the high-side switch

This implies that the significantly improved device performance does not degrade the EMI behavior. Indeed, this is confirmed by a comparison of the radiated emission of the two technology generations as shown in Fig. 13 and Fig. 14. The radiated emission measurements were done in accordance with the applicable standard EN 12895.

5 Conclusion

This work introduces our latest 200V power MOSFET technology that delivers improvements in all important device parameters and combines the benefits of low on-state resistance with a superior switching performance.

The remarkable progress in the overall device performance is enabled by substantial improvements at the device technology level. This has culminated in a unique device structure, which is the first to employ three-dimensional charge

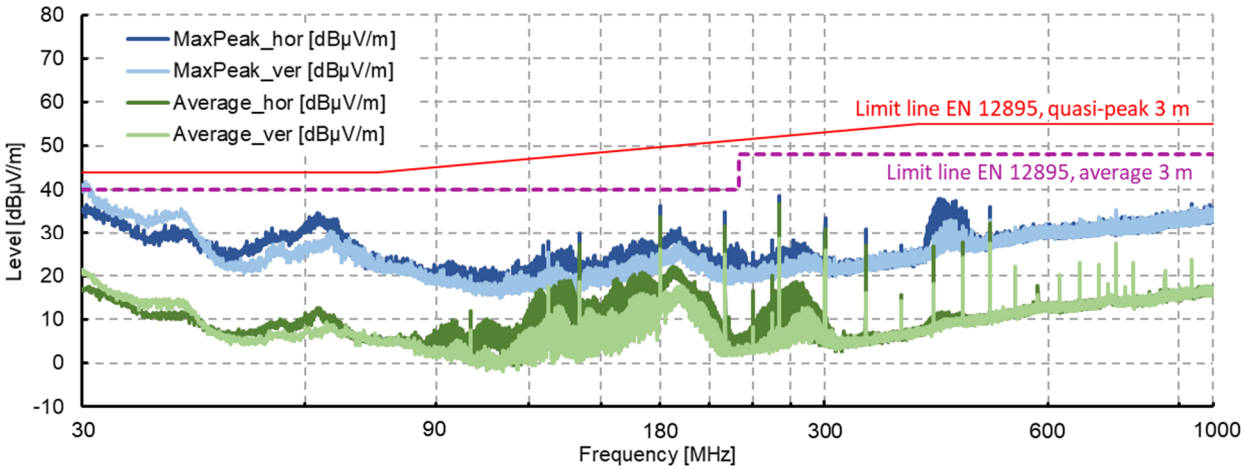

Fig. 13 Measurement of radiated emission in the application using the predecessor device generation

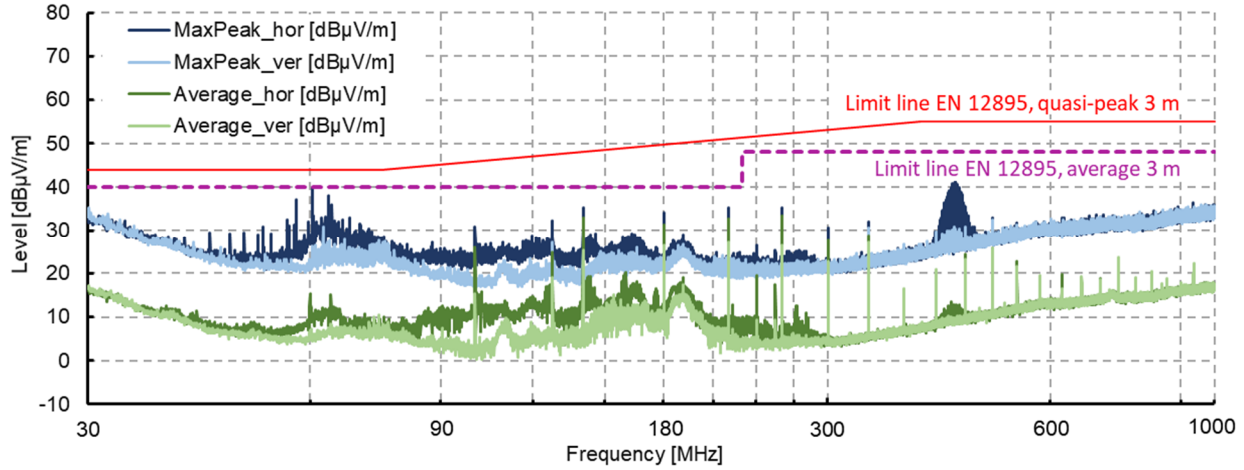

Fig. 14 Measurement of radiated emission in the application using the new device generation

compensation combined with a gate grid. The new design provides a so-far unmatched homogeneity of the gate and field plate resistance across the chip. The reduction achieved in the on-resistance, together with a low output charge and the improved switching homogeneity across the device area, enhance the system efficiency in the tested applications across all load conditions. The new device structure is also beneficial for the internal body diode of the MOSFET. Because the silicon area conducting current is increased, the body diode current density is decreased, which for the same current level means a decreased reverse recovery charge.

Motor drive applications benefit immensely from the new technology, as both conduction and switching losses reduce. The devices can easily be massively paralleled achieving clean switching waveforms. The good switching properties are also confirmed by radiated emission measurements which stay well within the required limits.

The significantly improved device performance even allows a reduction of up to half the number of paralleled devices required (depending on the application), or alternatively the use of smaller footprints, without having a negative impact on the temperature of the devices. This not only provides an advantage in terms of bill-of-materials (BOM) costs, but also the opportunity to reduce the area on the PCB.

This opens the door for a further optimization at the system design level, which is expected to further boost efficiency, reduce the converter or inverter size and increase the power density.

6 Acknowledgements

We thank Jannik Gade, Volodymyr Yakobniuk and Nikola Ivic for the measurement support on the motor drives inverter.

We also want to thank Adrian Finney for carefully editing this article.

7 References

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