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400V SiC MOSFET empowering three-level topologies for highly efficient applications from motor-drives to AI

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ABSTRACT

The introduction of 400 V SiC MOSFET technology bridges the voltage range gap between 200 V medium-voltage MOSFETs and 600 V super-junction MOSFETs. This technology is characterized by low switching losses and low on-state resistance, making it suitable for 2-level topologies in 120 VAC or 300 VDC systems or 3-level topologies with typical input voltages ranging from 180 VAC to 350 VAC or 400 VDC to 600 VDC.

The technology concept is presented, and its efficiency and power density gains are demonstrated through measurements on test boards representing a 3-level ANPC general purpose inverter and a 3-level FC PFC for highly-efficient power supplies.

Introduction

A new SiC Trench MOSFET technology is introduced, featuring a 400 V nominal blocking voltage. The new technology closes the long-standing gap in performance between medium-voltage 200 V MOSFETs and high-voltage 600 V Superjunction (SJ) MOSFET technologies. Scaling up 200 V MOSFETs or scaling down 600 V SJ MOSFET technologies resulted in compromised performance, including larger input-, output-, and reverse-recovery charges, and additionally often in a significant drop in output- and Miller-capacitance with increasing drain voltage, making them highly non-linear. This limits their use in hard-switching applications employing half- or full-bridge topologies.

The new 400 V SiC MOSFET devices offers improved performance and efficiency, featuring small gate-, output-, and reverse-recovery charges, as well as a highly linear output and Miller capacitance over drain voltage. With a low on-resistance, these devices promise to improve system efficiency and power density in their target application fields.

Device technology

General considerations

Wide band-gap semiconductors based on silicon-carbide have gained significant attention in the power device industry, and it is essential to understand the differences between silicon-carbide and traditional silicon-based devices.

One of the key differences is the higher surface density of atoms per unit area in silicon-carbide compared to silicon, resulting in a higher density of dangling bonds and carbon clusters at the interface (Chbili et al., 2016). These defects can affect device reliability. Additionally, silicon-carbide devices require a limitation of the electric field in the gate oxide to maintain reliability (Lutz et al., 2018), and they exhibit a higher Fowler-Nordheim current injection due to a smaller barrier height (Singh & Hefner, 2004; Matocha, 2008).

A significant challenge in silicon-carbide MOSFETs is the low electron mobility at the SiO_2-SiC interface, caused by carbon-related interface defects. These defects lead to electron scattering and trapping, reducing the channel mobility (Schaffer et al., 1994). The 4° off-axis tilt of commercially available silicon-carbide substrates, necessary for epitaxial layer growth, introduces surface roughness and steps when fabricating a MOS structure. Fig. 1 illustrates this situation schematically. This feature affects both lateral and trench MOSFET technologies, impacting channel properties and device performance.

Studies have shown that the vertical channel mobility strongly depends on the crystal plane, with a significant difference between worst and best channel mobility as indicated in Fig. 2 (Yano et al., 2007). A suitable post-oxidation annealing step, such as nitric oxide annealing, can significantly reduce the interface state density (Kimoto et al., 2005). By optimizing the post-oxidation anneal conditions, it is possible to

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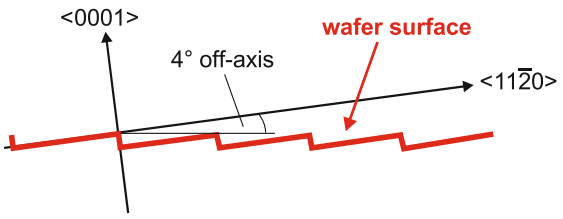

Fig. 1. Schematic illustration of the 4° off-axis cut of 4H-SiC wafers.

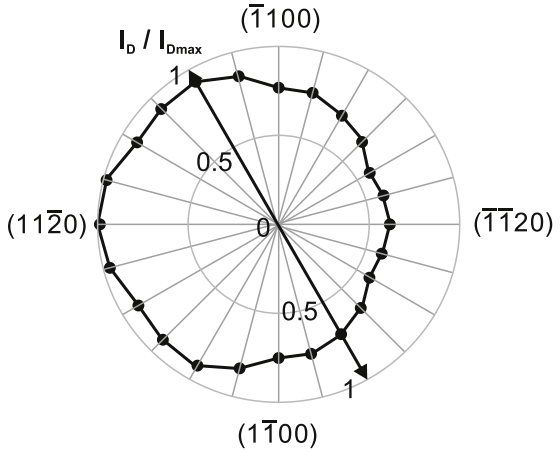

Fig. 2. Relative channel mobility for various trench planes of 4H-SiC on-axis substrate (Yano et al., 2007).

achieve high channel mobility and high threshold voltage stability simultaneously.

To address the limitation of the electric field strength in the blocking state, device design measures such as buried shielding regions can be employed. By understanding and addressing these challenges, it is possible to develop more efficient and reliable power devices.

400V trench MOSFET structure

The MOSFET design builds upon our previously introduced approach (Peters et al., 2017; Siemieniec et al., 2017). As shown in Fig. 3, the general cell concept features an active channel aligned along the a-plane, which provides optimal channel mobility and minimal interface

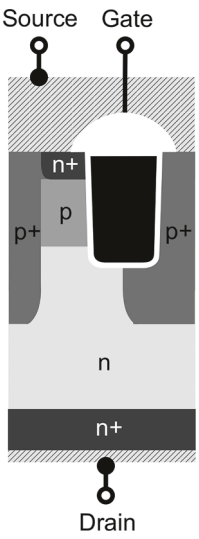

Fig. 3. SiC Trench MOSFET concept with an asymmetric channel.

trap density. The gate oxide is protected by deep p-wells connected to the source electrode at the semiconductor surface. By utilizing the inactive sidewall, the buried p-region is connected to the source electrode, resulting in a compact cell design. This design, combined with the high channel mobility of the a-plane, achieves a low area-specific on-resistance.

Compared to previous designs (Siemieniec et al., 2017; Siemieniec et al., 2019), the new MOSFET generation benefits from ongoing technology advancements. These improvements enable a reduced cell pitch, enhanced channel properties, and improved control over drift region properties. Furthermore, the chip design is optimized to minimize active area loss, for example through the use of a compact junction termination design. This results in a highly efficient and powerful MOSFET design.

Device properties

Fig. 4 highlights the key device property improvements of the new 400 V device compared to a 650 V device from the same technology generation, both with an identical chip size in a common TO-263–7 (D2PAK 7pin) package. The values shown are averages from a batch of devices, accounting for typical production variations. The comparison reveals lower values for the 400 V technology, indicating its potential benefits. The 400 V device's lower on-resistance values are also notable, which can be attributed to the advantages of trench technology over traditional DMOS devices with lateral channels.

The indicated FOMs describe the product of the on-resistance and the respective charge, e.g. FOMg = $R_{DS(on)}$ x Qg etc. The FOMg is related to the total gate charge required to turn-on the transistor and indicates the driving losses. The FOMgd is associated with the gate-drain-charge that governs the drain voltage transient and correlates with the switching losses. The FOMoss is linked to the output charge of the MOSFET, while FOMEoss relates to the energy stored in the output charge.

As all aforementioned switching FOMs are lower for the 400 V devices compared to the 650 V counterparts, the switching losses are reduced. Under datasheet switching conditions with respect to V_{DS}, the switching losses for the 400 V device are 2.5 to 3 times lower than that of the higher voltage rated parts - depending on the load current and the applied external gate resistance. Considering an identical switching speed (equal dv/dt), the difference can rise up to 4 times lower switching losses. These values were obtained by standard double pulse measurements.

The temperature dependence of the on-resistance indicates one of the key advantages of the 400 V technology. As shown in Fig. 5, the on-resistance ($R_{DS(on)}$) of the 400 V device exhibits a relatively flat temperature dependence. The value increases by only 11 % from 25 °C to 100 °C. This characteristic allows for the selection of a MOSFET with higher nominal $R_{DS(on)}$ values (as these are typically specified at room

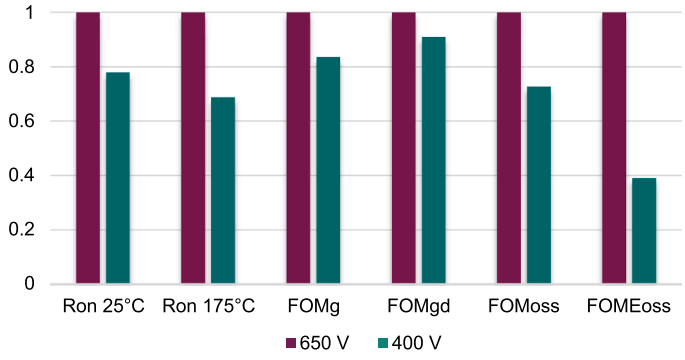

Fig. 4. Realized parameter improvements of the 400 V technology with respect to the 650 V device technology (identical chip size in a TO-263–3 package). FOMs defined at V_{DS} = 200 V / 400 V for the 400 V and 650 V devices, respectively.

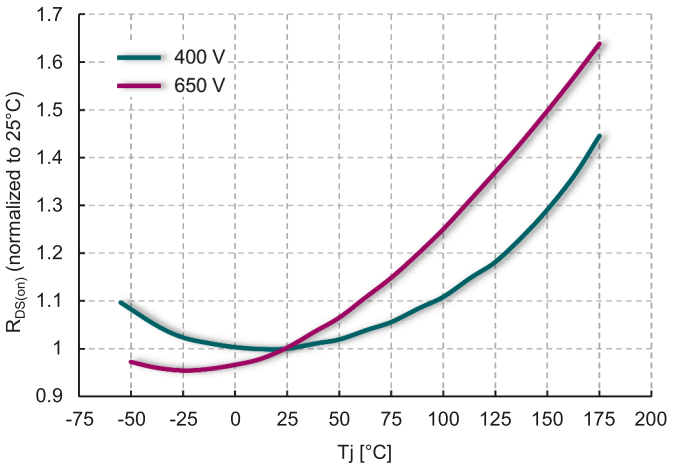

Fig. 5. Temperature dependence comparison of normalized on-resistance.

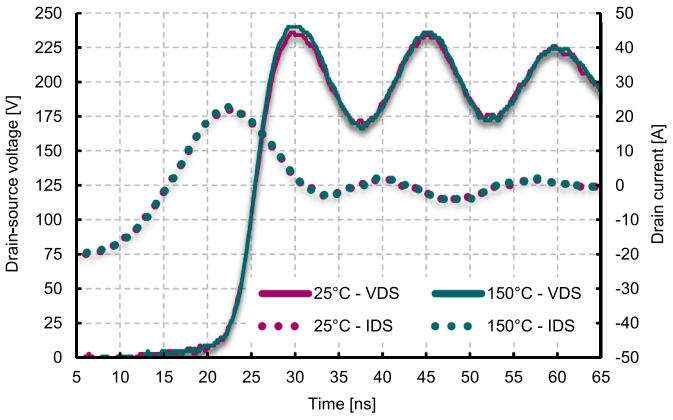

Fig. 6. Double-pulse characterization of 400 V SiC-MOSFET showing the body diode commutation.

temperature), resulting in lower costs and an improved switching performance.

Fig. 6 depicts the waveforms of the body diode commutation at two different temperatures. The measurements indicate an excellent commutation ruggedness with very low reverse recovery charge despite the high applied di/dt slew rate. Such a condition is a typical use case for SMPS applications. The switching waveforms further indicate a negligible dependence on the operation temperature.

Performance in 3L ANPC inverter

Advantages of using a 3L ANPC topology

The new devices are ideal for converting DC link or battery voltages of up to 600 VDC to single-phase (230 V_{RMS}) or three-phase (400 V_{RMS}) AC systems. Traditionally, these applications have used 1200 V semiconductors in a 2-level topology due to the lack of alternative options. However, the three-level active neutral point clamp (3 L ANPC) topology (Brückner & Bernet, 2001), as depicted in Fig. 7, enables the use of 400 V devices.

In this topology, the DC capacitor bank divides the DC link voltage, so each half-bridge sees half of the DC link voltage. This allows for a maximum blocking capability of 800 V, which offers enough safety margin for typical DC link voltages in the 600 V range, and offers bidirectional energy transfer. The higher possible DC link bus voltage contributes to efficiency improvements and increased power density, reduces PCB copper content, and eliminates the need for paralleling devices.

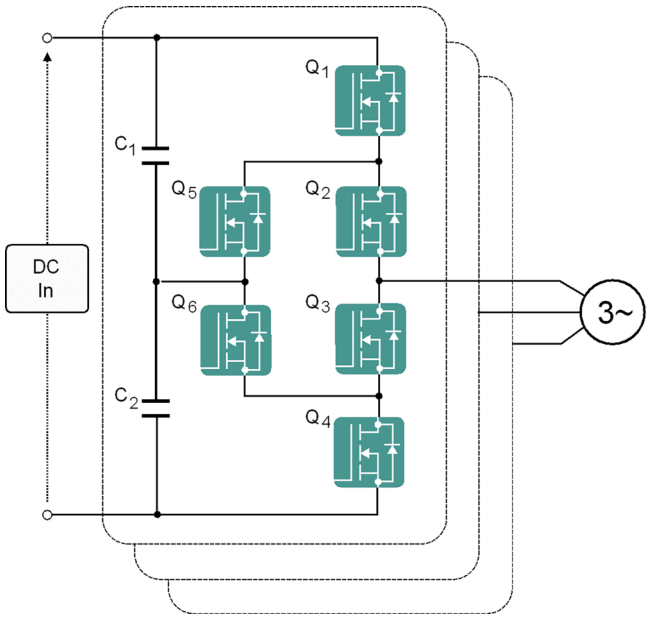

Fig. 7. Simplified basic schematic of the 3-phase 3 L ANPC Inverter.

Additionally, the 3L ANPC topology provides further benefits. With lower voltages applied across devices, switching performance improves, enabling higher overall efficiency and output power. Also, the slower dv/dt and the use of three different voltage levels improves EMI behaviour. This results in more efficient, reliable, and compact systems.

This topology allows for different usages. It can be used to drive three-phase motors from a DC link or battery, or it can also serve as a solar inverter. Here, the DC input is connected with the MPPT (maximum power point tracking) unit that is fed by the solar panels, while the AC output connects to the grid via an output filter inductor. Here the 3L ANPC topology offers an additional advantage, as the voltage at the switching node is just half of that of a 2-level B6 inverter. Thanks to this the core losses of the inductor will be significantly lower, as they correlate with the voltage over the inductor. Fig. 8 compares the core losses for a switching node voltage of 100 V and 200 V for a 47 µH inductor IHLP8787 (Vishay Intertechnology Inc, 2020), measured in a buck converter at 50 % duty cycle in full ZVS condition. A simple single-phase solution is possible, and would represent an attractive, highly-efficient solution for 230 V_{RMS} grids.

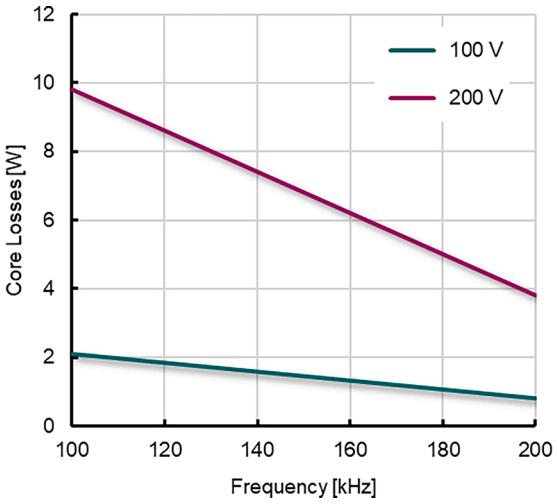

Fig. 8. Comparison of core loss for a typical power inductor in SMPS applications for two switching node voltages.

In motor-drive inverters, the dv/dt limit is typically restricted to 5 V/ns per switch, while 10 V/ns and above is applicable for solar inverters.

Introduction of the developed demonstrator board

The device performance is studied in a medium-power 3-phase 3 L ANPC inverter as depicted in Fig. 9. The inverter is equipped with 18 × 11 mΩ 400 V SiC MOSFET in TOLL packages and can handle peak power levels up to 20 kW. The board employs a 4layer FR4 PCB with 70 µm Copper thickness, the heat sink size is 240 mm x 43 mm.

The gate driver, which provides 18 isolated gate drive voltages, uses a reliable and cost-efficient isolated power supply solution based on a planar transformer. The forward converter requires just one input voltage to generate all 18 isolated output voltages.

To drive the 3 L ANPC topology, one can select between three different modulation schemes as explained in further detail in Song et al. (2024).

For this test board, the so-called 4H2L modulation is selected due to the uniform temperature distribution between the MOSFETs and the lowest layout complexity. In case of 4H2L modulation, Q2 is entirely turned-on during the positive half-cycle. Q1 and Q5 switch al-ternately, with Q1 controlling the duty cycle and phase voltage while Q5 acts as a synchronous rectifier. In the negative half-cycle, Q3 is turned-on completely. Now Q4 and Q6 switch alternately, with Q4 controlling the duty cycle and phase voltage and Q6 acting as a synchronous rectifier. The load will see the difference between the DC input voltage and the neutral point.

Test results

First the inverter was operated in double-pulse operation mode with a dv/dt limit of 10 V/ns per switch, to evaluate the switching behaviour of the new devices. The tests were conducted using an inductive-resistive load (200 µH + resistance of the coil) with the heatsink disconnected. A thermal camera monitored the temperature of the entire board area during the efficiency measurements. As there is no attached heatsink, the applicable power level is limited to about 10 kW.

A Yokogawa WT5000 Precision Power Analyzer was employed to analyse the inverter's performance. The efficiency analysis excluded the gate drivers and controller stage, and sinusoidal pulse width modulation (SinPWM) was used.

The measurements of the voltage and current waveforms during turn-on and turn-off of the high-side switch, using a double-pulse configuration of the 3L ANPC test board, indicate a very smooth switching behaviour. The waveforms are shown in Fig. 10.

For the efficiency measurements, the inverter was operated with a dv/dt of 10 V/ns and sinusoidal pulse width modulation (SinPWM).

Fig. 11 shows the measured efficiency and the maximum case temperature as a function of output power for two different switching frequencies. At a switching frequency of 10 kHz, the inverter delivers an excellent efficiency of 99.51 % for an 8.2 kVA load. Without an attached heatsink, the case temperature reached 114 °C. In the case of a higher switching frequency of 30 kHz, a comparable efficiency of 99.48 % for a 7.2 kVA load was obtained for the same case temperature.

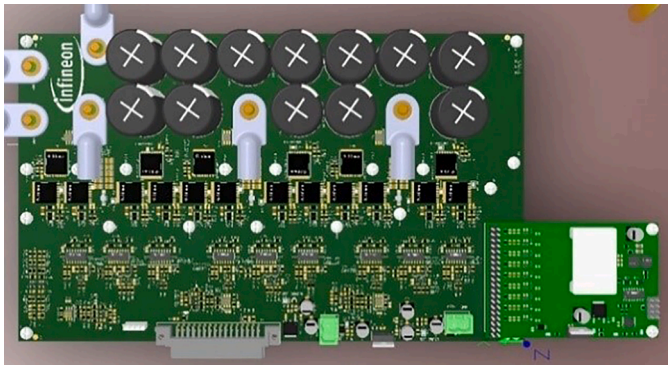

Fig. 9. The 3-phase 3L ANPC test board with attached gate driver.

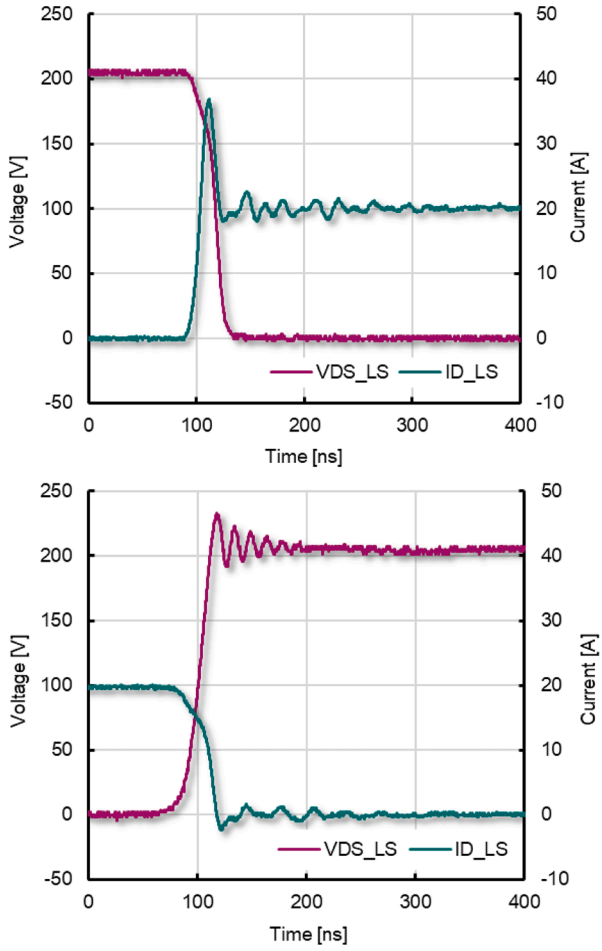

Fig. 10. Turn-on and turn-off waveforms of the high-side switch using a double-pulse configuration of the board [V_{DS} = 200 V, $R_{G(on)}$ = $R_{G(off)}$ = 15 Ω, I_{LOAD} = 20 A, dv/dt = 10 V/ns].

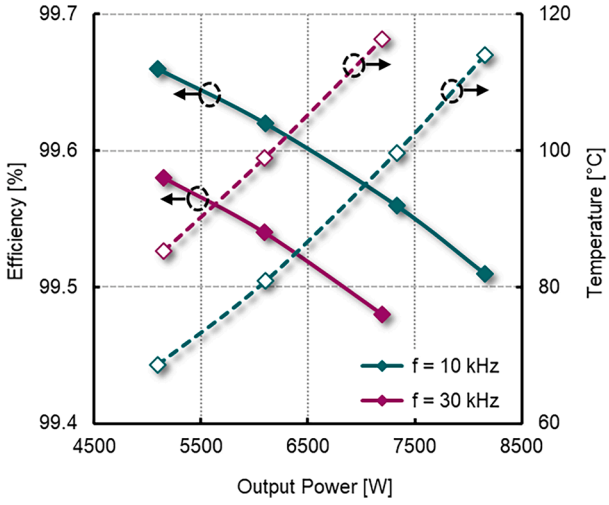

Fig. 11. Measurement of the efficiency and case temperature, operation without heatsink [$R_{G(on)}$ = 15 Ω, $R_{G(off)}$ = 0 Ω, t_{dead} = 500 ns, dv/dt = 10 V/ns, V_{DC} = 400 V, d = 100 %].

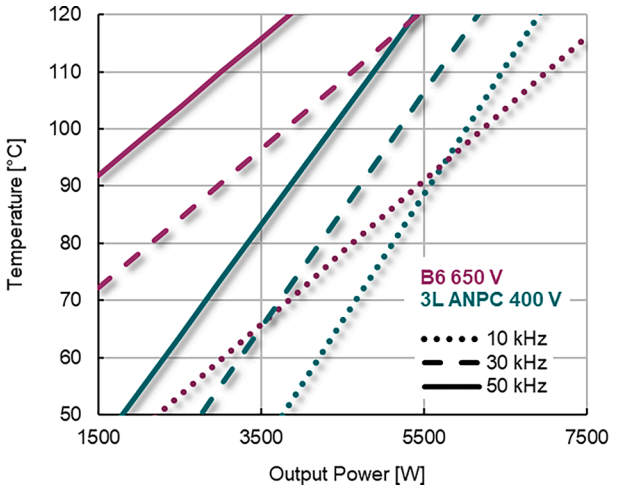

Fig. 12. Comparison of 400 V SiC MOSFET in 3L ANPC vs. 650 V SiC MOSFET in B6 topology [V_{DC} = 400 V, d = 81 %].

To identify the range where the 3 L ANPC solution with the new 400 V SiC MOSFETs offer the most benefits, the performance is compared to a common B6 topology equipped with 650 V SiC MOSFETs of the same device generation and chip size. The gate resistances are adjusted to gain comparable values of the dv/dt for both voltage classes. During these tests, no heatsink was attached to enable the measurement of the case temperature.

Fig. 12 depicts first results indicating the case temperature dependence on output power for different switching frequencies. With increasing switching frequency, the 3 L ANPC solution offers more and more benefits. This is especially true when considering that the case temperature of the MOSFET should not exceed 90 °C.

At 10 kHz, one can still see the impact of the higher conduction losses of the 400 V solution, as two devices are connected in series which results in a higher on-resistance as for a single 650 V device. With increasing switching frequency, the 3 L ANPC benefits from the advantage of the reduced switching losses. The 3 L ANPC solution also offers the option to run with higher DC voltages, as it can block 800 V compared to 650 V in the B6 topology.

Performance in 3L flying cap PFC

Introduction of the topology

The availability of hard-switching capable wide bandgap devices has led to the development of the full-bridge totem-pole topology, a simple yet highly efficient 2-level topology. This bridgeless topology eliminates diode-related losses, offering unparalleled efficiency and flexibility. It supports various control modes, including continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CrCM), and enables bi-directional power flow (Zhou, 2014; Mohan et al., 1995).

To further improve efficiency and power density, multi-level topologies are necessary. One such option is the 3-Level Flying Capacitor (FC) topology, as shown in Fig. 13. By connecting two devices in series, the voltage blocking requirement across each device is halved, resulting in reduced switching losses. The on-resistance and switching figure of merit (FOM) also improve, as it is possible to use devices with lower blocking voltages. This paves the way to higher switching frequencies, which, in addition to the advantages of the flying capacitor topology, i.e. doubled effective switching frequency and more voltage levels, enables a reduction of the boost inductance and hence its size and loss (cf. Fig. 8).

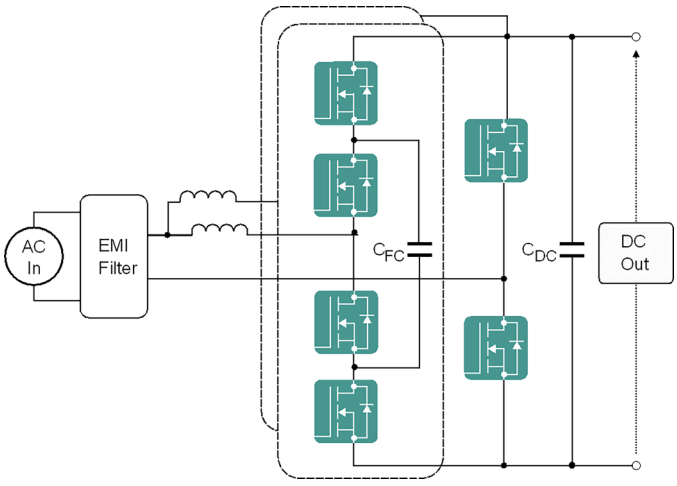

Fig. 13. Schematic of the interleaved 3-Level FC PFC.

EMI considerations and high effective switching frequency

Power supplies targeting industrial, scientific, and medical (ISM) usages need to comply with the respective EMI standards for conducted emissions in the same way as their counterparts in communication and information technology (IT) equipment. Fig. 14 shows the conducted emission limits of the relevant CISPR 22/32 / EN55022 standard. State-of-the-art designs usually try to keep their switching frequency outside the measured spectrum (i.e. below 150 kHz). Many other designs, including designs that employ a full-bridge totem-pole topology enabled by the availability of performant wide-bandgap devices (Siemieniec et al., 2019), operate at even lower frequencies, for example at 65 kHz to keep also the second harmonic out of the noise spectrum. The drawback of operation at such low switching frequencies is the need to use relatively bulky inductors. This increases the size and cost of the power factor correction (PFC) unit, and the design of a compact EMI filter inside the converter becomes challenging. As the 3rd harmonic is now found around 200 kHz, one needs to use relatively large filter components.

3-level topologies offer a different approach for modern power supplies (PSU). The use of the same switching frequency of the device as for a traditional approach results in a twofold increase in effective switching frequency at the boost inductor. As also the voltage swing across the boost inductor is reduced by 50 %, the inductor volume for the same current ripple reduces to only 25 % compared to a state-of-the-art solution, (cf. Fig. 15).

Combined with an interleaved approach as shown in Fig. 13, the

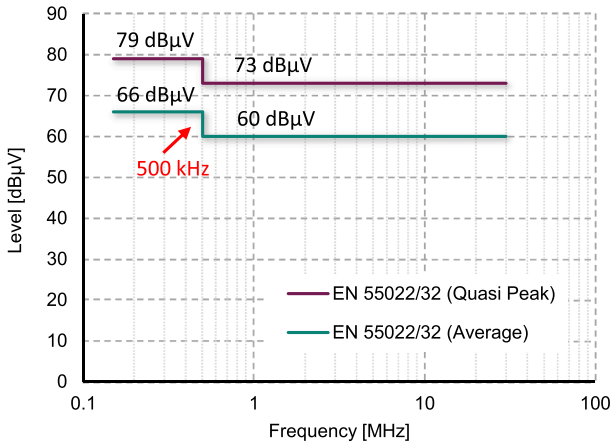

Fig. 14. Conducted emission limits for class A applications as set by EN55022.

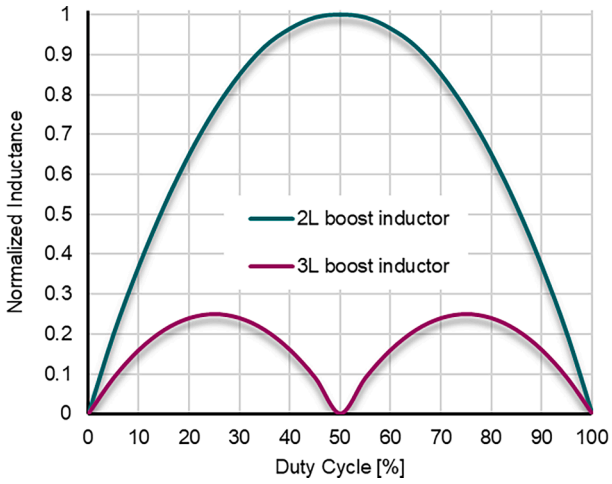

Fig. 15. Normalized inductance of the PFC choke vs. duty cycle.

effective switching frequency seen by the filter equals four times the switching frequency of the single device. This enables a significant reduction of the size of both the boost inductor and the EMI filter.

Even though the selected switching frequency does not fall within the spectrum of conducted emissions (cf. Fig. 14), one can now try to move it closer to the 500 kHz step in order to further minimize inductor and filter sizes. Overall this yields a design with a much higher power density than can be achieved with common state-of-the-art approaches.

Overview of the 3L FC PFC test board

Fig. 16 shows the board layout of a single boost stage and indicates the two commutation loops of a 3L design. The outer commutation loop is marked in blue. Here the flying capacitor is connected to either the DC voltage V_{DC} or to ground. The commutation of the flying capacitor is realized by the inner commutation loop, which is marked in pink. Both loops also serve to utilize a vertical power loop that minimizes the overall commutation inductance.

The inductor is realized with a RM12LP N49 ferrite core with an inductance of 50 µH using litz wire. The flying capacitor is placed on the bottom, and the loop inductance towards the DC link is minimized by the four MLCC capacitors close to the switching cell. The power stage uses a 400 V, 45 mΩ SiC MOSFET IMT40R045M2H. Fig. 17 depicts the realized power supply development platform. For the presented

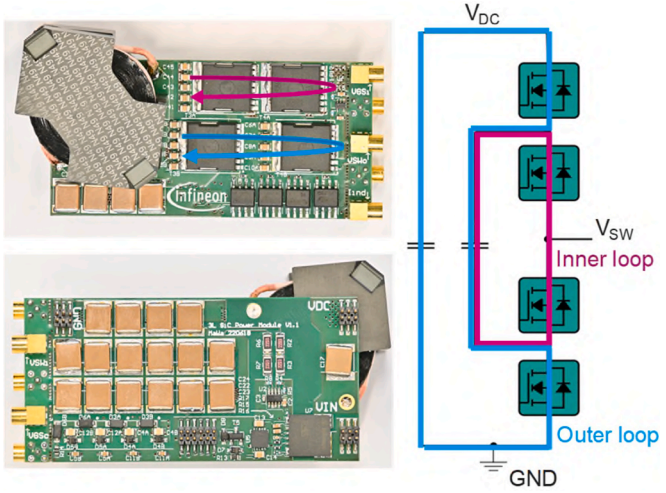

Fig. 16. View of a single 3L FC boost stage with inner (pink) and outer commutation loop (blue).

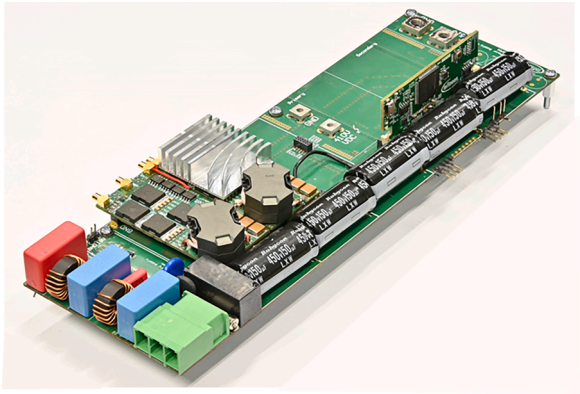

Fig. 17. View of the 3L PSU development plat-form, equipped with two 3L FC PFC stages. The controller board stands-up vertically on the right-hand side.

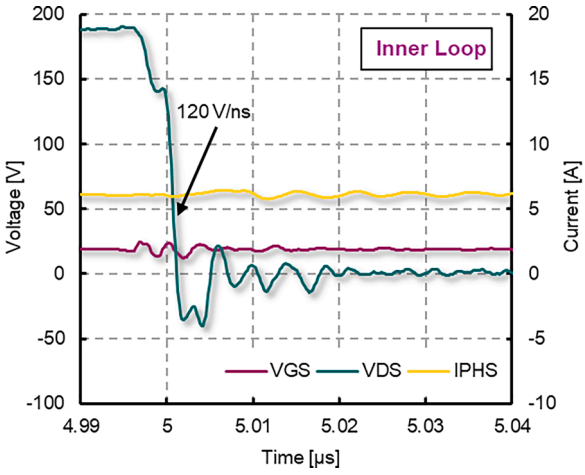

Fig. 18. Switching waveform for the low-side device on the inner loop [V_{DC} = 380 V, d = 75 %].

investigations, the board is equipped with one or two 3L boost stages, while the controller board is placed on the right-hand side. The empty area is reserved to provide space for an LLC for down-conversion to the 48 V rail.

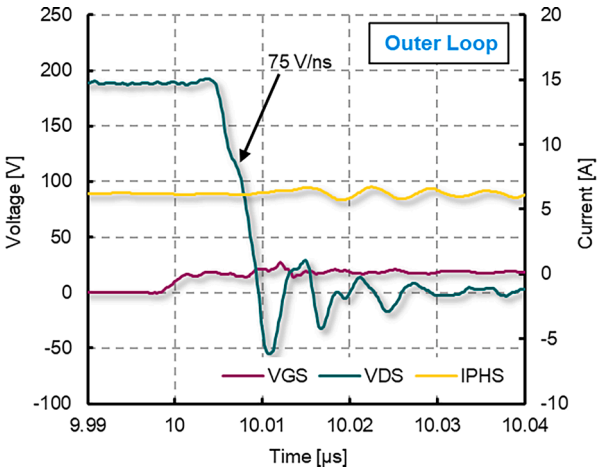

Fig. 19. Switching waveform for the low-side device on the outer loop [V_{DC} = 380 V, d = 75 %].

Experimental results

Fig. 18 shows the hard turn-on of the inner low-side switch with a DC voltage of 380 V at 7 A. Due to the usage of a multi-level design, the switch only needs to commutate 190 V. The initial drop with a plateau can be attributed to the commutation inductance after which a very rapid voltage transient is observed. The 45 mΩ SiC MOSFET achieves a maximum dv/dt of 120 V/ns, with a total transition time of <5 ns. Overall, the device delivers a very clean switching waveform with minimal ringing. The outer loop is physically larger in the layout with additional inductance, thus a more moderate dv/dt of "only" 75 V/ns is achieved as shown in Fig. 19.

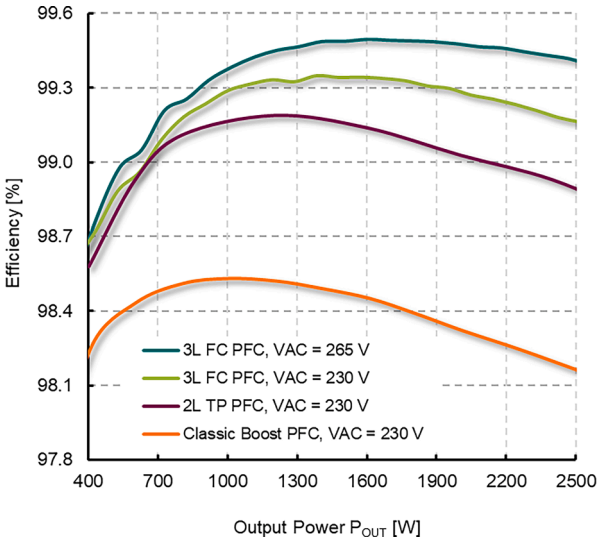

Fig. 20. Efficiency comparison between the 3L FC PFC using 400 V devices, a 2L TP PFC using 650 V devices and a classic boost PFC employing SJ devices (Yokogawa PA line filter enabled).

Next efficiency measurements are shown. The presented results use only one of the two interleaved boost stages to demonstrate the performance of a 3L topology using the new 400 V SiC MOSFET. Running at a switching frequency of 80 kHz (effectively 160 kHz), a single 3 L leg with the presented configuration is capable of delivering an output power of up to 2.8 kW. Fig. 20 compares the efficiency of this 3 L PFC with those of a common 2L 3.3 kW totem-pole (TP) PFC that uses a 650 V SiC Trench MOSFET (Siemieniec et al., 2019), and with a Classic Boost PFC employing the latest generation of SJ devices CoolMOS™ 8 (Infineon Technologies, 2024).

The 3L FC PFC outperforms the 2L TP PFC at 230 VAC whilst operating with almost 2.5 times of the switching frequency of the 2L TP PFC. The improved efficiency at maximum output power is substantial, with over 25 % lower losses. The peak efficiency improves from 99.19 % for the 2L TP PFC to 99.35 % in the case of the 3L FC PFC. Thanks to the series connection of two 400 V devices, even higher AC input voltages can be addressed easily. With an AC input voltage of 265 V, the peak efficiency of the 3L FC PFC rises to 99.58 %. Due to the increased power demand of AI in data centres, increased AC input voltage levels of up to 350 VAC are currently under consideration.

Fig. 21 shows an experimental waveform at 277 VAC input and 420 VDC link voltages. The inductor current shows the current ripple characteristic which is typical for a 3L topology: no ripple is present at a duty cycle of 50 %. This is an indication of the flying cap voltage temporarily matching the input voltage, consequently no current ripple occurs. The voltage of the flying capacitor gets naturally pinned at about half the DC-link voltage. Especially during AC operation where current alternates between positive and negative values, minimal control is required. A simple P-controller is sufficient to address any remaining offset due to non-idealities.

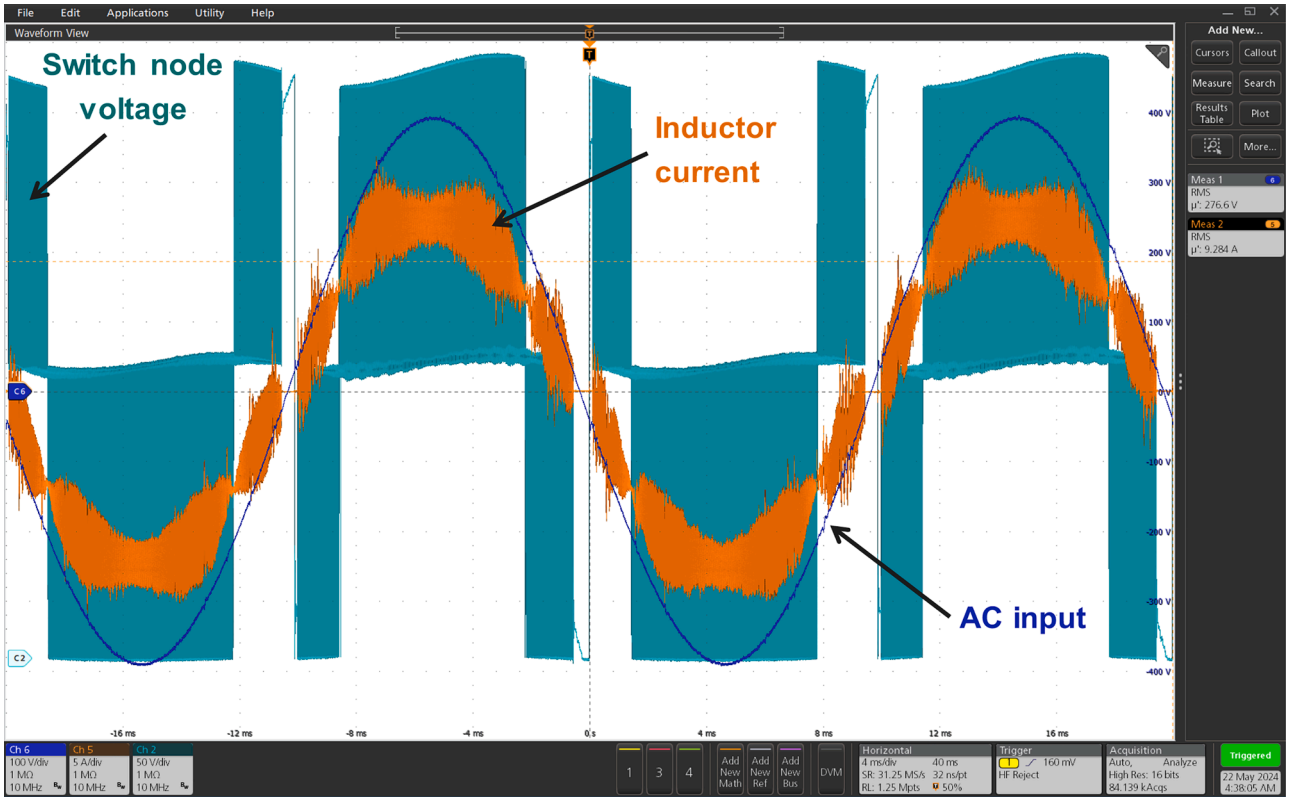

Fig. 21. Measured operation waveforms at one 3L PFC board [P_{OUT} = 2.5 kW, V_{AC} = 277 V, V_{DC} = 420 V, f_{SW} = 80 kHz, time 4 ms/div, inductor current 5 A/div, switch node voltage 50 V/div, AC input voltage 100 V/div].

Fig. 22. Temperature distribution across the PFC module without heatsink [VAC = 230 V, VDC = 380 V, POUT = 1.6 kW].

Fig. 23. Temperature distribution across the PFC module with attached heatsink [VAC = 277 V, VDC = 420 V, POUT = 2.8 kW].

Multi-level designs additionally offer the benefit of an inherent loss spreading across multiple devices. This can be seen from the thermal image presented in Fig. 22, indicating the temperature distribution across one boost stage. As no heatsink is used, one can observe a rather homogeneous heat spreading over the four devices. Fig. 23 underlines the strong impact of an attached heatsink.

Conclusion

This work introduces the new 400 V CoolSiC™ trench MOSFET technology. The new devices offer lower on-resistances and better Figures-of-Merit than existing solutions, and benefit from a flat temperature dependence of the on-resistance. Low gate-, gate-drain-, output- and reverse-recovery charges provide a fast-switching capability. The new devices offer a unique combination of performance, reliability and ease of use which enable the adoption of innovative, highly efficient topologies such as 3L FC PFC for power supplies or 3L ANPC for motor drive applications.

The performance of these devices is studied in two applications, employing a 3-phase 3L ANPC inverter and a 3L FC PFC stage.

The medium-power general purpose 3-phase 3L ANPC inverter is equipped with a total of 18 MOSFETs, and is capable of delivering up to 20 kW output power with an attached heatsink. Measurement results confirm the expected potential of the new 400 V technology, and reveal a superior inverter efficiency beyond 99.5 %. As the generated heat is spread over 18 MOSFETs, also the thermal management improves. The full potential of the devices is clearly shown in the 3L ANPC topology using higher switching frequencies of 30 … 50 kHz, which is especially attractive for solar inverters.

The 400 V devices deliver an outstanding performance in an ultra-high power-density PFC targeting next generation AI server and telecom power supplies. The measurements reveal that the device behaves well even at high switching speeds of 100 V/ns and above. The losses in the investigated PFC design are well-balanced across the different components. The achieved efficiency reaches 99.5 %, with a calculated power density of 140 W/in^3. Such power supply units pave the way to next generation AI Server and industrial SMPS, capable of offering scalable solutions to deliver an output power of 5.5 kW–8 kW and beyond.

Other application fields enabled by these new 400 V devices are battery-connected drives for light electric vehicles, which could benefit from a higher battery input voltage of 288 V (achieved by a serial instead of parallel connection) using a simple B6 topology.

CRediT authorship contribution statement

Ralf Siemieniec: Conceptualization, Investigation, Methodology, Writing – original draft, Supervision. **Martin Wattenberg:** Conceptualization, Data curation, Investigation, Software, Validation, Writing – review & editing. **Ertugrul Kocaaga:** Data curation, Investigation, Methodology, Software, Validation, Writing – review & editing. **Sriram Jagannath:** Data curation, Formal analysis, Investigation, Methodology, Validation, Writing – review & editing. **Elvir Kahrimanovic:** Conceptualization, Methodology, Resources, Supervision, Validation, Writing – review & editing. **Jyotshna Bhandari:** Conceptualization, Data curation, Formal analysis, Investigation, Methodology, Project administration, Supervision, Validation, Writing – review & editing. **Heejae Shim:** Data curation, Formal analysis, Investigation, Methodology, Validation, Visualization, Writing – review & editing. **Alberto Pignatelli:** Data curation, Formal analysis, Investigation, Validation, Visualization, Writing – review & editing.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Ralf Siemieniec has patent issued to Infineon Technologies AG. Jyotshna Bhandari has patent pending to Infineon Technologies AG. Martin Wattenberg has patent pending to Infineon Technologies AG. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

The authors do not have permission to share data.

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