New 400 V SiC MOSFET and its use in Multi-Level Applications

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***Abstract*—With the introduction of the first ever 400 V SiC MOSFET technology, a gap which previously existed in the voltage range between 200 V medium-voltage MOSFET and 600 V super-junction MOSFET is closed. The new technology offers low switching losses and low on-state resistance and represents a perfect fit for 2-level topologies in 288 VDC systems or 3-level topologies working from 230 V AC to 350 VAC or 400 VDC to 550 VDC input voltages. The technology concept is briefly introduced. The expected efficiency and power density gains are verified by measurements in an appropriate test board representing a 2.5 kW 3-level PFC and are compared with the results of a common 2-level totem-pole PFC using a 650 V SiC MOSFET, as well as a classic boost PFC solution.**

Keywords—component, SiC MOSFET, 400 V, power supply, PFC, multi-level application, efficiency

I. Introduction

This work introduces a new SiC Trench MOSFET technology with 400 V nominal blocking voltage. The technology is well-suited to address the needs of a wide range of applications including server and telecom switch-mode power supplies (SMPS), solar inverters, energy storage, battery switches or main inverters in light electric vehicles and forklifts.

With the introduction of high-performance devices in the 400 V class, a previously poorly-addressed gap is closed. Scaling-up existing medium-voltage 200 V MOSFETs that employ lateral charge-compensation by means of an isolated deep field-plate is not ideal. Similarly, scaling-down existing 600 V SJ MOSFET technologies is problematic. In both cases, the application performance suffers from the compromises originating from the specific device set-ups, namely large input-, output- and reverse-recovery charges, and a pronounced drop in the output- and Miller- capacitance with increasing drain voltage. These device properties prevent the devices finding common usage in hard-switching applications employing half- or full-bridge topologies.

The new 400 V SiC MOSFET devices combine small gate-, output- and reverse-recovery charges, and a much more linear output- and Miller-capacitance over drain voltage with a small on-resistance. The linked ultra-low switching and conduction losses promise a clearly improved system efficiency and power density in the targeted application fields. The devices are a perfect fit for all 3-level topologies with an input voltage between 230 V and 350 V RMS AC input / 400 V to 550 V DC link voltage, and for any 2-level topology with a 288 V DC link or battery bus voltage.

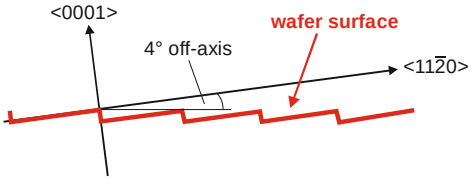

Fig. 1 Schematic illustration of the 4° off-axis cut of 4H-SiC wafers

II. Device Technology

A. General considerations

Wide band-gap semiconductors based on silicon-carbide are very attractive for power devices due to their low losses, improved temperature capability and high thermal conductivity, and have recently developed into a mature technology. While the use of a wide-bandgap material such as silicon carbide offers many advantages over silicon, there are some noteworthy differences. This leads to several challenges when employing the 4H-SiC polytype which is the most prominent silicon-carbide polymorph used for power semiconductor devices:

- SiC has a higher surface density of atoms per unit area compared to Si, resulting in a higher density of dangling Si- and C- bonds and carbon clusters at the interface. Defects located in the gate oxide layer near to the interface may appear in the energy gap and act as traps for electrons [1].
- SiC devices allow much higher drain-induced electric fields in the blocking mode compared to their Si counterparts and thus require a limitation of the electric field in the gate oxide to maintain reliability [2].
- SiC devices show a higher Fowler-Nordheim current injection compared to Si devices due to a smaller barrier height, consequently the electric field on the SiC side of the interface must be limited [3],[4].

Consequently, one challenge of SiC MOSFETs is the low electron mobility at the SiO_2/SiC interface due to carbon-related interface defects. Due to electron scattering and trapping at such point defects at the interface, the channel mobility is typically only a fraction of the bulk mobility of ca. 400 cm²/Vs (the value at a bulk doping level equal to the channel doping) [5]. Another challenge is the 4 ° off-axis tilt of commercially available SiC substrates. This is a consequence of the need for epitaxial layer growth. Due to the tilt, the wafer surface does not perfectly coincide with the (0001) crystal c-plane, causing increased surface roughness and steps when fabricating a MOS structure at the wafer surface. This situation is schematically illustrated in Fig. 1.

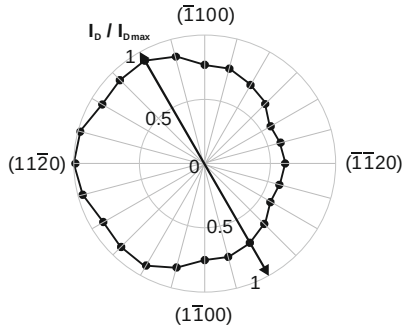

Fig. 2 Relative channel mobility for various trench planes of 4H-SiC on-axis substrate [6]

This off-axis cut obviously imposes a challenge on devices using a lateral channel and will have a strong impact on the channel properties in addition to the usual limitations imposed by the cell pitch shrink. Nevertheless, the off-axis cut also affects trench MOSFET technologies, as a vertically etched trench will result in sidewalls with different roughness, performance and reliability. Studies show that the vertical channel mobility strongly depends on the crystal plane with a factor of almost two between worst and best channel mobility as indicated in Fig. 2 [6]. A suitable post-oxidation annealing step like a nitric oxide annealing can reduce the interface state density significantly [7]. The conditions of the post-oxidation anneal (POA) also affect the stability of the threshold voltage. An optimized POA provides high channel mobility and high threshold voltage stability at the same time.

The limitation of the electric field strength in the blocking state needs to be addressed by appropriate device design measures like a buried shielding region.

B. *400 V trench MOSFET structure*

The general device structure follows the design approach introduced previously [8],[9]. Fig. 3 gives a schematic cross section of the general cell concept. The active channel aligns along the a-plane which gives the best channel mobility and the lowest interface trap density. The gate oxide is protected by deep p-wells that are connected to the source electrode at the semiconductor surface. As the 2nd trench sidewall does not coincide with this crystal plane, it is not used as an active channel. Instead, the buried p-region is connected to the source electrode along the inactive sidewall. This leads to a very compact cell design and, in combination with the high channel mobility of the a-plane, to a low area-specific on-resistance.

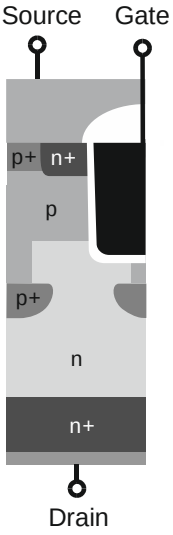

Fig. 3 SiC Trench MOSFET concept with an asymmetric channel

While the new 400 V MOSFET is similar to the previously introduced designs of the first device generation [9],[10], it benefits from the continuous improvements of the technology that, for example, enable a clearly reduced cell pitch and further improved channel properties or improved control over the drift region properties. Additionally, the chip design is carefully optimized to avoid any unnecessary active area loss, for example by the optimization of the junction termination design.

C. *Device properties*

As a typical example, Fig. 4 indicates the most important device property improvements of the new 400 V device over a 650 V device of the same technology generation, with an identical chip size in a common TO-263-7 (D2PAK 7pin) package. All values are averaged over a batch of devices to account for typical production variations. The comparison clearly reveals lower values for the 400 V technology, indicating the huge potential of this new voltage class.

In addition, the substantially lowered on-resistance values underline the advantages of a trench technology, which benefits from a much better channel mobility compared to typical DMOS devices with a lateral channel.

These good parameters are complemented by a rather flat temperature dependence of the on-resistance $R_{DS(on)}$ as shown

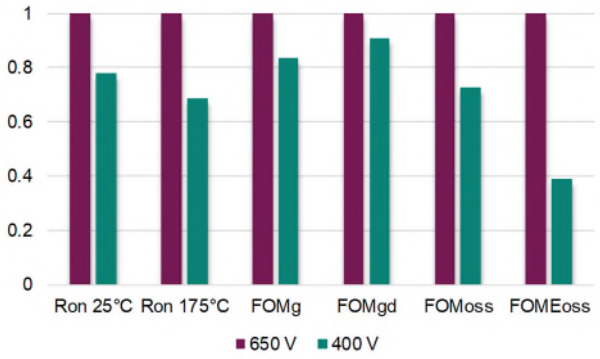

Fig. 4 Realized parameter improvements of the 400 V technology with respect to the 650 V device technology (identical chip size in a TO-263-3 package)

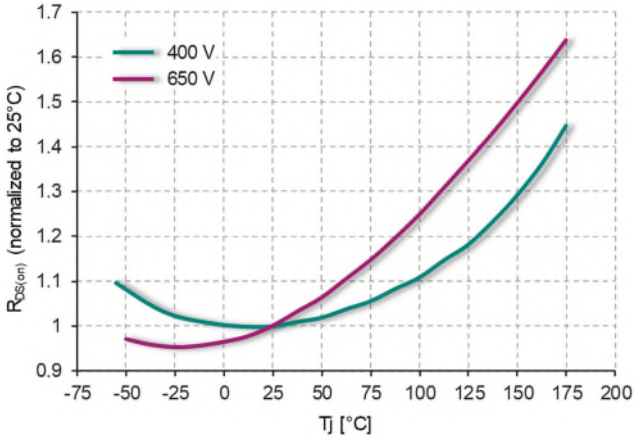

Fig. 5 Temperature dependence comparison of normalized on-resistance

in Fig. 5. The value only increases by 11 % from 25 °C to 100 °C in the case of the new 400 V device. This property allows a MOSFET with higher $R_{DS(on)}$ to be chosen, with the benefit of lower costs and better switching performance.

III. Performance in 3-Level PFC

A. Advantages of a 3-Level topology

With the availability of hard-switching capable wide bandgap devices, the full-bridge totem-pole topology emerged as a simple 2-level topology capable of providing the highest practically achievable efficiency. This topology is bridgeless, so it completely eliminates any diode-related losses [11]. The topology can be operated in many different control modes [12] including CCM, DCM, CrCM etc., and is intrinsically capable of providing a bi-directional power flow. However, to further improve the efficiency, and in particular to increase the power density in order to realize smaller units, multi-level topologies must be chosen.

One such option is the 3-Level Flying Capacitor topology, as schematically depicted in Fig. 6. Here, two devices connect in series for the same DC output voltage; consequently the voltage drop over each device reduces by half – which directly translates into reduced switching losses. Additionally, on-resistance and switching FOM improve, as devices with lower blocking voltages can be used. This paves the way to higher switching frequencies, which, in addition to the advantages of the flying capacitor topology, i.e. doubled effective switching frequency and more voltage levels, enables a reduction of the boost inductance and hence its size. The combination with an interleaved approach as depicted in Fig. 6 opens the door to an even higher power density.

B. EMI considerations

Power supplies marketed for industrial, scientific, and medical (ISM) usages need to comply with the respective EMI standards for conducted emissions in the same way as their counterparts in communication and information technology (IT) equipment. For example, Fig. 7 shows the conducted emission limits of the CISPR 22/32 / EN55022 standards, which cover a wide range of applications. Traditional designs try to keep their switching frequency outside the measured spectrum (i.e. below 150 kHz). Many designs, including designs that employ a full-bridge totem-pole topology [10], operate at even lower frequencies, for example at 65 kHz. This approach keeps the second harmonic (i.e. at 130 kHz) out of

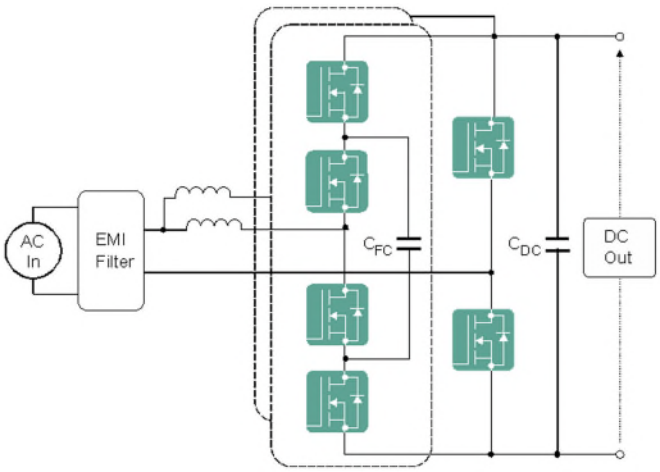

Fig. 6 Schematic of the interleaved 3-Level FC PFC

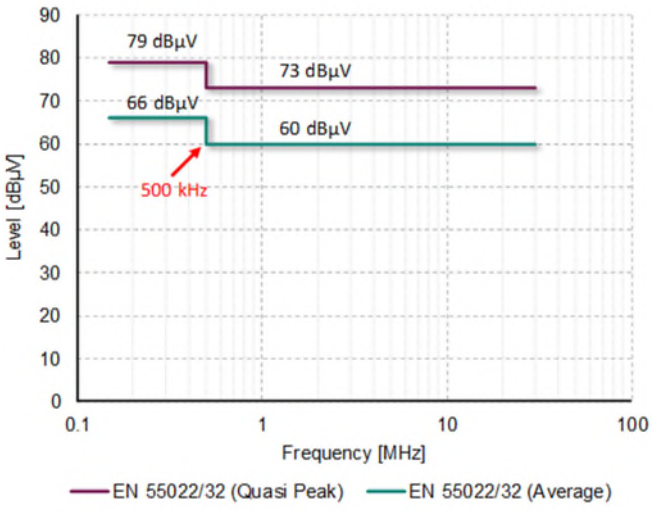

Fig. 7 Conducted emission limits for class A applications as set by CISPR/EN 32/55022

the noise spectrum. However, operation at such low switching frequencies requires the use of relatively bulky inductors, thus increasing the size and cost of the power factor correction (PFC) unit. Additionally, the design of a compact EMI filter inside the converter remains challenging, as the 3rd harmonic is now found around 200 kHz and requires the use of relatively large filter components.

However, a different approach can be chosen for modern power supplies (PSU). Instead of selecting a fundamental switching frequency outside of the measured spectrum, one can move it close to the step at 500 kHz (see Fig. 7). The much higher switching frequency allows a significant shrink not only of the boost inductor, but also of the EMI filter. In addition, it might be possible to mitigate bulky electrolytic dc-link capacitors by utilizing the flying capacitor for power pulsation buffering [13]. All these benefits directly translate into a higher power density, either via a smaller form factor at the same power level, or via an increased output power for a unit of the same size.

C. Achieving 500 kHz effective switching frequency

Several conditions need to be fulfilled to achieve multi-kilowatt power conversion with switching frequencies close to 500 kHz mark:

- The use of wide-bandgap semiconductors, such as Gallium-Nitride (GaN) or Silicon-Carbide (SiC) devices, enables operation at much higher frequencies without generating higher losses which would be the case with Silicon devices.
- An effective switching frequency enhancement needs to be provided by the chosen topology, e.g. via interleaving or via multi-level topologies. Due to the inherent frequency multiplication, the Flying Capacitor Multi-Level (FCML) converter represents an especially attractive solution.
- To support fast switching transients found in multi-level applications, power semiconductors must provide appropriate FOMs in the suitable voltage classes.

The new 400 V SiC MOSFET meets the aforementioned requirements. The performance and benefits of a new 400 V

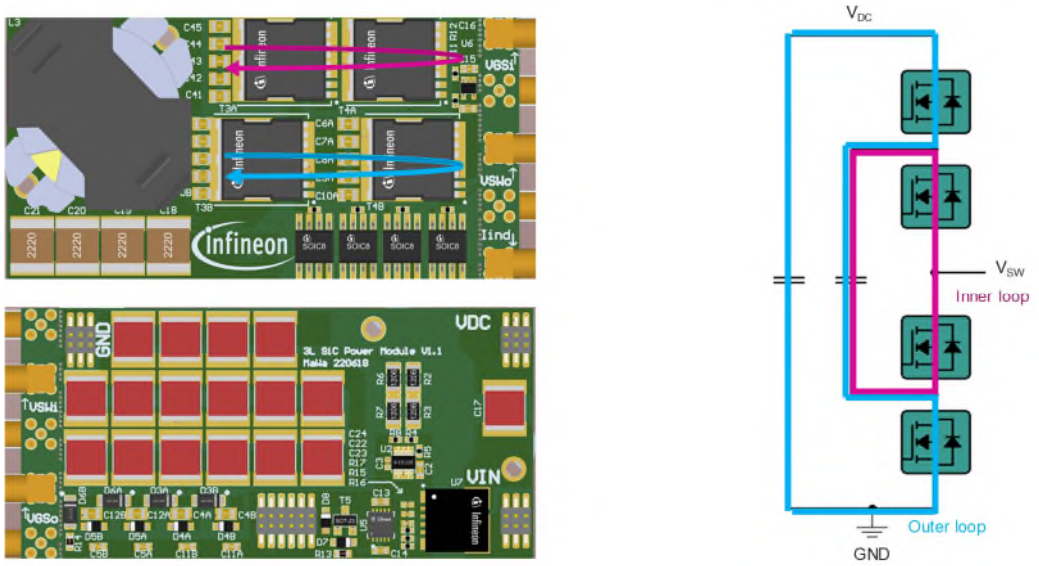

Fig. 8 View of a single 1.5 kW 3L FC boost stage with inner (pink) and outer commutation loop (blue). The board is 32 mm by 60 mm in size.

45 mΩ device are now investigated in a 3-Level FC PFC stage.

D. Single-stage test board overview

The basic schematic of the 3L FC PFC has already been shown in Fig. 6. Assuming each individual MOSFET switches at 125 kHz, this results in an effective switching frequency of a single 3L boost stage of 250 kHz. To further raise the effective frequency seen by the EMI filter, a second interleaved stage is used. With this approach, the PFC reaches an effective frequency slightly below 500 kHz.

Fig. 8 shows the board layout of a single boost stage and indicates the two commutation loops of a 3L design. The outer commutation loop is marked in blue. Here the flying capacitor is connected to either the DC voltage V_{DC} or to ground. The commutation of the flying capacitor is realized by the inner commutation loop, which is marked in pink. Both loops also serve to utilize a vertical power loop that minimizes the overall commutation inductance. To also allow evaluation below 125 kHz, the flying capacitor is oversized and placed on the bottom. In addition, the loop inductance towards the DC link is minimized by the four MLCC capacitors close to the switching cell.

Fig. 9 shows the realized single-stage board. The mounted cooler is especially designed to provide an optimized air flow.

E. Experimental evaluation under DC conditions

The performance of the single power stage with inductor is studied under DC conditions at different current and voltage levels and is presented here, followed by measurements with an AC input.

The inductor is realized with a RM10LP ferrite core. The targeted inductance of 40 µH was experimentally optimized using different litz wire diameters. The power stage uses a 400 V, 45 mΩ SiC MOSFET.

Fig. 10 shows the hard turn-on of the inner low-side switch with a DC voltage of 380 V at 7 A. Due to the usage of a multi-level design, the switch only needs to commutate 190 V. The initial drop with a plateau can be attributed to the commutation inductance after which a very rapid voltage transient is observed. The 45 mΩ SiC MOSFET achieves a maximum dV/dt of 120 V/ns, with a total transition time of less than 5 ns. Overall, the device delivers a very clean switching waveform with minimal ringing. The outer loop (not shown) is physically larger in the layout with additional inductance, thus a more moderate dV/dt of “only” 75 V/ns is achieved.

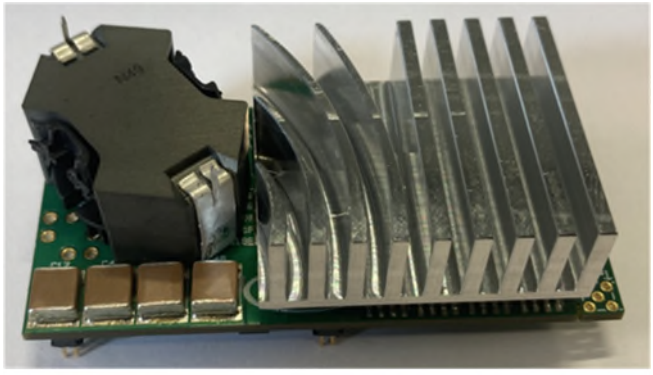

Fig. 9 View of the single-stage board with mounted cooler

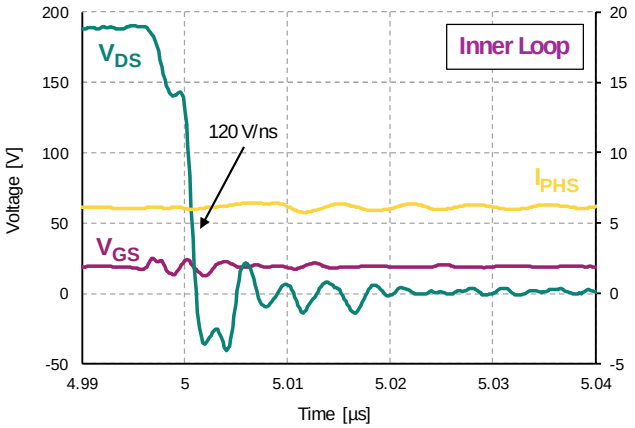

Fig. 10 Switching waveform for the low-side device on the inner loop [V_{DC} = 380 V, d = 75 %]

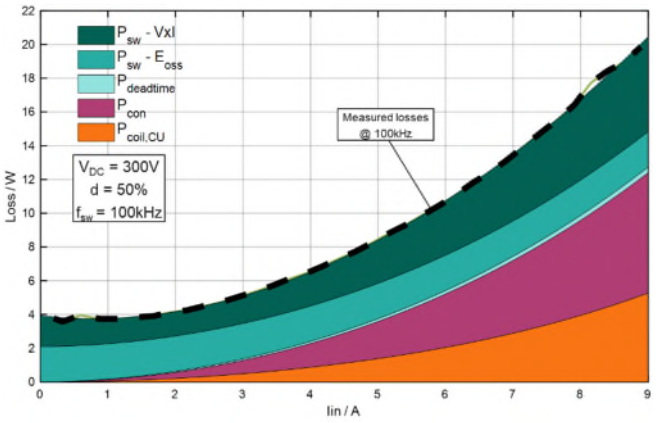

Fig. 11 Loss split for step-up operation: DC-link voltage V_{DC} = 300 V, input voltage V_{IN} = 150V at 100 kHz

Fig. 11 shows the loss split at 50 % duty cycle. This operation point is of particular interest as there is no current ripple, with the following implications:

- no hysteresis losses in the magnetic core
- no skin / proximity related winding losses
- pure DC current in the inductor, no frequency dependency of related losses
- always hard turn-on of the low-side and ZVS turn-off of the high-side switch

To determine these values, a hybrid approach was used that combined measurements and analytic calculations. Under the indicated conditions, the losses distribute very well across the different components, and there is little room for further optimization. However, the loss composition is expected to change for different duty cycles, e.g. 25 % or 75 %, where current ripple is at its maximum.

Fig. 12 depicts the measured efficiency for different switching frequencies under DC-conditions for a single 3L stage. The efficiency is very flat across the load range considered and reaches a peak efficiency of 99.25 %. At full load there is only a minor difference in efficiency between 80 kHz and 120 kHz. Beyond 120 kHz, the efficiency slowly starts to degrade. The maximum case temperature of the

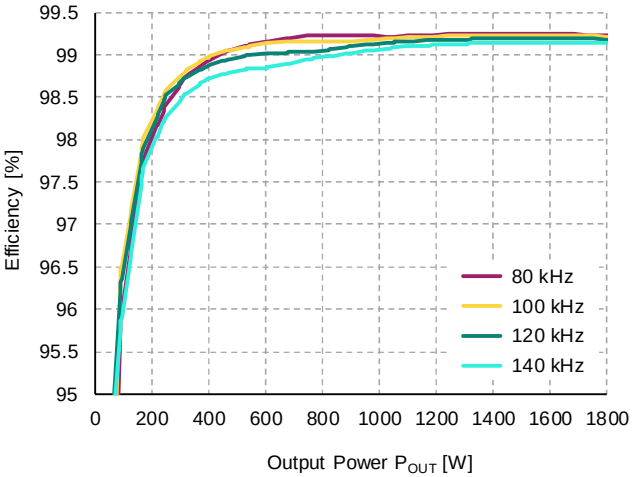

Fig. 12 Measured efficiency of a single stage 3-Level FCML PFC (V_{DC} = 380 V, V_{IN} = 285 V, duty cycle = 25 %)

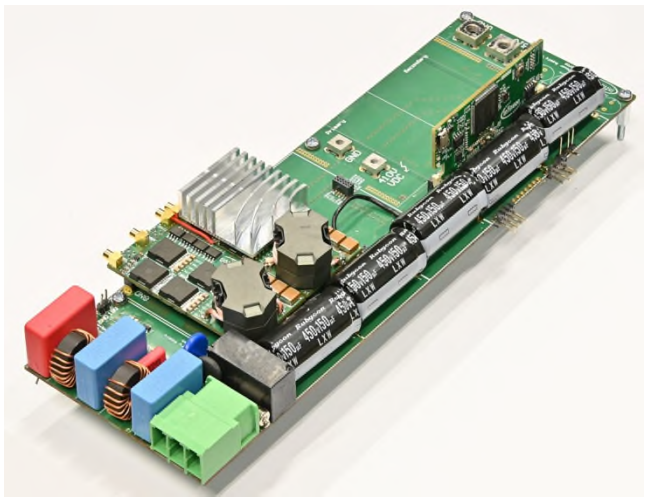

Fig. 13 View of the 3L power supply development platform, equipped with two 3L FC PFC stages. The controller board stands-up vertically on the right-hand side.

SiC MOSFET at full load increases over the switching frequency from 81 °C to 96 °C, offering a sufficient margin for the design.

F. Experimental results of the complete PFC stage

After having done the characterization of a single-stage board under DC conditions, the investigation focuses on the performance of the complete interleaved PFC. Fig. 13 depicts the realized power supply development platform. For the presented investigations, the board is equipped with two 3L boost stages, while the controller board is placed on the right-hand side. The empty area is reserved to provide space for an LLC for down-conversion to the 48 V rail. A hold-up extension circuit allows more energy out of the DC-link to be utilized, thus reducing its size.

The results presented in the following use only one of the two interleaved boost stages to demonstrate the performance achievable with a 3L topology using the 400 V SiC MOSFET. Even though Fig. 12 shows only minimal degradation of efficiency between 80 kHz and 120 kHz, 80 kHz was chosen for the following comparison as it shows the highest efficiency. Future work will address the operation of two interleaved stages along with pre-compliance measurements.

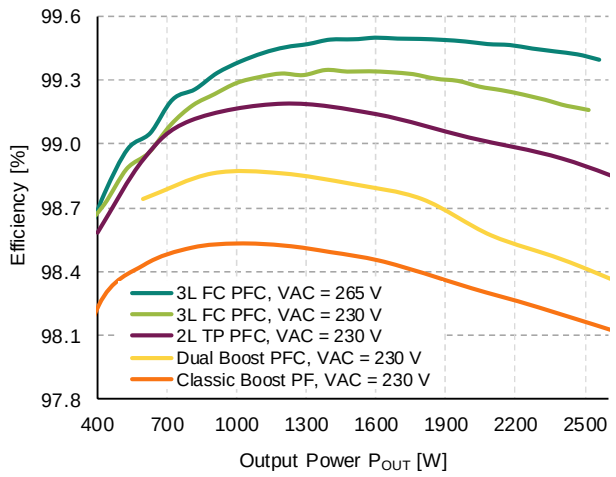

Fig. 14 Efficiency comparison between the 3L FC PFC using 400 V devices, a 2L TP PFC using 650 V devices and a classic and dual boost PFC employing SJ devices

Running at 80 kHz (effectively 160 kHz) a single 3L leg that uses a 45 mΩ 400 V SiC MOSFET is well-capable of running 2.5 kW of output power. Therefore an efficiency comparison with a common 2L 3.3 kW totem-pole (TP) PFC that uses a 650 V SiC Trench MOSFET as introduced in [10], as well as with a Classic or Dual Boost PFC employing SJ devices [14] is carried out. For the efficiency comparison presented in Fig. 14, the 3L FC PFC and 2L TP PFC respectively use 400 V [15] and 650 V SiC MOSFETs [16] of the same device generation. The Dual Boost PFC uses CoolMOS P7 with $R_{DS(on),typ}$ = 26 mΩ [17], while the Classic Boost PFC uses CoolMOS™ 8 devices with $R_{DS(on),typ}$ = 31 mΩ [18].

The 3L FC PFC outperforms the 2L TP PFC at an AC input voltage of 230 V while operating with almost 2.5x of the switching frequency of the 2L TP PFC. The difference in efficiency at 2.5 kW is substantial: 99.15 % vs. 98.9 %, or over 25 % fewer losses in the power conversion. This translates into significantly lower cooling efforts, for example in data centers. Also, the peak efficiency improves from 99.19 % for the 2L TP PFC to 99.35 % in case of the 3L FC PFC. With series connection of two 400 V devices, giving a theoretical blocking voltage of 800 V, even higher voltages can be addressed easily. With the increased power demand of AI in data centers, AC input voltage levels of 277 VAC or even up to 350 VAC are under consideration.

Fig. 15 shows an experimental waveform at 277 VAC input and 420 VDC link voltages. The inductor current shows the characteristic phenomenon in the current ripple that is typical for a 3L topology: no ripple is present at a duty cycle of 50 %. An indication of the flying cap voltage can be seen in the switch node voltage. The additional third level of the 3L FC topology is located in the middle of the switching pattern at half the DC-link voltage so it closely tracks the 100 Hz ripple of the DC link. A simple P-controller is sufficient to accomplish this behavior.

As can be seen from Fig. 14, an increase in the AC input voltage level is also beneficial for the efficiency. In case of 265 VAC, the peak efficiency further increases to a peak value of 99.58 %. Also, the efficiency at the maximum output power of 2.5 kW rises to 99.39 %. This again results in 25 % lower losses, translating into further reduced cooling efforts.

IV. Conclusion

This work introduces the new 400 V CoolSiC™ trench MOSFET technology, which closes a long-standing gap between 200 V medium-voltage MOSFETs and 600V super-junction and SiC MOSFETs. The new devices offer a unique combination of performance, reliability and ease of use and enable the adoption of innovative, highly efficient topologies as 3L PFC for power supplies or 3L ANPC for motor drive applications or with blocking capabilities of up to 800 VDC.

The new 400 V MOSFETs offer lower on-resistances and better Figures-of-Merit than existing solutions, and benefit from a flat temperature dependence of the on-resistance. Low gate-, gate-drain, output- and reverse-recovery charges provide a fast-switching capability.

The device performance has been investigated in an ultra-high power density PFC targeting next generation AI server and telecom power supplies. The measurements reveal that the device behaves well even at high switching speeds of 100 V/ns and above. The losses in the investigated PFC design are well-balanced across the different components. The achieved efficiency reaches 99.5 %, with a calculated power density of 140 W/in³. Such power supply units pave the way to next generation AI Server and industrial SMPS, capable of offering scalable solutions to deliver an output power of 5.5 kW – 8 kW and beyond.

Other application fields enabled by these new 400 V devices include motor-drives employing a 3L ANPC inverter topology [19], or battery-connected drives for light electric vehicles, which could benefit from a higher battery input

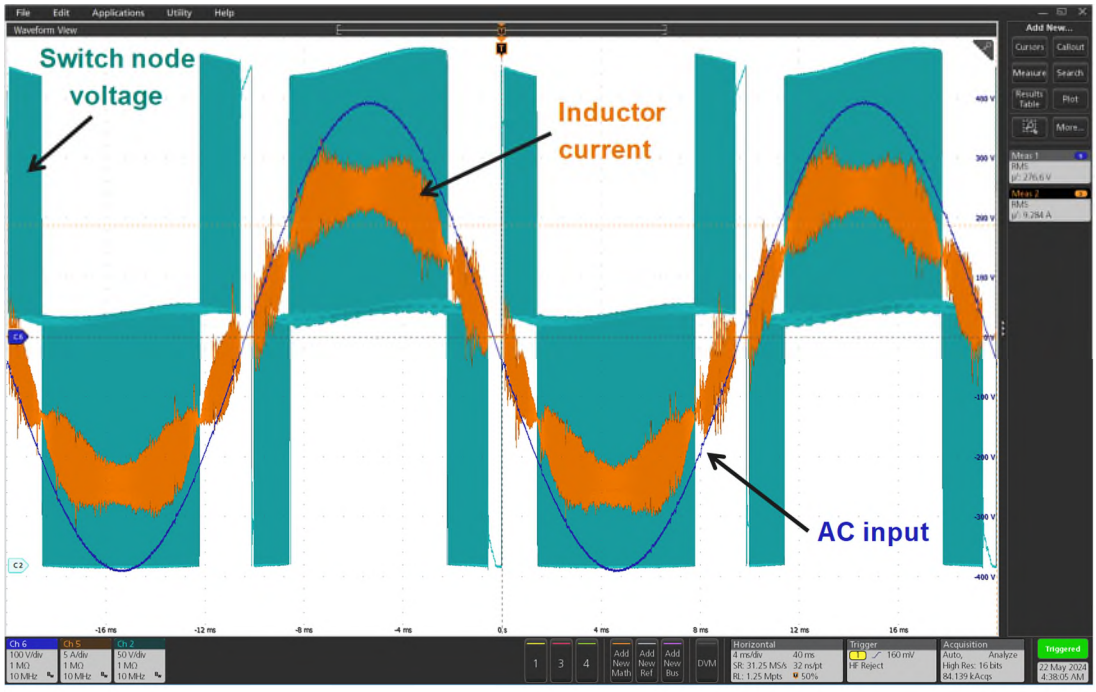

Fig. 15 Measured operation waveforms at one 3L PFC board [V_{DC} = 420 V, V_{AC} = 277 V, f_{SW} = 80 kHz, P_{OUT} = 2.5 kW, time 4 ms/div, switch node voltage 50 V/div, AC input voltage 100 V/div, inductor current 5 A/div]

voltage of 288 V (achieved by a serial instead of parallel connection) using a simple B6 topology.

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REFERENCES

[1] Z. Chbili, A. Matsuda, J.Chbili, J.T. Ryan, J.P. Campbell, M. Lahbabi, D.E. Ioannou, and K.P. Cheung.: Modeling Early Breakdown Failures of Gate Oxide in SiC Power MOSFETs, IEEE Trans. Electr. Dev., Vol. 63, No. 9, pp. 3605-3613, 2016

[2] J. Lutz, T. Aichinger and R. Rupp.: Reliability Evaluation, in K. Suganuma (Ed.): Wide Bandgap Power Semiconductor Packaging: Materials, Components, and Reliability, Elsevier, 2018

[3] R. Singh, and A.R. Hefner.: Reliability of SiC MOS devices, Solid-State Electronics, Vol. 48, pp. 1717–1720, 2004

[4] K. Matocha.: Challenges in SiC power MOSFET design, Solid-State Electronics, Vol. 52, pp. 1631–1635, 2008

[5] W.J. Schaffer, H.S. Kong, G.H. Negley and J.W. Palmour.: Hall effect and CV measurements on epitaxial 6H-and 4H-SiC, Institute of Physics Conference Series, Vol. 137, pp. 155-160, Bristol, 1994

[6] H. Yano, H. Nakao, T. Hatayama, Y. Uraoka and T. Fuyuki.: Increased channel mobility in 4H-SiC UMOSFETs using on-axis substrates, Materials Science Forum, Vols. 556-557, pp. 807-811, 2007

[7] T. Kimoto, Y. Kanzaki, M. Noborio, H. Kawano and H. Matsunami.: Interface properties of Metal-Oxide-Semiconductor Structures on 4H-SiC{0001} and (11-20) Formed by N2O Oxidation, Jap. Journ of Appl. Phys., Vol. 44, No. 3, pp. 1213-1218, 2005

[8] D. Peters, T. Basler, B. Zippelius, T. Aichinger, W. Bergner, R. Esteve, D. Kueck and R. Siemieniec. “The new CoolSiC™ Trench MOSFET Technology for Low Gate Oxide Stress and High Performance”, Proc. PCIM, Nuernberg, 2017

[9] R. Siemieniec, D. Peters, R. Esteve, W. Bergner, D. Kück, T. Aichinger, T. Basler and B. Zippelius.: A SiC Trench MOSFET concept offering improved channel mobility and high reliability, Proc. EPE, Warsaw, Poland, 2017

[10] R. Siemieniec, R. Mente, W. Jantscher, D. Kammerlander, U. Wenzel and T. Aichinger.: 650 V SiC Trench MOSFET for high-efficiency power supplies, Proc. EPE, Genova, Italy, 2019

[11] B. Zhou.: CCM Totem-Pole Bridgeless PFC with Ultra-Fast IGBT, Master Thesis, Virginia Polytechnic Institute and State University, Blacksburg, USA, 2014

[12] N. Mohan, T. M. Undeland and W. P. Robbins.: Power Electronics – Converters, Applications, and Design – 2nd Edition, John Wiley & Sons, USA, 1995

[13] D. Menzi, S. Weihe, J.A. Anderson, J. Everts and J.W. Kolar.: Single-Phase PFC Rectifier With Integrated Flying Capacitor Power Pulsation Buffer, IEEE Open Journal of Power Electronics, 2022

[14] R. Siemieniec, R. Mente, M. Kutschak and F. Pulsinelli.: Power device solutions for highly efficient power supplies, Proc. ISPS, Prague, Czech Republic, 2021

[15] Infineon Technologies.: CoolSiC™ MOSFET 400 V G2, Available at: https://www.infineon.com/cms/en/product/power/mosfet/silicon-carbide/discretes/imbg40r045m2h/

[16] Infineon Technologies.: CoolSiC™ MOSFET 650 V G2, Available at: https://www.infineon.com/cms/en/product/power/mosfet/silicon-carbide/discretes/imza65r040m2h/

[17] Infineon Technologies.: CoolMOS™ P7, Available at: https://www.infineon.com/cms/en/product/power/mosfet/n-channel/500v-950v/coolmos-p7/

[18] Infineon Technologies.: CoolMOS™ 8 power transistor, Available at: https://www.infineon.com/cms/en/product/power/mosfet/n-channel/500v-950v/ipw60r037cm8/

[19] O. Song, R. Siemieniec, E. Kahrimanovic, E. Kocaaga, J. Bhandari, A. Pignatelli, W.-J. Chen, H. Shim, S. Jagannath.: New 400 V SiC MOSFET technology delivering highest efficiency in three-level industrial drive applications, Proc. PCIM Asia, Shenzhen, China, 2024