# Next step in power MOSFET evolution boosts application efficiency

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***Abstract*— This work introduces the characteristics and properties of the latest trench MOSFET technology released to the market. Based on the advantages of a revolutionary new cell design combined with the benefits of an advanced manufacturing technology, this new device family brings together the benefits of exceptionally low conduction losses, superior switching performances, improved SOA and good ruggedness. Typical applications for these MOSFETs include telecom, server, datacom as well as solar applications, motor drives, drones, e-bikes, power tools and many other battery-powered applications. Application tests using the new devices reveal clear efficiency improvements.**

***Keywords—power semiconductor device, MOSFET, new switching devices, efficiency, resonant converter, motor drives***

## I. Introduction

MOSFET technologies have always been noted as excellent candidates to be used as switches in power management circuits. Starting in the late seventies with the commercial introduction of vertical diffused MOSFET (VDMOS) structures (Fig. 1a), these devices offered an appealing alternative to bipolar technologies that dominated the power semiconductor arena at the time, thanks to their superior switching performance in combination with a high input impedance [1]. Nevertheless, the high on-state resistance limited the current-handling capabilities of the VDMOS and hence its use in power electronics applications. For medium-voltage devices, the total on-state resistance between drain and source was set by the intrinsic channel resistance, and by the JFET region between the body regions, which limits the channel current flow into the drift region.

It took more than a decade of development in device design and process engineering to overcome these limitations. In the late 1980s, the appearance of the first trench gate MOSFETs (Fig. 1b) marked a milestone for the broad adoption of field-effect transistors in the power electronics industry [1]-[3]. Moving the channel into the vertical direction, this device concept virtually removed the JFET region and reduced the on-state resistance. However, the remarkable increase in cell density also brought to light

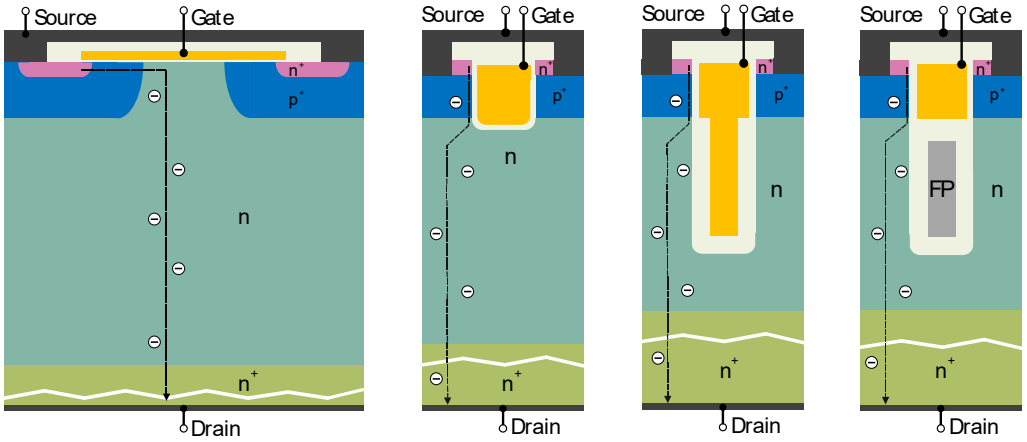


Fig. 1a-d: Exemplary device structures depicting the evolution of power MOSFET:
a) VDMOS structure with lateral channel and planar gate
b) Trench MOSFET structure with vertical channel
c) Trench MOSFET with lateral charge-compensation by a gate-connected field plate
d) Trench MOSFET with lateral charge-compensation by an insulated field plate connected to source

significant disadvantages. The gate-drain capacitance and gate-source capacitance both increased linearly with the number of trenches, i.e. with the cell density. Since the MOSFET is uniquely controlled through its gate terminal, the gate driver circuitry has to provide the total gate charge $Q_G$ required to turn on the transistor. In the case of high switching frequency applications such as switched-mode power supplies (SMPS), the lowest gate charge is desirable since it proportionally reduces the driving losses. A part of the total gate charge is associated with the gate-to-drain charge $Q_{GD}$, which governs the drain voltage transient. Larger values of $Q_{GD}$ affect the transient speed, resulting in an increase in the switching losses, and additionally force the use of longer dead-times. Additionally, another constraint is imposed by the Miller charge ratio: $Q_{GD}/Q_{TH}$ must be lower than one. This is needed in order to ensure an intrinsic robustness against parasitic turn-on of the MOSFET under fast drain voltage transients [4].

The introduction of charge-compensated structures, exploiting the same principle as super junction devices, marked the beginning of a new era. The introduction of devices employing an insulated deep field plate as an extension of the gate electrode enabled the lateral depletion of the drift region in the off state (Fig. 1c) [5]. The lateral depletion alters the electric field distribution throughout the structure, and it is possible to block the same voltage within a shorter length. In turn, the electric field can now be supported by a thinner and more heavily doped drift region, which leads to a substantial reduction in the on-state resistance. Unfortunately, the field plate as an extension of the gate electrode leads to a significant increase of the gate-drain capacitance $C_{GD}$ (hence also $Q_{GD}$ and $Q_G$) and a nonlinear dependence on the drain voltage.

Isolating the field plate from the gate and instead connecting it to the source (Fig. 1d) resolves these issues. While the charge compensation principle operates as before, the now buried field plate does not introduce any additional contributions to the gate-drain capacitance. Instead, the field plate shields the gate electrode from the drain potential, which reduces the gate-drain capacitance $C_{GD}$ and related charges. At the time of their introduction, these devices delivered best-in-class performance [6]. While the presence of the field plate comes with the disadvantage of an increased output capacitance $C_{OSS}$ and output charge $Q_{OSS}$ (a consequence of the lateral charge-compensation), a careful device optimization enabled field plate-based power technologies with $FOM_{OSS} = R_{DS(on)} \times Q_{OSS}$ comparable to those of the standard trench MOSFET [7],[8].

## II. Novel Device Concept

### A. Device structure

New MOSFET devices are required to provide improvements across all figures of merit. To meet these requirements, a novel cell-design approach is developed, which explores a true three-dimensional charge compensation. Today's state-of-the-art MOSFET technologies use an insulated deep field plate underneath and separated from the gate electrode and employ a stripe layout as depicted in Fig. 2. The new generation separates the field plate trench, which is now formed with a needle-like structure, from a grid-like gate trench that surrounds the needles [9], as shown in. Fig. 3. This increases the silicon area available for current conduction, allowing for a further reduction in the overall on-resistance [9]. In order to further reduce the $FOM_G = R_{DS(on)} \times Q_G$ and $FOM_{GD} = R_{DS(on)} \times Q_{GD}$ values, the gate trench underwent a complete redesign to minimize its lateral extension.

### B. Distributed gate resistance

The substantially smaller dimensions of the gate impose a new challenge, as the use of polysilicon as gate material would result in unacceptably large internal gate resistances. The introduction of gate fingers usually addresses this issue, but significantly reduces the active area available for current conduction as shown in Fig. 4. The introduction of a metal gate system, which is a novelty for a trench power MOSFET, clearly reduces the internal gate resistance, but also significantly improves the gate resistance uniformity over the chip [9]. Fig. 5 illustrates the improved homogeneity of the new gate design approach with a comparison of the distributed

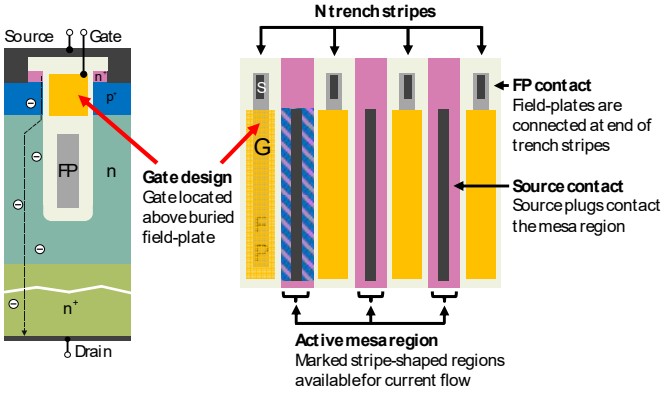


Fig. 2: Typical Trench MOSFET structure with lateral charge-compensation by an insulated field plate connected to source (left) and commonly employed stripe layout approach in the chip design (right)

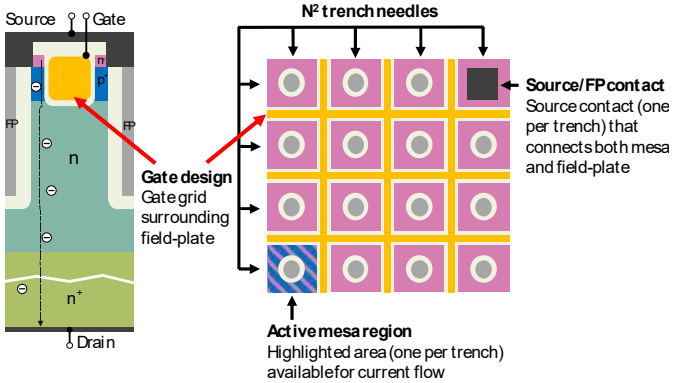


Fig. 3: Trench MOSFET structure with lateral charge-compensation by an insulated field plate and separated gate trench (left) and the new grid-like layout approach in the improved chip design (right)

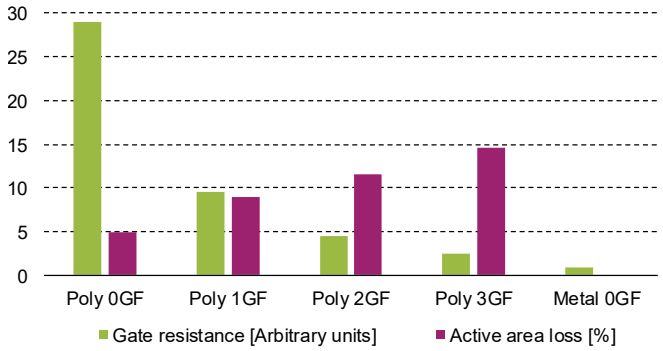


Fig. 4: Gate resistance and active area loss depending on the number of gate fingers (GF) for a best-in-class chip in a PQFN 3.3 x 3.3 mm² package [9]

gate resistance for BiC PQFN 5x6 mm² devices. In the case of the stripe design, the local gate resistance rises along the length of the stripe, with the lowest values at the gate runners and the gate pad. The use of a combination of a metal gate and a gate grid results in a much more even distribution of the gate resistance across the chip, supporting faster switching of the device. This strongly improved homogeneity is also advantageous for device robustness, for example avalanche ruggedness, by reducing the probability that a part of the chip is affected by gate signal delays [10] or parasitic turn-on. In former transistor generations, both gate signal delay and parasitic turn-on degrade the device ruggedness as power dissipation is limited to just a part of the chip.

This device setup is mandatory for telecom, server and data center switched-mode power supplies (SMPS) which use switching frequencies in the range from 100 kHz to 800 kHz. However, the 200 V voltage node mainly targets battery power and motor drive applications, such as light-electric vehicles (LEVs) and forklifts. Here the switching transients are slower due to heavy parallelization, and the requirements on the gate resistance values are less challenging with values of 2-3 Ω. This can still be achieved by using a standard polysilicon gate.

### *C. Distributed field plate resistance*

Fig. 6 compares the distribution of the field plate resistance across the chip. The previous generation device with a stripe layout shows an increase of the local resistance with increasing distance from the source runner in the center of the chip. In contrast, the field plate resistance distribution for the new device is completely flat, as the trench electrodes acting as field plates connect directly to the source metal. Thanks to this, the chip is expected to switch extremely homogeneously, supporting fast transitions between the on- and off-state and vice versa. It is further beneficial for achieving a high avalanche ruggedness, as an increased local field-plate potential may alter the local breakdown voltage [11] and can lead to an inhomogeneous power dissipation over the chip area. In addition, the direct connection between the source and

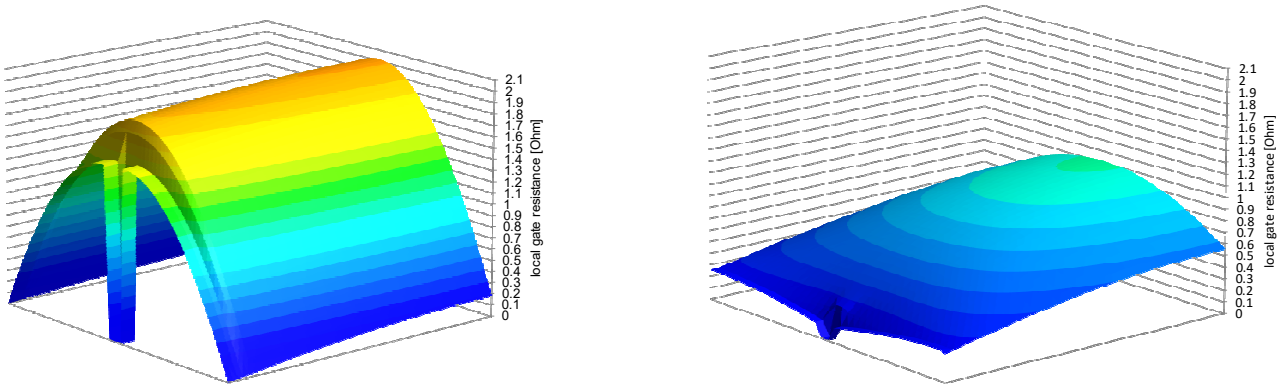


Fig. 5: Distributed gate resistance for a common stripe design (left) and the new grid-like design (right)

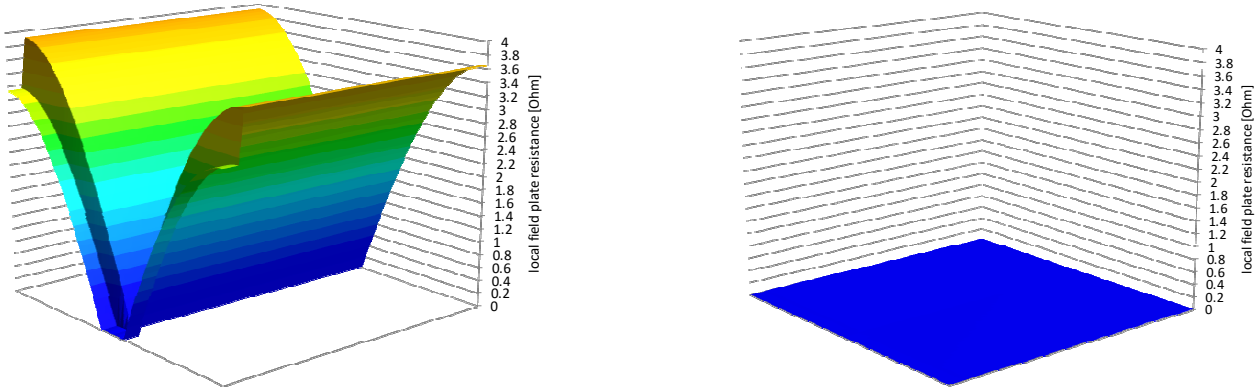


Fig. 6: Distributed field plate resistance for a common stripe design (left) and the new grid-like design (right)

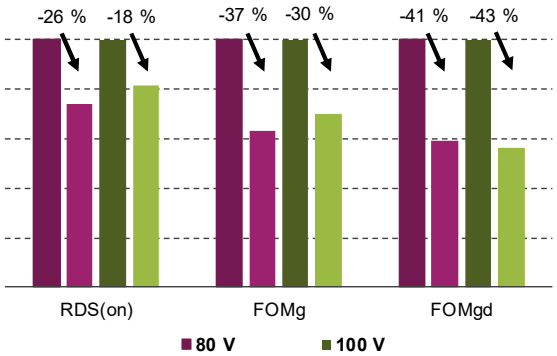


Fig. 7: Improvement in device performance for best-in-class 80 V and 100 V devices in PQFN 5x6 package

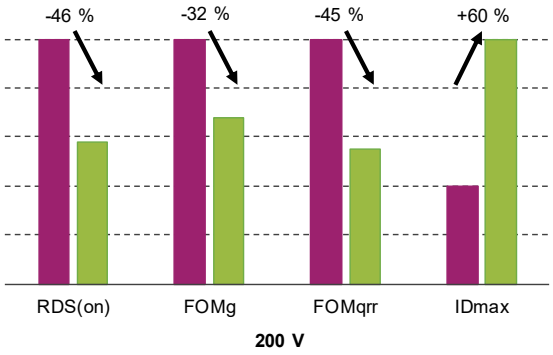


Fig. 8: Improvement in device performance for best-in-class 200 V devices in TO-263 ($D^2PAK$) package

the field plate practically eliminates any resistance in series with the output capacitance, which minimizes conduction losses during charging and discharging of the output capacitance [12],[13].

### *D. Improvements in device parameters*

Fig. 7 summarizes the achieved device parameter improvements for the 80 V and 100 V technologies, indicating impressive improvements in all of the relevant parameters over the predecessor technology generation. The innovative gate trench engineering of the new device results in a remarkable reduction of both gate-source and gate-drain specific capacitances, which is reflected in the respective figures-of-merit $FOM_G$ and $FOM_{GD}$. The $FOM_G$ reduction helps to achieve better efficiencies, especially at light load conditions, due to the reduced driving losses. This is very important for an SMPS operated at high switching frequencies, as well as in applications where a large number of MOSFETs are paralleled. In this case, the low gate charge also relaxes the requirements on the gate driver's current capability. In addition, the low $Q_{GD}$ enables fast switching transients, lowering the switching losses.

Fig. 8 summarizes the realized parameter improvements for the new 200 V technology based on the introduced grid-like layout with trench needles. Here, it was especially important to further reduce the reverse-recovery charge with respect to the previous technology generation with a fast diode [14]. This is not only important for a further reduction of switching losses, but also improves the EMI behavior and ensures a high commutation ruggedness [15]. Thanks to the new advanced cell design, the on-resistance of the device is heavily lowered, allowing the device to conduct a much higher current in the same package footprint.

### *E. Summary of the achieved device improvements*

Overall, the use of a gate grid, a metal gate electrode where needed and the direct connection of the field plates to the source metal realizes a very attractive device setup. This new device structure not only ensures a very fast and homogeneous transition at turn-on and turn-off to minimize switching losses, but also reduces the risk of an unwanted, dv/dt induced parasitic turn-on of the MOSFET.

## III. Performance In Resonant Operation

### *A. Introduction of the test plattform*

The test platform is represented by a 1 kW open-loop LLC DC-DC intermediate bus converter (IBC) [16]. Fig. 9 depicts the basic schematic. The platform serves to study the performance of the new devices in the 80 V class. Fig. 10 gives a view of the board in a standard quarter-brick form factor. The IBC operates as a DC transformer from an input which may vary from 42 V to 60 V. The turns ratio of the transformer is 4:1. The resonant frequency of the LLC converter is 310 kHz. The switching frequency is fixed, so that the converter operates at resonance over the whole input voltage and load range. ZVS for the primary-switches and ZVS / ZCS for the SR switches are achieved by design.

Two 80 V MOSFETs BSC030N08NS5 of the predecessor generation OptiMOS™ 5 in PQFN 5x6 $mm^2$ package with $R_{DS(on),max}$ = 3 mΩ are paralleled on the primary-side full-bridge (marked in yellow), while four IQE006NE2LM5 25 V, PQFN 3.3x3.3 $mm^2$ source-down devices are used in parallel on the secondary-side arranged in a full-bridge configuration.

The significantly improved device parameters of the new technology generation allow the replacement of the originally two paralleled MOSFETs of the predecessor generation on the primary side by just one new generation OptiMOS™ 6 device ISC014N08NM6 with half the $R_{DS(on),max}$ of 1.45 mΩ. The use

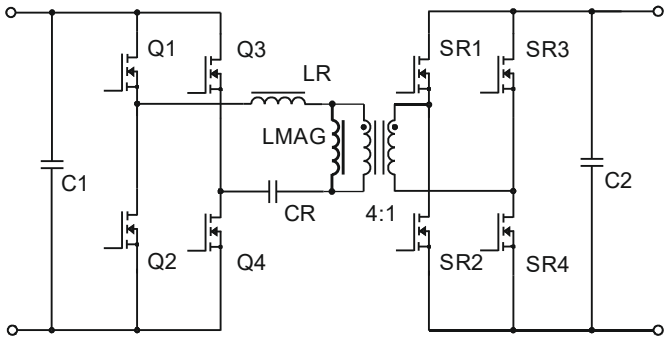


Fig. 9: Schematic of the LLC converter

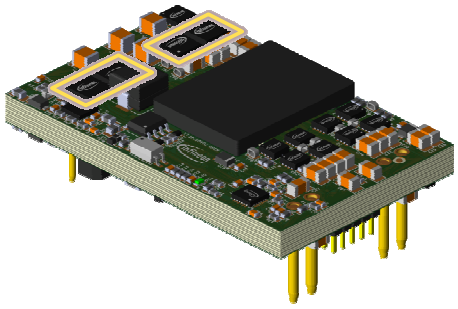

Fig. 10: View of the 1 kW LLC DC-DC board. The primary side MOSFET (DUT) are marked by the yellow rectangle

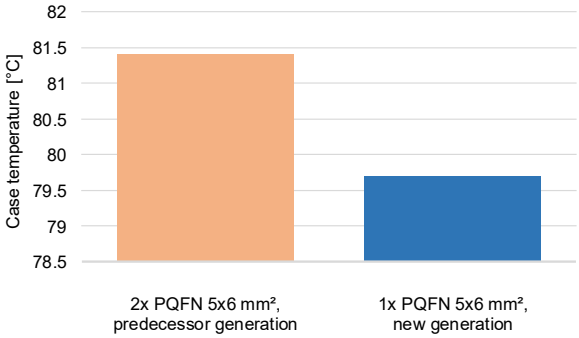


Fig. 12: Comparison of the case temperature at maximum output current

of different device generations on the primary-side calls for the use of different dead-times. For running comparable tests, the dead-times are adjusted to keep the effective body diode conduction time the same for both devices under investigation.

### *B. Test results in 1 kW IBC for data center*

Fig. 11 compares the efficiency, with up to 0.8 % better values for the new technology. Fig. 12 even indicates a lower package temperature for the usage of a single die of the new generation compared to the two from the previous one [13].

The LLC topology targets to achieve soft switching (either at zero-voltage or at zero-current) for all MOSFETs, meaning that the switching losses are assumed to be negligible. The relevant losses that need to be considered are the conduction and the gate-drive losses. The impressive efficiency improvement found with the new device generation therefore largely results from the dramatically lowered gate and gate-drain charge, together with the strongly improved switching homogeneity across the chip area.

In addition, there is another loss mechanism contributed by the power device itself, which is often neglected. It relates to the field plate resistance $R_{OSS}$ that is in series with the field-plate capacitance $C_{OSS}$. Every time $C_{OSS}$ is either charged or discharged, a large portion of the magnetizing current must pass through $R_{OSS}$. This current flow causes conduction losses, which depend on the device setup. It is evident that the $R_{OSS}$ can become significant for a MOSFET with a common stripe layout as shown in Fig. 2, as the field plates can only be connected with the source at the end of the trench stripes. This is completely different for the new MOSFET technology. Here each field-plate directly connects to the source metal, as can be seen in Fig. 3, which almost eliminates $R_{OSS}$ [13].

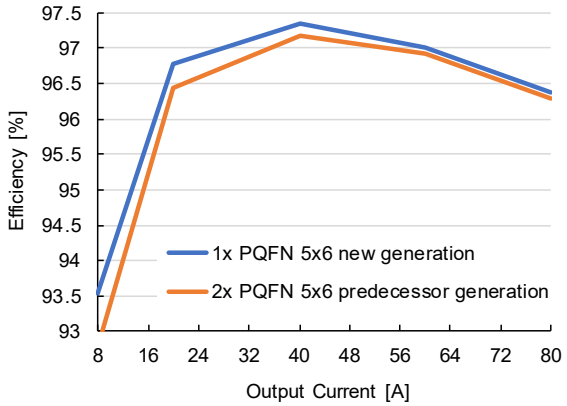


Fig. 11: Comparison of gained efficiency in the LLC ($V_{IN}$ = 54 V) [13]

## IV. Performance In Motor Drives

### *A. Introduction of the test platform*

This application compares the performance of the latest 200 V technology with that of its predecessor [14] under hard switching conditions in a motor drives application. The modified commercially available inverter employs a common B6 topology as depicted in Fig. 13, with a nominal input voltage of 144 V, an average current output of 135 Arms and a 1-minute phase RMS output current of 500 Arms. The inverter is sized to drive a 65 kW AC induction motor. The power board contains overall 96 MOSFETs, with 16 devices paralleled in each leg. The use of an insulated metal substrate power base provides superior heat transfer for increased reliability and performance. All tests are performed at a switching frequency of 10 kHz, with a dead time of approximately 1 µs. Fig. 14 illustrates the general functional block diagram of the test environment.

The inverter uses devices in standard TO-263-3 packages, making it relatively easy to desolder the original devices and to replace them by the devices of interest. The investigation presented in this work focusses on the comparison of the new OptiMOS™ 6 200 V devices with its direct predecessor technology. The comparison uses best-in-class devices, where

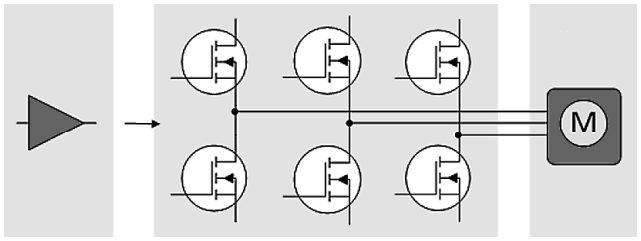


Fig. 13: Basic schematic of the B6 inverter

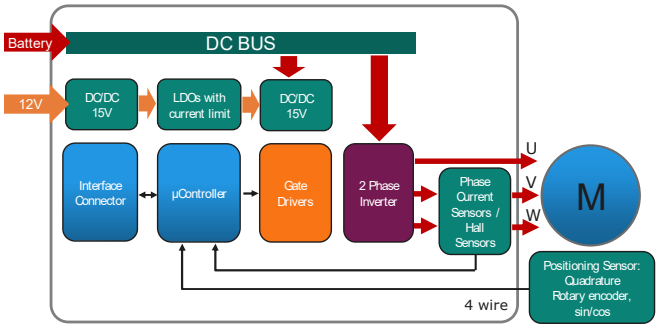


Fig. 14: General functional block diagram

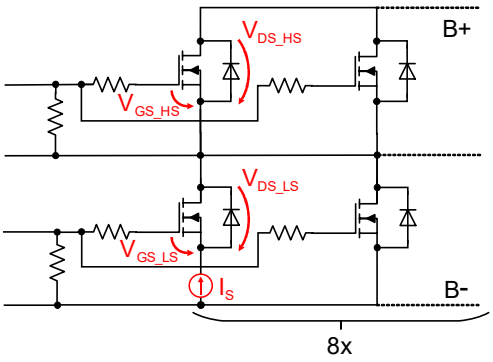


Fig. 16: Indication of test points for the waveform measurements

the new OptiMOS™ 6 devices come with an on-resistance of 6.8 mΩ, while the predecessor OptiMOS™ 3 devices own an on-resistance of 11.7 mΩ.

In the presented measurements, the motor was running in a load condition with a phase current of 160 Arms. To enable the loss calculations, the measured values, among others, include low-side MOSFET current, high- and low-side drain-to-source and gate-to-source voltages and the phase current. All measurements extended over one complete electrical period of the motor.

*B. Test results in the motor drives inverter*

The first investigation determined the mean losses per MOSFET. The results are shown in Fig. 15. The comparison includes the overall mean losses per MOSFET as well as the separate conduction, turn-on and turn-off losses. The overall loss reduction accounts for remarkable 36 %. It is also worth to mention that the new OptiMOS™ 6 200 V devices achieve a reduction in any of the loss contributors.

Beside a reduction of the losses, it is important that the devices provide a clean switching behavior. Switching waveforms are measured at a single MOSFET. Fig. 16 gives an overview on the investigated device parameters, and at which positions of the circuitry these values get measured. All gate-to-source and drain-to-source voltages are calculated from two separate measurements, taken from the respective electrode to ground. The current through the MOSFET is measured by a Rogowski coil at the source of a low-side device. Fig. 17 shows the switching waveforms of the new generation devices when the high-side switch is turned-on. Fig. 18 depicts the transients for the turn-off of the high-side switch, with the low-side MOSFET operating in synchronous rectification mode. In both cases, the use of the OptiMOS™ 6 devices result in clean waveforms. There is no visible ringing, and the slew rates are rather linear which is advantageous for the EMI behavior.

This implies that the significantly improved device performance does not degrade the EMI behavior. Indeed this

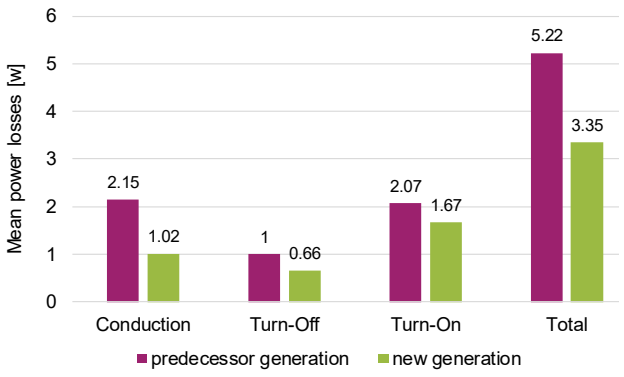


Fig. 15: Comparison of mean power losses per MOSFET

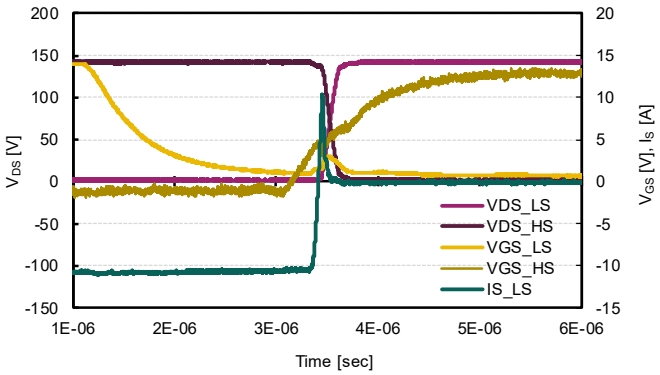


Fig. 17: New device switching waveforms at turn-on of the high-side switch

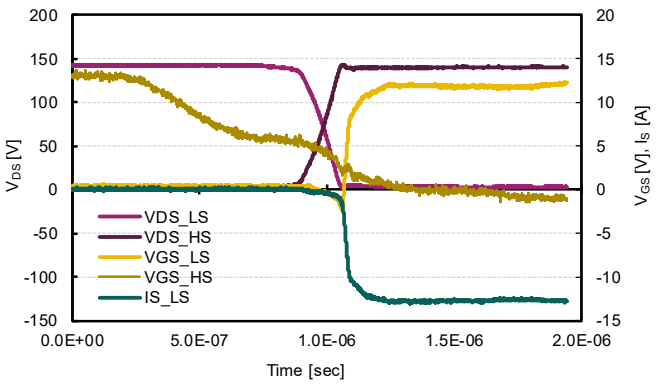


Fig. 18: New device switching waveforms at turn-off of the high-side switch

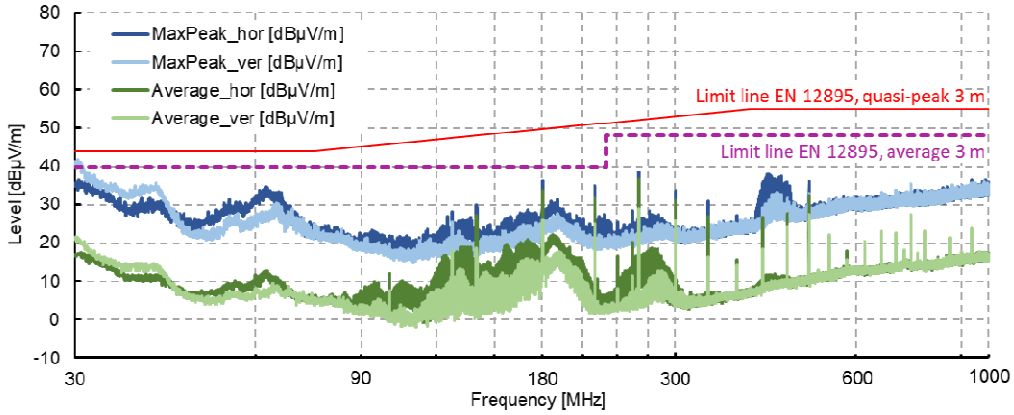


Fig. 19: Measurement of radiated emission in the application using the predecessor device generation

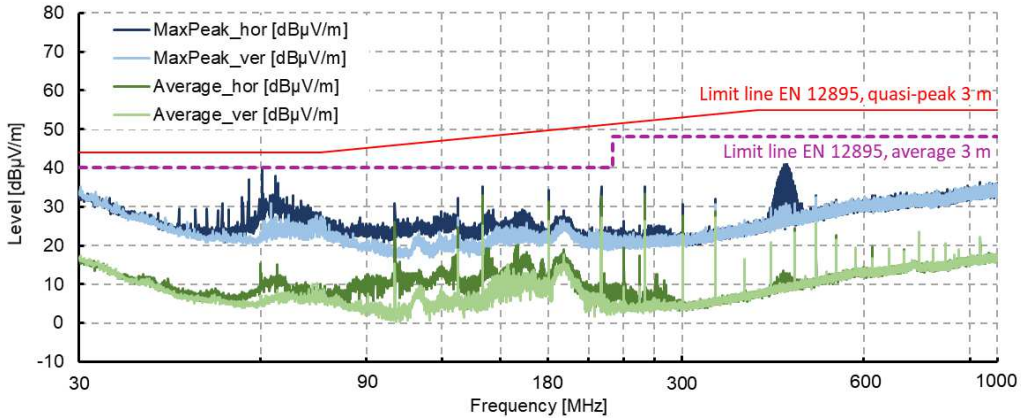


Fig. 20: Measurement of radiated emission in the application using the new device generation

is confirmed by the comparison of the radiated emission between the two technology generations, as shown in Fig. 19 and Fig. 20. The radiated emission measurements were done in accordance with the applicable standard EN 12895.

## V. Conclusion

This work introduces our latest power MOSFET technology family that delivers improvements in all important device parameters and combines the benefits of low on-state resistance with a superior switching performance.

The remarkable progress in the overall device performance is enabled by substantial improvements at the device technology level. This has culminated in a unique device structure, which is the first to employ three-dimensional charge compensation combined with a gate grid and the first ever use of a metal gate in a trench power MOSFET (if it is needed by the application). The new design provides a so-far unmatched homogeneity of the gate and field plate resistance across the chip. The reduction achieved in the on-resistance, dramatically lowered total gate charge, the low gate-drain charge together with a low output charge and the improved switching homogeneity across the device area, enhance the system efficiency in the tested applications across all load conditions. The new device structure is also beneficial for the internal body diode of the MOSFET. Because the silicon area conducting current is increased, the body diode current density is decreased, which for the same current level means a decreased reverse recovery charge.

Resonant applications like the LLC converter especially benefit from the improved device characteristics. Here the losses due to the stored charge in the output capacitance of the power semiconductors are largely avoided, as this charge swings from one MOSFET to the other. This swing current is linked to conduction losses due to the PCB tracks, the transformer windings and the internal series resistance $R_{OSS}$ connected to the output capacitance $C_{OSS}$ of the device structure; however this series resistance $R_{OSS}$ is effectively eliminated with the new technology.

Also motor drive applications benefit immensely from the new technology, as both conduction and switching losses reduce. The devices can easily be massively paralleled, achieving clean switching waveforms. The good switching properties are also confirmed by radiated emission measurements, which stay well within the required limits.

The significantly improved device performance even allows a reduction of up to half the number of paralleled

devices required (depending on the application), or alternatively the use of smaller footprints, without having a negative impact on the temperature of the devices. This not only provides an advantage in terms of bill-of-materials (BOM) costs, but also the chance to save real space on the PCB. This opens the door for a further optimization at the system design level, which is expected to further boost efficiency, reduce the converter or inverter size and increase the power density.

## ACKNOWLEDGMENT

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