Application-tailored development of Power MOSFET

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Abstract

Low-voltage power MOSFETs based on charge-compensation using a field-plate offer a significant reduction of the area-specific on-resistance. Beside a further improvement of this key parameter, the new device generation takes an in-depth focus on the other device parameters which areessential to the targeted application fields. The paper discusses how the most important of these often conflicting requirements were identified. It is shown that beside the device technology the package contributes significantly to the overall device performance.

Keywords: synchronous rectification, motor drive application, package contribution, overall efficiency

INTRODUCTION

In previous work the optimization of modern power MOSFET technologies with the focus on synchronous rectification was discussed based on a detailed analysis of the loss mechanism [1-3]. To improve the overall efficiency, both on-resistance and switching losses need to be minimized at the same time in order to meet the efficiency targets at low and medium load conditions. It was shown that those targets can be reached by the use of improved manufacturing setups linked to better process control capabilities, in combination with an optimized cell structure leading to an increase of the overall efficiency level, while at the same time reducing the voltage overshoot. These improvements did not compromise the single-pulse avalanche capability of the device, and no significant shift in the device performance was found in the case of repetitive avalanche events [3].

APPLICATION REQUIREMENTS

Addressing a wide range of voltage classes from 60 V to 100 V is linked with targeting a significantly wider range of application fields. To offer a solution capable of delivering the best performance for as many of them as possible, one needs to identify the device properties which are beneficial for all applications, in order to focus on the optimization of the right device features. An in-depth analysis of the application requirements also allows a ranking of the different device properties in order of their importance. Ideally this procedure also identifies the essential parameters which need to be optimized in opposing directions for different applications, thereby indicating opportunities or requirements to establish technology derivatives. Established methodologies for such an analysis are offered in general by the Quality Function Deployment [4,5]. Within our work, the House-of-Quality Matrix was employed as an aid in determining how products live up to customer needs [6]. Fig. 1 illustrates the basic worksheet used in this process for analyzing the relationship between customer wishes and product capabilities and their interactions, identifying development priorities and including a bench-marking of the new concepts against predecessor products and the competition in the market. As the required inputs are

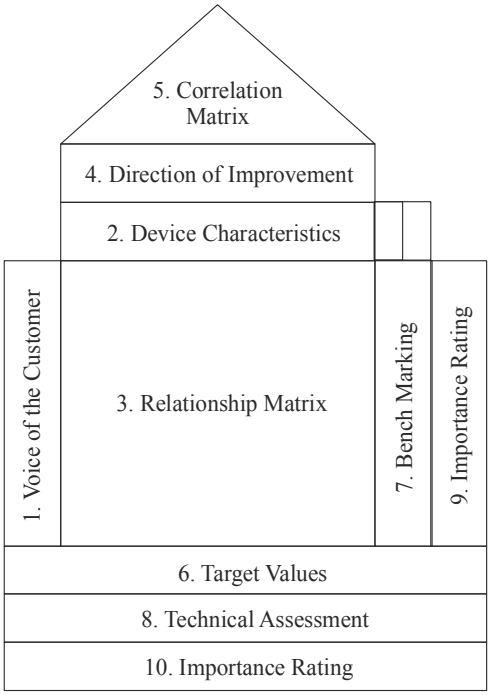

Fig. 1: House-of-Quality matrix used for concept evaluation

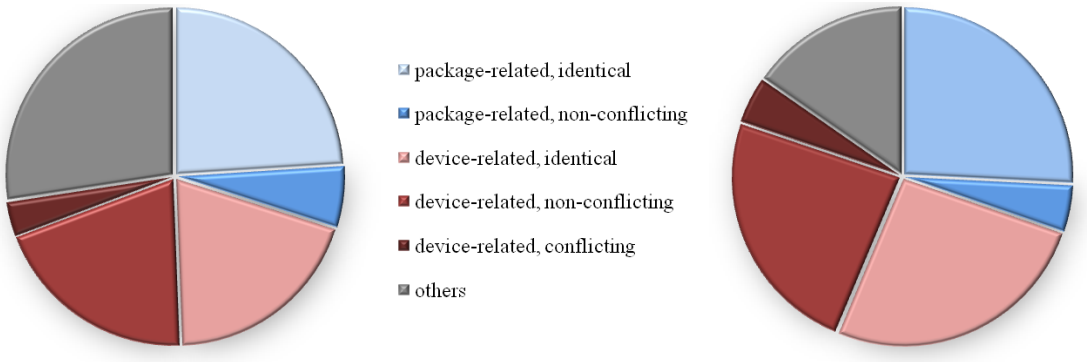

Fig. 2: Requirements for synchronous rectification and primary-side switch applications (left) and motor drive applications (right)

delivered from different functional units such as marketing, engineering and manufacturing, the methodology also increases the cross-functional integration within the organization.

Fig. 2 presents the summary out of this investigation for initially three application fields. Synchronous rectification and primary side switches turned-out to have so many requirements in common that these two form one group, the second group being motor drive applications. In total, almost 30 parameters were evaluated against the identified application requirements and their interactions. Fewer than half of those parameters proved to have an influence significant enough to take account of them in the optimization process. Here, two main groups of parameters are identified – parameters related to the device package and parameters related to the electrical characteristics of the chip itself. It was found that most of the significant parameters such as low on-resistance, reduced gate- and output charge, small parameter tolerances or low thermal resistance, are of equal importance for both application groups. One parameter causes a conflict, meaning that there are opposing optimization targets. Unsurprisingly this parameter is related to the common need of paralleling devices in typical drive applications to meet the load current requirements. Paralleling of devices calls for the ability to switch all of them at the same time, which is usually linked to longer switching times in order to balance inevitable device tolerances. On the other hand switching frequencies are typically lower than in the case of synchronous rectifiers and primary-side switches. Consequently, devices for drive applications may also have larger Miller and input capacitances in addition to a low variation of the threshold voltage in order to ease the task of paralleling. It is important that the di/dt and dv/dt can be controlled over a wide range by chosing an adequate external gate resistance, as this could avoid the need for a derivative with increased capacitances.

The first conclusion out of this analysis is that just one technology needs to be developed since it is relatively easy to adapt it later to get a derivate for the other field of application. The second conclusion underlines the need for further improved package technologies. Here, the most important requirements are a further reduction of the package contribution to the overall on-resistance of the product and improved cooling capabilities (lower R_{thJC}). However, it is not only the package contribution to the on-resistance of the device that matters, but also the parasitic inductance which it introduces. The inductance due to the package leads to additional switching losses, slower switching speed, or may even cause an unwanted turn-on of the device, all lowering the overall efficiency of the power-electronic device.

DEVICE PROPERTIES

The device concept discussed is related to a field-plate trench MOSFET as shown schematically in Fig. 3. Such devices entered the market more than 10 years ago and developed into a kind of standard technology for fast-switching devices. The basics and properties of these devices have been discussed in many publications over the years [7-11]. The application of a field-plate leads to an almost constant field distribution in the vertical direction since the ionized dopants in the drift region are laterally compensated by mobile carriers in the field-

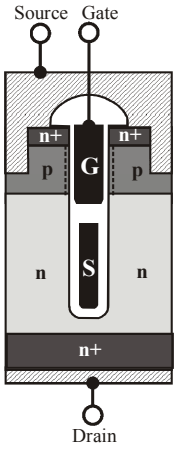

Fig. 3: General structure of a field-plate MOSFET

plate, thereby reducing the necessary drift region length and increasing the allowed drift region doping for a given breakdown voltage. Both contribute to the significantly reduced area-specific on-resistance. Since the field-plate electrode is connected to the source electrode of the MOSFET and the gate is formed by a separate electrode, such a device offers an outstanding area-specific on-resistance and a low gate-charge at the same time.
In previous work the basic technological assumptions and ideas which enabled the new device generation were described [2,3]. Limited at that time to the 60 V class, the device familyhas since been extended towards higher voltage classes, following the same cell optimization approaches to take further advantage of the significantly improved manufacturing setups. These new voltage classes of 80 V and 100 V offer a greatly reduced on-resistance $R_{DS(ON)}$ together with improved Figures-of-Merit FOM_{OSS}, FOM_G and FOM_{GD} , while maintaining a good avalanche capability and device ruggedness. As paralleling turned-out to be controllable, no derivative technology has been introduced so far. Work is ongoing here to verify further advantages of such a derivate.

PACKAGING ISSUES

With silicon technology moving rapidly forward the package becomes an increasingly important part for low-voltage MOSFETs. The on-resistance of the latest device technologies has become remarkably low; the package proportion of the overall on-resistance has changed from a negligible 1:10 to 1:1 or even worse. In the past this need for low-ohmic packages to avoid a limitation of the device by the package characteristics drove the development of new packages, optimized for high currents and high switching frequencies. This becomes clear when referring to the package contributions of the discussed low-voltage MOSFET devices with maximum die-size for the given package in Fig. 4. These advanced device technologies allow for MOSFET dies in a still widely used TO-220 with an on-resistance being equal to or lower than the package resistance. Therefore, the package resistance clearly limits the minimum achievable on-resistance. To follow the route towards denser and more efficient power converter designs, available surface-mounted package types, such as the new TO-Leadless (TO-LL), the SuperSO8, the Shrinked SuperSO8 (S3O8) or the CanPAK™, are needed to replace the leaded SMD or through-hole devices for low-voltage MOSFETs.

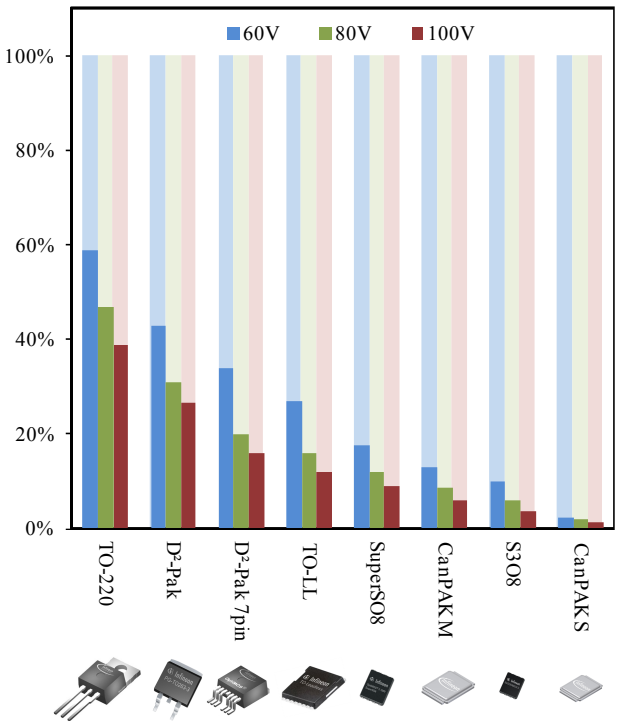

Fig. 4: Package contribution to the overall device resistance for devices with maximum die-size in the respective package

Of course it is not only the package contribution to the on-resistance of the device which matters, but also the parasitic inductance it introduces. At increasing switching frequencies and switching speeds, the package inductance can play a major part in loss generation for the overall device and application performance. For example, a buck-converter with an output current of 30 A, operating at 250 kHz, generates 0.7 W of losses in a D-PAK design due to the total package inductance of 6 nH. With a low-inductive package like the SuperSO8, showing an inductance of less than 0.5 nH, the losses drop below 0.1 W.
However, most surface-mounted devices available so far were less suited for high-current applications due to their limited footprint area and the corresponding limited current-density due to the package itself. A recent solution addressing such applications is the new TO-Leadless (TO-LL), which offers a lower parasitic resistance and inductance, a lower thermal resistance and a higher current capability [12]. This solution also extends the maximum allowed current capability of the commonly available TO-packages such as TO-220 or D²PAK 7-pin up to 300 A, as it offers a 50 % bigger solder contact area. This reduces the current densitiy through the solder contact areas and thus avoids electromigration issues at high current levels.

DEVICE PERFORMANCE

Efficiency and voltage overshoot

Improvements of the MOSFET die itself are mainly based on a detailed understanding of the device physics

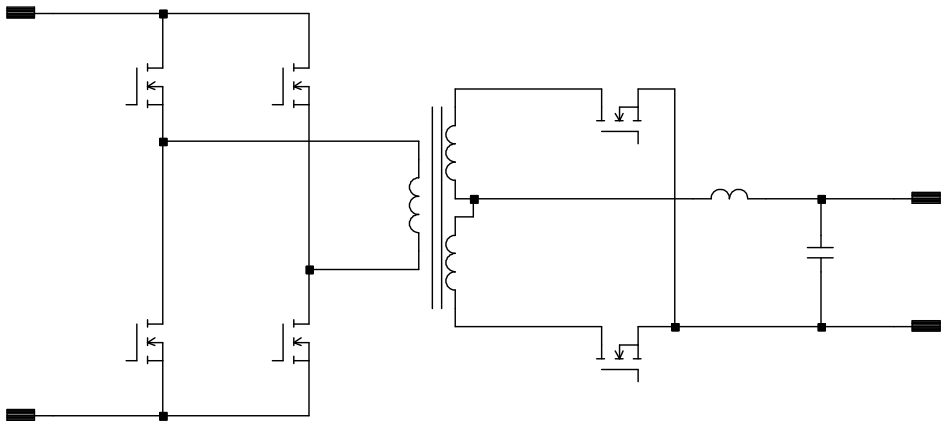

Fig. 5: Simplified schematic of a 400 W / 33 A PSU using a full-bridge converter on the primary side and full wave synchronous rectification.

and consequent improvement of manufacturing capabilities as discussed in detail before [3]. The improvements realized by the new 2nd generation OptiMOS 80 V and OptiMOS 100 V MOSFETs over the equivalent 1st generation products were investigated in a 400 W Power Supply (PSU) based on a full-bridge converter with full wave synchronous rectification, as schematically shown in Fig. 5. For the efficiency evaluation, the synchronous rectifier stage was equipped with either 80 V or 100 V devices:

- for 80 V: one 1st generation / 4.7 mΩ or one 2nd generation / 3 mΩ device.
- for 100 V: two paralleled 1st generation / 4.6 mΩ or two paralleled 2nd generation / 4 mΩ devices.

Fig. 6 compares the measured efficiency over the full load range of the PSU equipped with 1st generation or 2nd generation devices in the synchronous rectifier stage.

Fig. 7 indicates the voltage overshoot at the synchronous rectification switches for the example of the 100 V devices at low load. While the on-resistance of the 2nd generation device is much lower, resulting in the better high-load efficiency, the efficiency at low and medium load conditions is also maintained due to the improved FOM_{OSS}. By chosing the right on-resistance of the device, efficiency can be easily improved over the full load range. Also the voltage spikes are lowered despite the higher degree of charge-compensation responsible for the lower on-resistance.

The lower overall losses translate into a lower device temperature as shown in Fig. 8. As different color scales are used, the maximum temperature of the devices is indicated on the graphs.

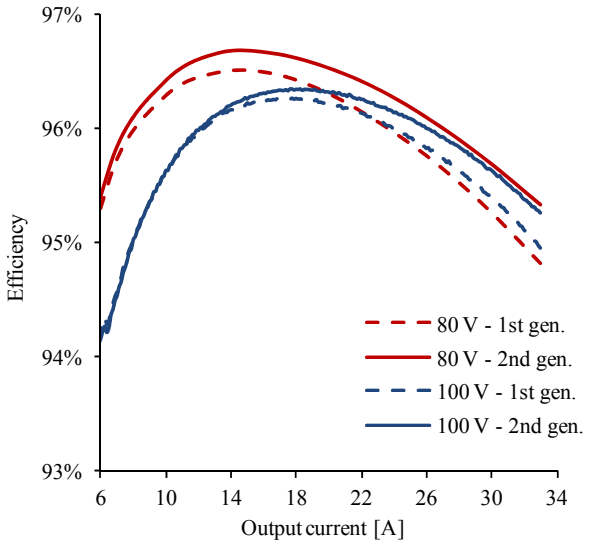

Fig. 6: Comparison of the overall efficiency at different load conditions and an input voltage of 48 V

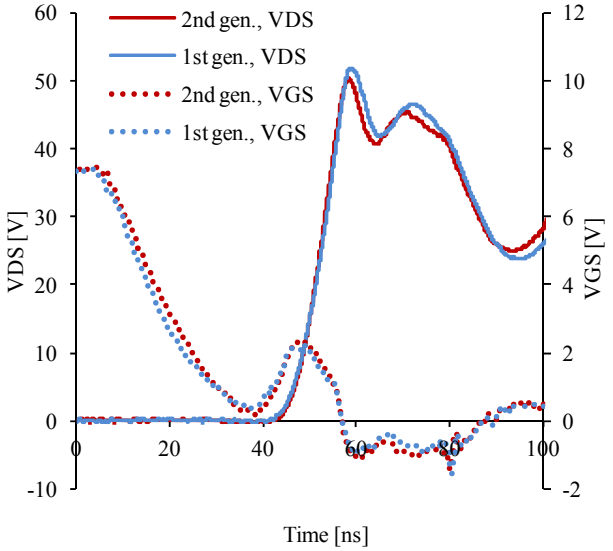

Fig. 7: Comparison of voltage overshoot at the secondary rectification stage of a PSU equipped with OptiMOS 100 V devices of the 1st device generation or the new 2nd generation at a load current of 8 A

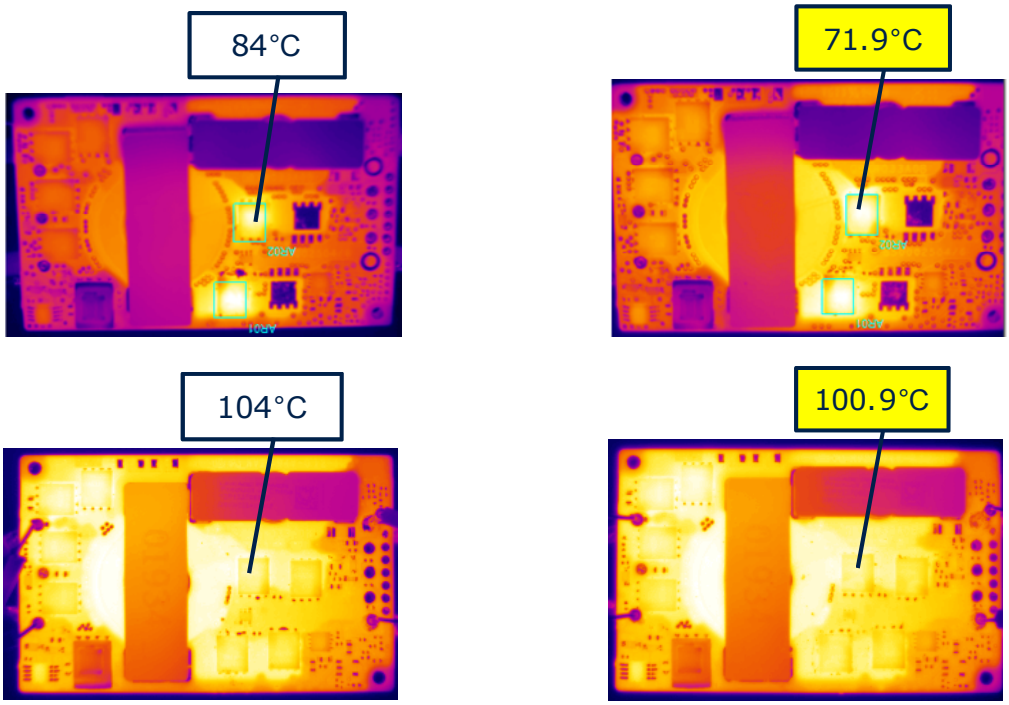

Fig. 8: Maximum chip temperature for 80 V devices (top) and 100 V devices (bottom) in synchronous rectifier stage, each for 1st generation device (left) and 2nd generation device (right) [V_{IN} = 48 V, I_{OUT} = 33 A]

Performance of TO-LL package

As previously discussed, advanced package concepts enable a significant reduction of the package contribution to the overall on-resistance of a device. How big this difference can be is shown in a direct comparison between a D^2PAK 7 pin and a TO-LL, both with identical chip size. A typical application for such low ohmic MOSFETs in a high current package is the inverter for an electric 3-phase motor. Starting with a few tenths of an Ampere, the continuous current easily reaches several hundred Amperes or more. A typical battery voltage is 24 V, therefore 60 V MOSFETs are an appropriate choice. The lowest available on-resistance of such a device in D^2PAK 7 Pin is 1 mΩ. This is the upper guaranted limit, including both silicon and package resistance. The package (= "copper") losses are already around 0.4 mΩ, representing nearly 50 % of the conduction losses. A better solution would be a package with an improved design for lower copper losses. In TO-LL with its optimized electrical and mechanical design, the package resistance goes down to ca. 0.25 mΩ. This enables a 60 V MOSFET with a maximum on-resistance of less than 0.75 mΩ. The reduction of package resistance results in dramatically lower losses, enabling, for example,. the chip temperature to be kept lower. Fig. 9 shows the chip temperature in a typical motor control application (3-phase 24 V motor system, I_{RMS} = 100 A) for both packages, D^2PAK 7 Pin and TO-Leadless (identical chip size). After one hour the temperature difference is already around 10 K. As a consequence the temperature stress to the TO-LL parts is much lower, leading to an increased reliability of the parts linked to less failures in the field and as such longer expected lifetimes.

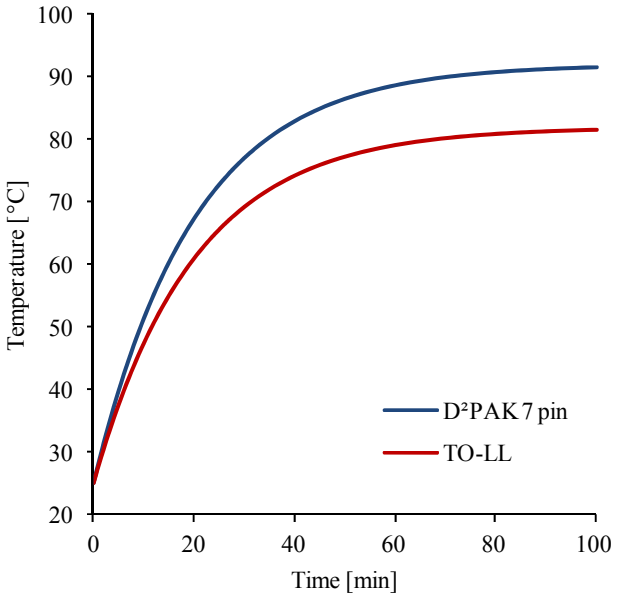

Fig. 9: Evolution of chip temperature with time for 60 V MOSFET in a typical drives application for devices with identical chip area in two different package types

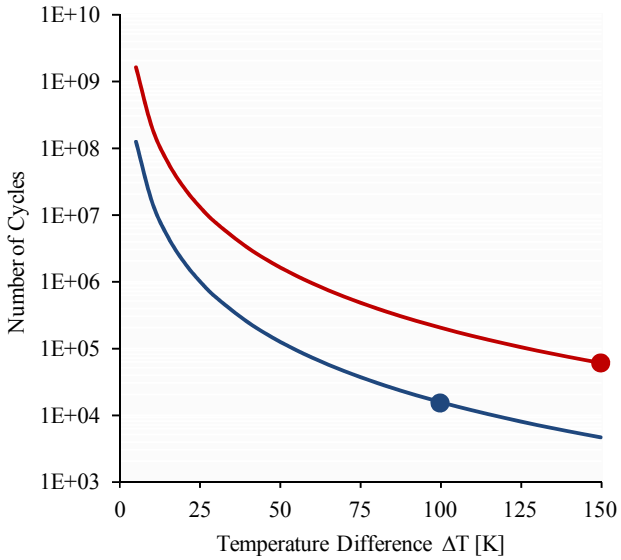

Fig. 10: Power cycling of MOSFET.
red line: calculated number of cycles over temperature rise, derived from the measurement conditions (ΔT=150K, red dot).
blue line: requirements according to AEC Q101 standard, derived from cycles with ΔT=100K (blue dot)

Using Intermittent Operating Lifetime tests (IOL), also called „Power Cycling“, the reliability of the devices in the new TO-LL package was proven. In this test, the device is heated up by a high current flow in each cycle until the defined temperature difference is reached. The relevant industry standard AEC Q101 requires the device to survive a minimum of 15,000 cycles at a temperature difference of 100 K.
As a rule of thumb, each additional temperature increase by 10 K leads to a reduction of the expected lifetime by 50 % (= half the number of possible power cycles). In order to to reduce the test time (15,000 cycles last app. 1 month), the temperature difference was increased from 100 K to 150 K, applying a much higher stress to the MOSFET. 60,000 applied cycles using this dramatically higher stress condition did not result in any device failures or measurable parameter drifts. Fig. 10 shows the diagram including also the calculated curves for different temperature rises.

CONCLUSION

In this paper the extension of our latest power MOSFET technology to a higher voltage range based on a detailed requirements analysis methodology is described. The increasing importance of the package and its influence on the overall performance is discussed. Measurement results in the respective target applications indicate the achieved progress in the overall device performance, both from the device and the package point of view.

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