The new CoolSiC™ Trench MOSFET Technology for Low Gate Oxide Stress and High Performance

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Abstract

The paper describes a novel SiC trench MOSFET concept which is designed to balance low conduction losses with Si-IGBT like reliability. Basic features of the static and dynamic performance of the 45 mΩ / 1200 V CoolSiC™ MOSFET are presented. The favorable temperature behavior of the on-state and the low sensitivity of the switching energies to temperature make the device easy to use. The gate oxide is designed to fulfill requirements of industrial applications. Long term gate oxide tests reveal that the extrinsic failure rate can be confidentially predicted to be low enough for industrial applications.

1. Introduction

SiC MOSFETs based power switches for blocking voltages of 1200 V offer significant system advantages in terms of power density, efficiency and cooling effort due to their much lower switching losses compared to Si-IGBT and Si diodes. It was shown that the system costs of solar applications as well as the running costs of UPS systems can be drastically reduced [1]. In addition to these applications also electric vehicle drivetrain and industrial motor drives can exploit SiC MOSFETs for better efficiency, in particular in case of frequent operation under partial load conditions [2].

While switching performance as well as conduction behavior of the commercial available SiC devices is already quite encouraging, there are still concerns about the SiC MOSFET gate oxide reliability [3], in particular about the potential high failure rate as a consequence of the quite high gate oxide stress field of above 4 MV/cm [4]. However, SiC DMOS are typically designed with such high gate oxide fields or such thin gate oxides, respectively, in order to compensate for their low channel mobility. This issue can be overcome with the trench concept presented in this paper.

2. Cell Concept of the Device

The novel CoolSiC™ MOSFET uses a trench structure in order to achieve higher inversion channel mobility with respect to a planar channel which is aligned to the Si face. An investigation of different orientations of the trench sidewalls resulted in slightly different threshold voltages as well as significantly different channel mobility as shown in [5]. The reason for this phenomenon is attributed to the dependency of the density of interface states to the crystal orientation of the MOS system. In addition, an off-orientation of the 4H-SiC substrate of 4° is necessary to ease the epitaxial growth process on 4H-SiC substrates. As a consequence, most of the practicable options to align the MOS channel on a trench sidewall are off-oriented with respect to the crystal orientation.

In our device the most favorable orientation was chosen for the MOS channel. Fig. 1 shows a sketch of the CoolSiC™ MOSFET cell which is arranged along stripes. Following the considerations presented before, the doped

regions adjoining the trench are asymmetric. The left hand side of the trench sidewall contains the MOS channel which is aligned to the a-plane in order to achieve optimum channel mobility. A large portion of the bottom of the trench is embedded into a p-type region which extends below the bottom of the trench. This p-type region has three main electrical functions:

i) connect the p-body region to the source electrode as low-resistive as possible,

ii) form an efficient p-type emitter to operate the body diode as rapid freewheeling diode and

iii) protect the gate oxide of the trench corner against a too high electric field induced by the drain bias.

This MOSFET structure inherently owns a favorable small ratio of the Miller capacity C_{GD} related to the gate source capacity C_{GS}. C_{GS} is comparably large since a large part of the trench contributes to it, i.e. the n^+-type areas on both sides of the trench and all p-type areas which are all connected to source. This allows for a well-controlled switching with very low dynamic losses [6]. In particular this feature is essential to suppress undesirable additional losses caused by a parasitic turn-on in topologies using half bridges.

The cell construction of Fig. 1 is also supportive to realize an adequate short circuit capability. The JFET region formed by the adjacent p-emitter regions is not only good to limit the oxide field in the trench corner but also lowers the saturation current of the device by adjusting the distance between the p-type regions. A smaller distance supports both a lower saturation current and lower field in the gate oxide of the trench corner but causes an additional contribution in the overall on-state resistance due to the JFET.

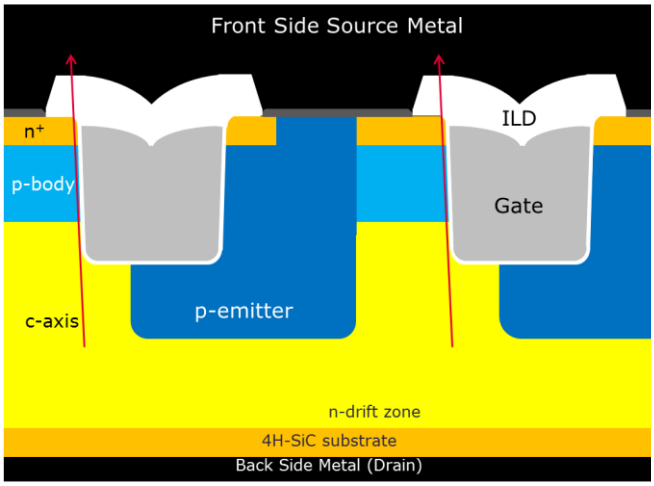

Fig. 1 Sketch of the CoolSiC™ Trench MOSFET cell. (Color code: grey/black = electrodes, blue = p-type, orange = n^+-type, yellow = n^--type)

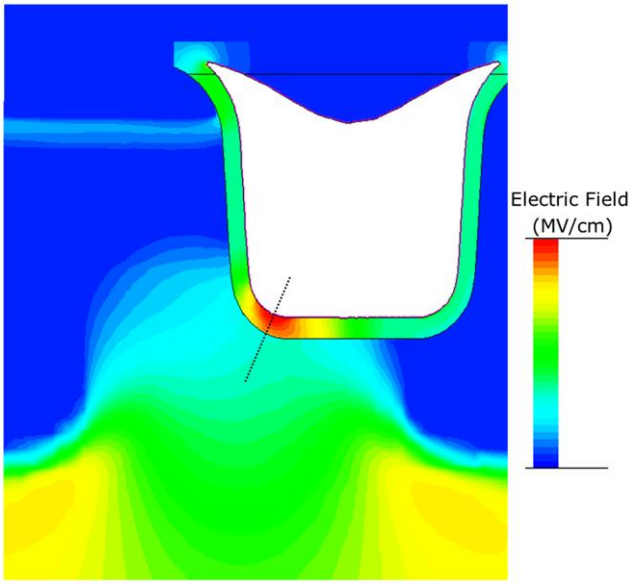

Fig. 2 Simulation of the electric field in blocking state: The dotted line indicates the most critical area with respect to the gate oxide field.

As mentioned before a critical issue regarding gate oxide reliability of the SiC MOSFETs is the limitation of the gate oxide field to a certain value fitting to a requested maximum failure rate. This is a known issue for a trench MOS structure in blocking state since the electric field in the trench corners is enhanced due to the trench shape. In addition, the drain bias causes field peaks. With respect to this specific cell configuration the field peak is found in the left trench corners. This local maximum of the electric field determines the lifetime of the gate oxide in blocking state. Therefore, it is necessary to have a careful look to the field distribution in blocking state. Fig. 2 presents a 2D simulation result for the electric field under worst case conditions, i.e. at maximum drain source voltage of $V_{DSS} = 1200$ V and a minimum gate voltage of $V_{GS} = -10$ V. The simulation indicates that the electric field in the gate oxide can be limited to a value of less than 4 MV/cm.

In summary, the described MOSFET cell concept is designed to combine small conduction losses with a sufficiently low gate oxide stress in on-state and in off-state being appropriate to fulfill the reliability requirements of industrial applications.

3. Device Performance

The following characterization data are measured on typical single chips mounted in TO-247 packages; part number IMW120R045M1.

3.1. Static Characteristics

The 1200 V CoolSiC™ MOSFET is designed for an operation with standard gate driver voltage levels of -5 V … 0 V for off-state and +15 V for on-state. The full output characteristics for selected gate voltages are shown in Fig. 3 for temperatures of 25°C and 175°C, respectively.

The typical on-resistance equals R_{DSon} = 45 mΩ at V_{GS} = +15 V, I_D = 20 A and T = 25°C. Please note that the slope of the curves is steadily decreasing with V_{DS} but does not fully disappear. There are two effects being responsible for this behavior. At lower gate voltages V_{GS} the drain current I_{DS} is limited by the MOS channel. With the channel fully open at reasonable large V_{GS}, the drain current is now governed by the JFET region. This behavior is intended in order to limit the saturation current for very high drain voltages V_{DS}, e.g. during a short circuit event. With

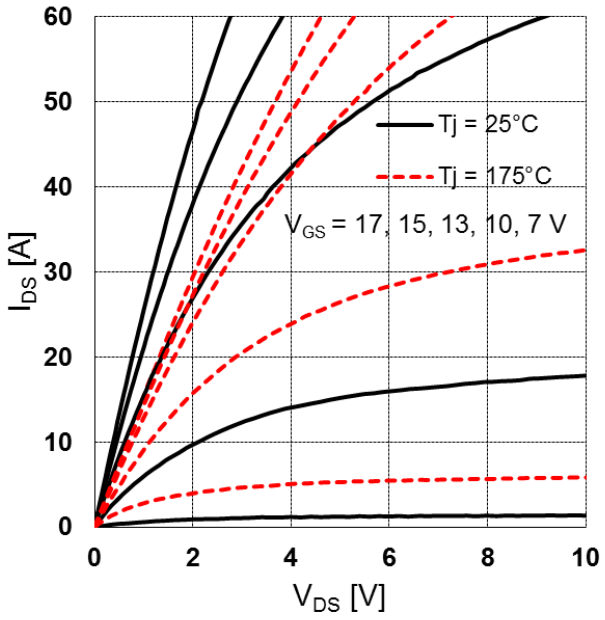

Fig. 3: Output characteristics showing the drain current I_{DS} as function of drain source voltage V_{DS} for gate source voltage V_{GS} = 17, 15, 13, 10, 7 V at 25°C (solid, black) and 175°C (red, dotted), typ. values, gate voltages sorted from top to down.

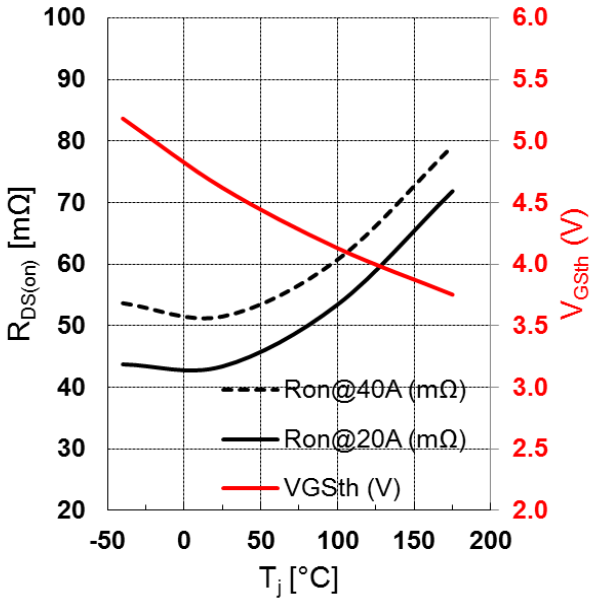

Fig. 4: Typical temperature dependency of $R_{DS(on)}$: black solid curve: V_{GS} = 15 V, I_{DS} = 20 A, black dashed curve: V_{GS} = 15 V, I_{DS} = 40 A, red curve: V_{GSth} (at V_{GS} = V_{DS}, I_{DS} = 10mA)

increasing temperature all main contributors to the on-resistance change, i.e. the MOS channel as well as the JFET region and the drift region. As their temperature coefficients are different the contribution of the JFET to the overall on-resistance decreases, leading to more linear curves in on-state at higher temperatures.

The temperature dependency of the on-resistance is plotted in Fig. 4 within the specified temperature range between -40°C and 175°C. The on-resistance has its minimum at room temperature and increases from R_{DSon} = 45 mΩ to typically 72 mΩ at 175°C taken at a rated current of I_{DS} = 20 A for V_{GS} = 15 V. The threshold voltage V_{GSth} is typically 4.5 V (at I_{DS} = 10 mA, V_{GS} = V_{DS}, T = 25°C) and decreases by about 6 mV/K down to 3.75 V at 175°C.

Typical transfer characteristics are shown in Fig. 5 for a drain source voltage of V_{DS} = 20 V again for two junction temperatures of 25°C and 175°C, respectively. In contrast to SiC MOSFET with a DMOS structure, the transfer characteristics are not just more or less parallel shifted towards lower gate voltages with increasing temperature. Fig. 5 indicates that there is a crossing point at V_{GS} = 15 V. The temperature dependence decreases with increasing gate source voltage. Qualitatively, this follows the threshold voltage dependency depicted in Fig. 4.

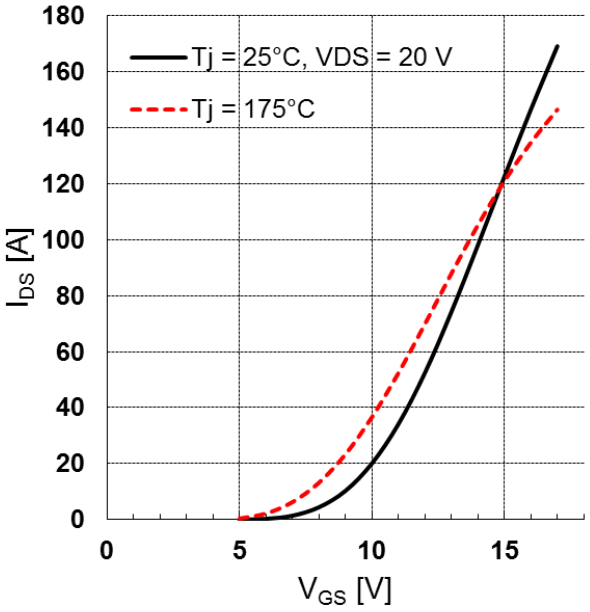

Fig. 5: Typical transfer characteristics measured in pulse mode at V_{DS} = 20 V at 25°C (solid, black) and 175°C (red dashed)

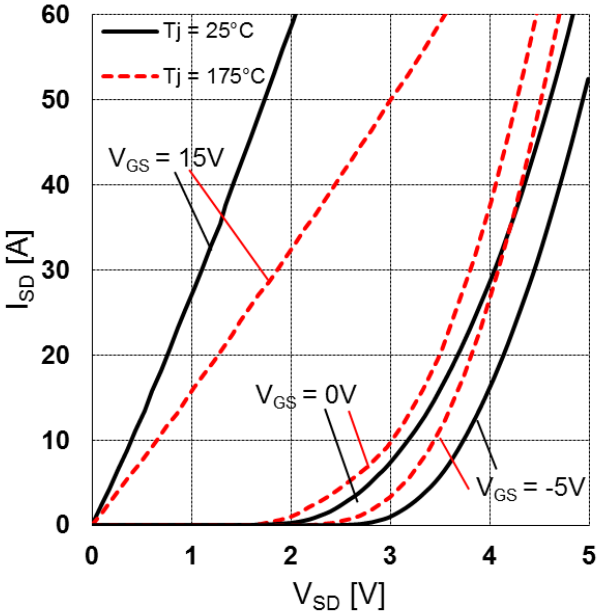

Fig. 6: Typical 3rd quadrant characteristics at 25°C (black, solid) and at 175°C (red, dotted), V_{GS} = +15 V, 0 V and -5 V, resp.

However, for normal operation keeping the current within a 3-fold rated current range (60A), the temperature coefficient is indeed negative but this will be found only for a short moment during the switching transient.

The characteristics of the 3rd quadrant are given in Fig. 6. The curves with a gate source voltage of V_{GS} = -5 V represent pure body diode operation without a partial bypass by the MOS channel. At zero gate voltage there is already some contribution of the channel to the current which lowers the source drain voltage V_{SD}. However, very low V_{SD} and linear characteristics are found as soon as the channel is turned-on by applying +15 V to the gate. Now the corresponding 3rd quadrant on-resistance falls down to 33 mΩ at 25°C and 57 mΩ at 175°C, respectively. These values are lower compared to the 1st quadrant since the JFET resistance is significantly reduced due to the inverse polarity of the pn junction.

Hence, in order to keep static losses in reverse conduction mode low, synchronous rectification is recommended by turning on the channel after an appropriate interlock time.

3.2. Dynamic Characteristics

The switching behavior is analyzed by double pulse experiments performed with a rapid test bench for discrete packages. The MOSFETs were mounted in 3-pin TO-247 housings. The tests were done in a half-bridge configuration or with a SiC Schottky diode (IDH20G120C5) in a chopper configuration.

An essential feature of the MOSFET is that the voltage slope for turn-on as well as for turn-off is fully controllable by the external gate resistor in order to cope with any dv/dt limitations required by the system. This is demonstrated in Fig. 7 which shows typical switching transients for 2 different gate resistors of R_{gext} = 10.2 Ω and 4.5 Ω, resp. Such double pulse experiments were done with different external gate resistors varied in a range between 2.2 and 30 Ω. The maxima dv/dt and di/dt of the transients were determined, switching energies were calculated and plotted in Fig. 8.

Fig. 8a proofs that the voltage slopes dv/dt for turn-off and turn-on can be easily controlled by the external gate resistor R_{gext} within in a range between 50 kV/µs down to 15 kV/µs. On the other hand it is plausible that the switching losses increase with the value of the gate resistor (see Fig. 8b). Very low switching losses can be achieved if the gate resistor is small, e.g. $E_{on} + E_{off}$ = 0.42 mJ for R_{gext} = 2.2 Ω.

The switching losses are almost invariant to temperature as long as the gate resistor is kept constant. This behavior is in contrast to that of an

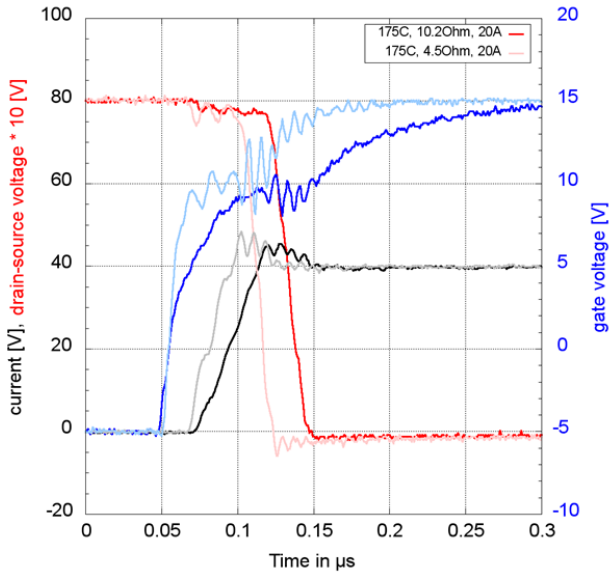

Fig. 7a Turn-on transient

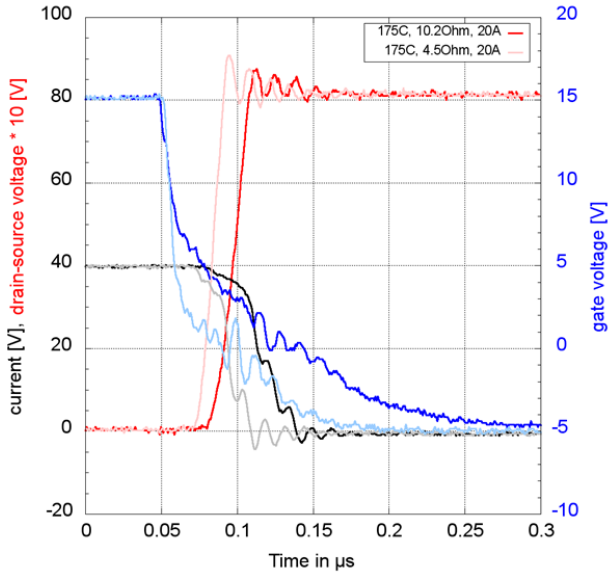

Fig. 7b Turn-off transient for 2 different external gate resistors R_{gext} = 10.2 Ω and 4.5 Ω, resp. (switching conditions: 800 V, 40 A, 175°C, freewheeling SBD type IDH20G120C5) Color codes of curves in Fig. 7a and 7b: R_{gext} = 10.2 Ω: I_D (black), V_{DS} (red), V_{GS} (blue) R_{gext} = 4.5 Ω: I_D (dark grey), V_{DS} (bright grey), V_{GS} (bright blue)

IGBT since minority carriers do not impact the device behavior, neither for the Schottky barrier diode nor in the MOSFETs. The dynamic behavior is mainly governed by the capacitances of the MOS system or by the built-up space charge regions. Both are in first order not dependent on temperature. Only the trigger point in time changes as the threshold voltage decreases with temperature.

An additional measure for a further reduction of the switching losses is given by the use of a 4-pin package which provides an additional Kelvin source pin. In case of a small gate resistor of R_{gext} = 2.2 Ω, the total switching energy per switching period will be reduced down to a value of E_{tot} = 0.39 mJ. As a rule of thumb, up to 30% of dynamic losses can be saved by using a 4-pin TO-247 package instead of one with 3 pins.

The switching performance of the MOSFET is also investigated in a half-bridge configuration. The low side MOSFET is switched with a double

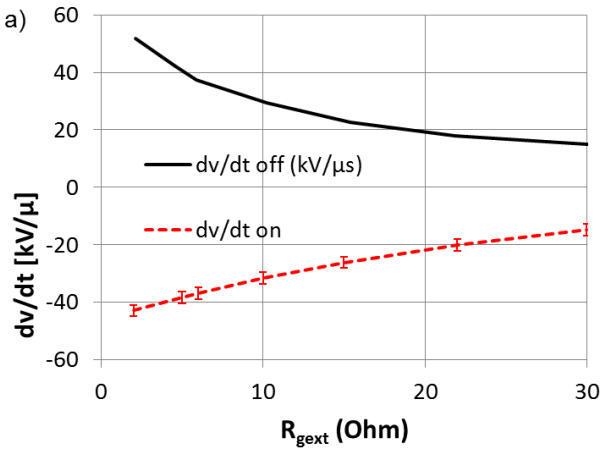

Fig. 8:a) maximum voltage slope dv_{DS}/dt measured at turn-on (red) and turn-off (black), Switching conditions: 800 V, 20 A, 175°C, freewheeling diode IDH20G120C5, TO-247-3

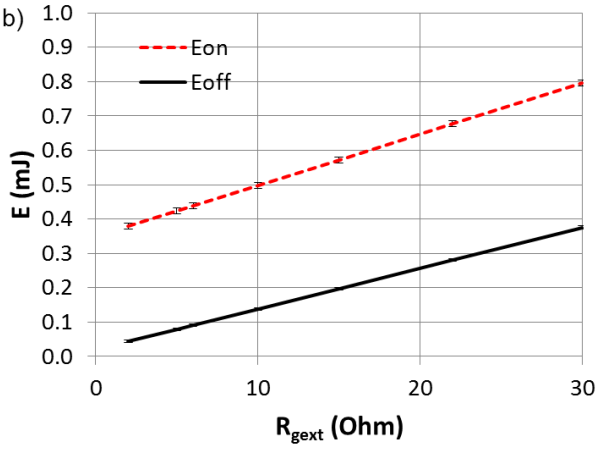

Fig. 8:b) E_{on} (red) and E_{off} (black) as function of external gate resistor R_{gext}. Switching conditions: 800 V, 20 A, 175°C, freewheeling diode IDH20G120C5, TO-247-3

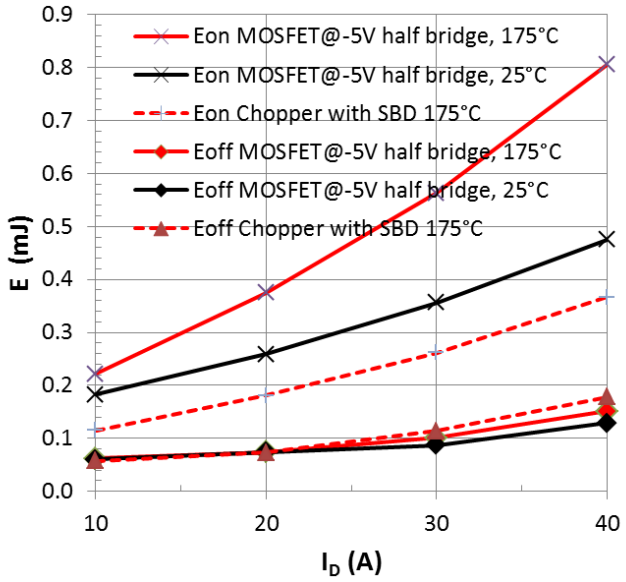

Fig. 9 Turn-on energy E_{on} (3 top curves) and turn-off energy E_{off} (3 bottom curves) as function of drain current, measured at 175°C (red) and 25°C (black) with 2 MOSFET in half bridge configuration in TO-247-4 (solid lines) compared to chopper configuration with a 20 A Schottky diode IDH20G120C5 (dashed). V_{bus} = 800 V, R_{gext} = 2.2 Ω, V_{GS} = -5 /+15 V.

pulse (V_{GS} = -5 /+15 V) whereas the high side MOSFET is kept in off-state (V_{GS} = -5 V). Fig. 9 indicates the determined switching energies as a function of the load current I_D. In order to allow an easy comparison also the results in the chopper configuration are included, where the high side is

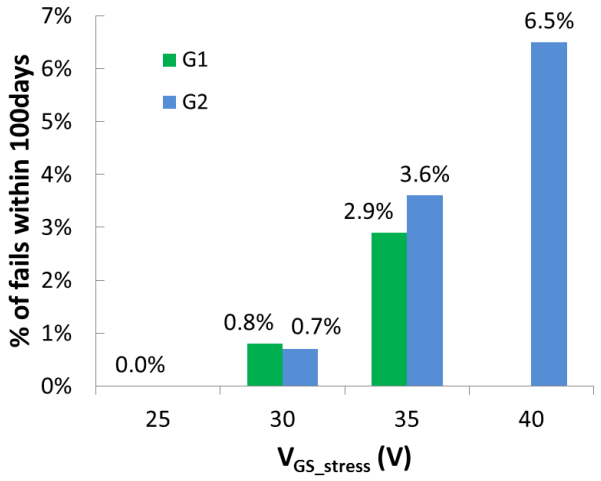

Fig. 10: Failure rate after 300 days long term gate stress test: 2 groups of 1000 MOSFETs were tested at 150°C with constant gate stress which was increased by 5 V after 100 days.

equipped with a 20 A rated Schottky barrier diode (IDH20G120C5). The 3 bottom curves show the turn-off energies E_{off} and do not significantly differ from each other. The most evident difference can be seen in the turn-on energies E_{on} (top 3 curves). In half-bridge configuration the body diode is active and shows an increasing impact with larger load current as well as higher temperature (see differences between red and black solid line in Fig. 9). Obviously this is an effect due to minority carriers injected by the forward biased pn-junction which generates a reverse recovery charge. However, the absolute values at the rated current of 20 A are still reasonable small.

4. Reliability

One of the most serious concerns about commercial SiC MOSFET compared to SiC JFET is the reliability of the gate oxide which is impacted by extrinsic defects. The root cause for extrinsic defects in the gate oxide of SiC MOS devices is dominated by the substrate material, the epitaxial process and, to a less significant contribution, by defects of the remaining process chain [7]. Hence, the challenge with respect to the gate oxide reliability of SiC MOS devices is how to ensure a low enough failure rate including extrinsic defects for a desired life time under given operation conditions, e.g. < 100 ppm in 20 y for industrial applications.

Long-time gate stress tests were performed with a large number of devices in order to determine the extrinsic gate oxide failure rates. The investigation was done for 2 groups consisting of 1000 discrete devices. The tests were performed at 150°C under constant gate bias stress for 3 times 100 days each. The gate source voltage was increased by +5 V after each 100 days. The time stamp of each failure was monitored. Fig. 10 shows the sum of fails after each 100 day sequence. In case of group G1 (green bars in Fig. 10), the test started at a gate source voltage of +25 V with zero fails after 100 days. The test of group G1 ended at +35 V, which is +20 V above the recommended use voltage of +15 V, with in total 2.9% fails after 300 days. The 2nd group (blue bars in Fig. 9) started at 30 V, continued at 35 V and ended at 40 V, with 6.5% fails in total.

As could be demonstrated in [8], these failure statistics fit well to the linear E-Model. By extrapolating this result to a life time of 20 years of device operation, the model predicts a failure

rate of 0.2 ppm. This experiment demonstrates an IGBT like reliability of the gate oxide with a failure rate under use conditions which is well below the typical industrial requirement specification of 100 ppm.

In addition, high temperature gate stress tests (HTGS) were performed. Both positive bias temperature stress (PBTI) as well as negative bias stress (NBTI) show well predictable power-law like threshold voltage shifts of the form $\Delta V_{GSth} \sim (\text{time})^n$ which is similar to silicon MOSFETs. Within 1000 h stress time at 150°C, the total threshold voltage shift reaches about +0.3 V for V_{GS} = +20 V and -0.1 V for V_{GS} = -10 V.

Different to silicon the BTI induced threshold voltage shift in SiC MOSFETs is superimposed by a fully recoverable on-off hysteresis [9]. This threshold voltage hysteresis is an intrinsic non-destructive feature of the SiC/SiO_2 interface and occurs most likely due to very fast charge trapping at interface defects. From an application point of view, the more relevant permanent or slowly recoverable threshold voltage shift component is limited to some 100 mV for typical DC stress conditions (1000 h / +20 V / 150°C). The remaining threshold voltage shift at the end of the BTI stress test is most likely due to charge trapping at defects within the gate oxide close to the SiC/SiO_2 interface. A carrier trapped at such a site does not degrade the oxide integrity but needs more time to be released.

5. Summary

This paper presents the results of a detailed performance characterization of the Infineon CoolSiC™ MOSFET. The device combines low static and dynamic losses with high Si-IGBT like gate oxide reliability right fitting to typical industrial requirements. The temperature behavior makes the device easy to operate, in particular for operation in parallel. The switching behavior can be fully controlled by the gate resistor.

6. Acknowledgements

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