Comparison of Different Cell Concepts for 1200V-NPT-IGBT's

R.Siemieniec, M.Netzel, R. Herzer, D.Schipanski

Abstract - IGBT's are relatively new power devices combining bipolar and unipolar properties. In this work we carried out theoretical investigations of IGBT cells with different concepts and properties using the two-dimensional device simulator ToSCA [1] and the process simulation system DIOS [2]. The investigations are done at three different cell types: a common planer gate cell with different p-base depths, a cell with double implanted emitter [3] and a cell with a trench gate structure. For the realization of devices with low static losses and a high degree of ruggedness an advanced cell concept is necessary. For ruggedness modelling of the IGBT's the calculation of the short circuit current is used. It is shown, that the concept of IGBT's with double implanted emitter is a good alternative to the trench IGBT concept. An improvement of the short circuit behaviour of this device is possible in addition with lower static losses.

I. Introduction of Cell Concepts

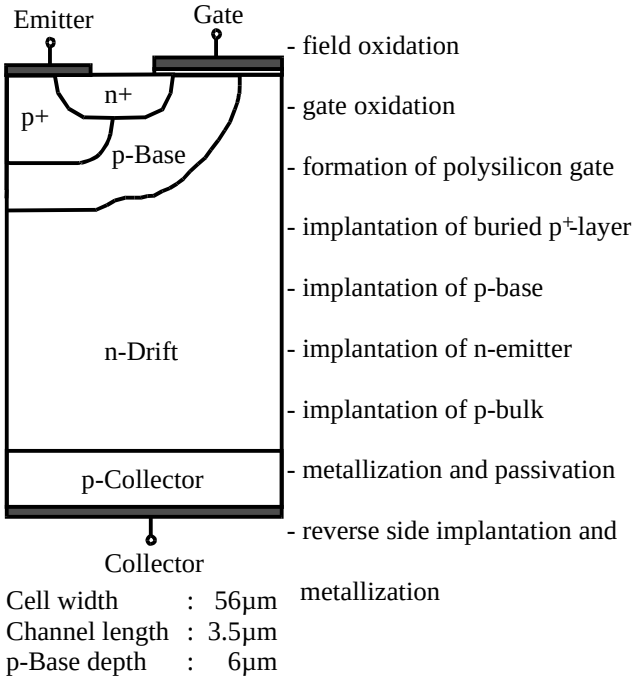

Fig.1: Structure and main preparation steps of planer gate IGBT

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The investigations are done at three different cell types: a common planer gate cell with different p-base depths, a cell with double implanted emitter introduced in [3] and a cell with trench gate. Figure 1 shows the basic structure, some typical dimensions and the main steps of the technological process, an adapted VDMOS-technology, of a common planer gate IGBT. An IGBT with a double implanted emitter and the main steps of technological process are shown in figure 2 [3]. This type is the result of a consistent improvement of vertical IGBT's for realizing low losses. Caused by the different concepts a new technological process is necessary. Essential for reaching low losses is the short channel. The high ruggedness is gained by the highly

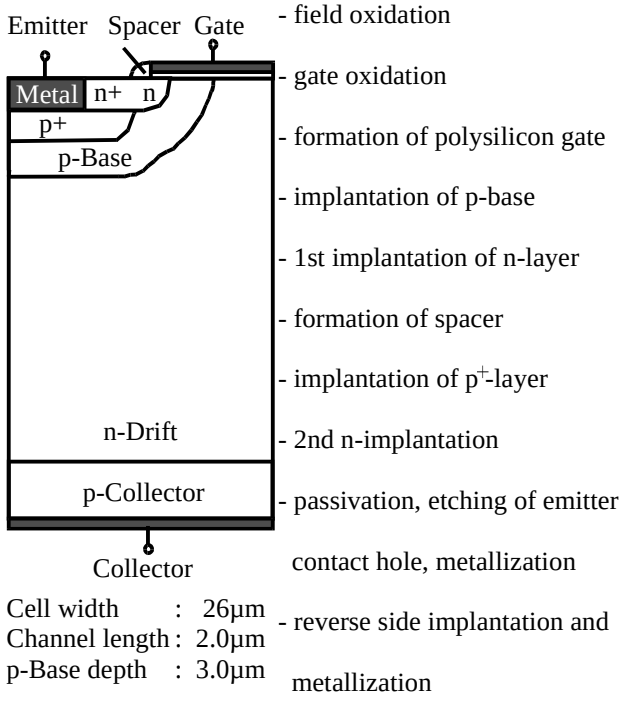
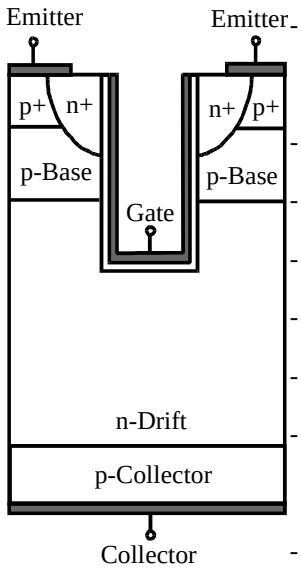


Fig.2: Structure and technology of a double implanted IGBT

doped p-layer beneath the n-emitter. Another way for the realization of low losses is the concept of IGBT's with a trench gate structure (figure 3) [4] [5]. Although this type promises excellent characteristics it is not produced in high quantities yet caused by it's high costs. If there will be a

way for a cheaper manufacturing it will be surely the dominating device.



- formation of b-base
- deposition of oxide- and nitride-layer
- opening of active area
- implantation of n-emitter
- trench formation by RIE
- deposition of gate oxide
- trench refill using polysilicon
- planarization and oxidation of polysilicon for gate formation
- remove of nitride layer
- metallization and passivation
- reverse side implantation and metallization

Cell width	:	12µm
Channel length	:	2.0µm
p-Base-depth	:	3.0µm

Fig.3: Structure and technology of a trench gate IGBT

II. Optimization of planer gate IGBT

The first investigations deal with common IGBT cells. The devices investigated here are 1200V non-punch through IGBT's. For this n-type silicon with a thickness of 250µm and a doping density of $6 \cdot 10^{13}$ is necessary to realize the aimed blocking capability.

Figure 4 shows the different output characteristics of this planer gate cells with varied p-base depth. How to expect, the cell with the lowest p-base depth shows the lowest losses (indicated by the on stage voltage), but even this cell has a very low Latchup resistivity (table I). A possibility to characterize this behaviour is the determination of the p-layer resistance as shown in figure 5. The reason for this is the fact that the parasitic npn-transistor (figure 6) will turn on if the voltage drop, caused by the lateral hole current flow in this region, reaches 0,7V. Due to this the whole device is latching.

Another point of interest is the ruggedness of the devices. One possibility to characterize this property is the short circuit behaviour of the device. For this the short circuit case II is calculated (the turned on device is switched to the

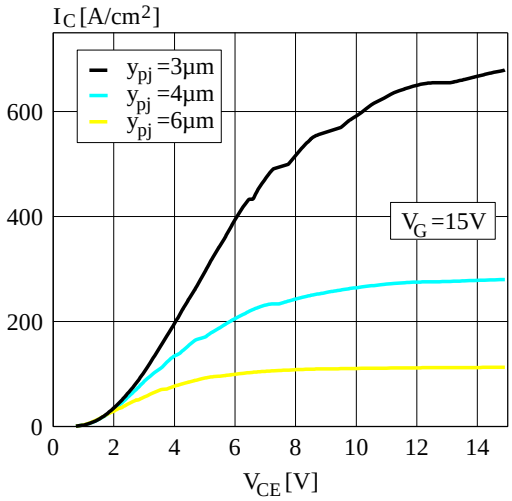


Fig.4: Output characteristics of IGBT with different p-base depth

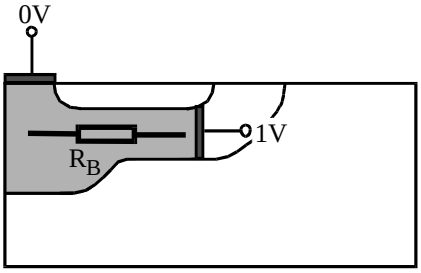


Fig.5: Determination of p-base resistance

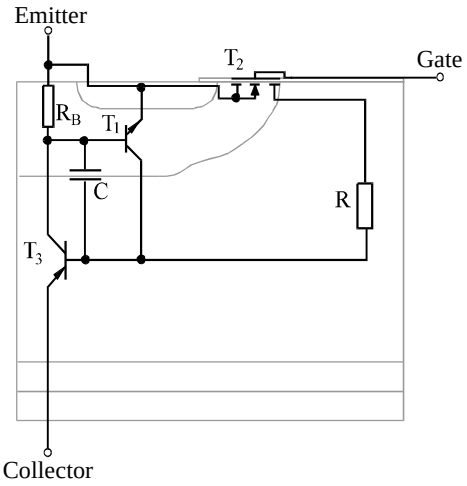


Fig.6: Equivalent circuit of an IGBT

running voltage, the result is the current after the transient period). Figure 7 shows the schema used for the simulation. As to be seen, no series inductivity and no inverse diode were included, so the worst case for the device was simulated. Figure 8 shows collector current and -voltage in the first 500ns of shorting. The results of the investigations on Latchup resistivity and short circuit behaviour are shown in table I too.

It's obvious that the IGBT with the highest p-base depth shows the best ruggedness, but even the highest static losses. The devices with lowest p-base depth show lowest losses, but an insufficient ruggedness (dynamic avalanche breakdown occurs) and Latchup resistivity. Also the type with a p-base depth of 4µm has not a sufficient ruggedness. The reason for that is the difference between the static simulation and the done dynamic measurements (resulting in a higher current level) for the determination of the short circuit current. So a new cell concept is necessary.

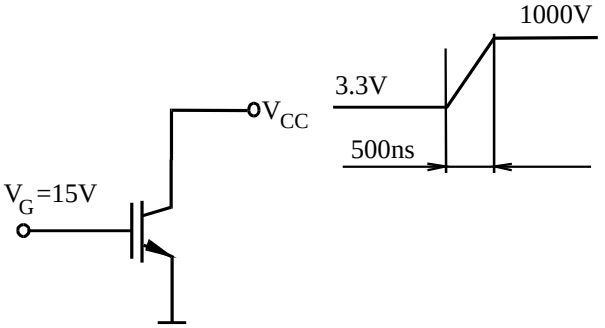


Fig.7: Schematic for the simulation of the short circuit behaviour

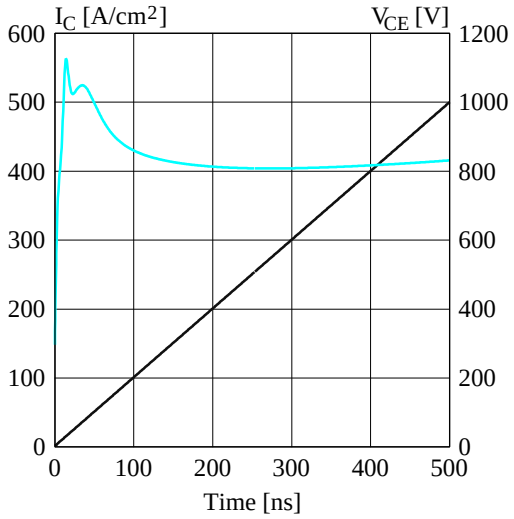


Fig.8: Collector current and voltage in case of short circuit

III. Advanced Cell Concepts for IGBT's

As mentioned before there are different cell concepts for the realization of IGBT's with better properties. One possibility is the realization of a structure with a double implanted emitter using a spacer technology [3]. Caused by the smaller cell width in comparison with the standard cell it is possible to reach higher current densities of the whole device. Yet far better properties are realizable with trench IGBT's as the second new device concept, but here a highly developed and expensive technology is needed. Trench IGBT's show very good properties, especially low forward losses caused by the elimination of the parasitic JFET and the low channel resistance. So this structure allows a further reduction of cell width as well. Figure 9 shows the three different output characteristics, the interesting values are shown in table II.A static Latchup has not occurred by all of the three types. Both of the advanced cell types have a higher short circuit current. During the simulation of short circuit behaviour of trench IGBT dynamic avalanche break-

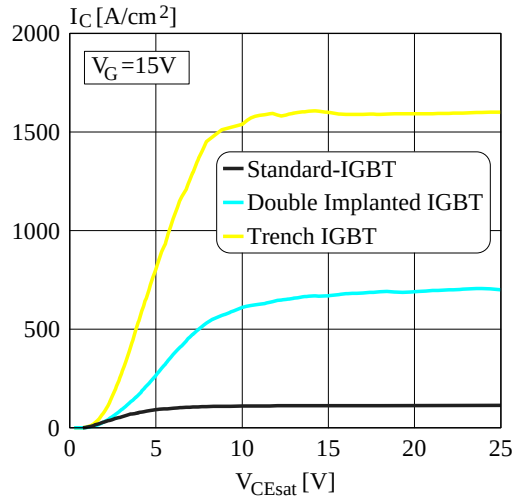


Fig.9: Output characteristics of different types of IGBT

TABLE I

DEPENDENCE OF DEVICE CHARACTERISTICS ON P-BASE DEPTH

p-base depth	3µm	4µm	6µm
V_{CESat}(I= 50A/cm²)	2.2V	2.4V	2.7V
V_{CESat}(I=100A/cm²)	2.9V	3.3V	6.2V
$I_{Latchup}$	1070A	1950A	no
R_B	0.86Ω/cm	0.56Ω/cm	0.42Ω/cm
I_{ShC}	Avalanche	390A	133A

TABLE II

DEVICE CHARACTERISTICS OF DIFFERENT IGBT TYPES

IGBT type	Planer Gate	Double implanted	Trench gate
cell width	56µm	36µm	10µm
V_{CESat}(I= 50A/cm²)	2.7V	2.3V	1.7V
V_{CESat}(I=100A/cm²)	6.2V	3.15V	2.1V
R_B	0.42Ω/cm	0.1Ω/cm	0.03Ω/cm
I_{ShC}	133A	680A	Avalanche

down happens. To prevent this a further optimization of the cell structure is necessary.

Although trench IGBT's shows lower forward losses and a high Latchup resistivity, the double implanted IGBT will surely discover a wide range of applications because it's good characteristics and more simple, less expensive technology as trench IGBT's have. The simulation results show a very good ruggedness and low losses if optimized parameters were used, but also a strong dependence of the device properties on the parameters chosen for the single implantations. One more reason is the lower short circuit current of double implanted IGBT in comparison with trench gate devices.

IV. Investigations on IGBT's with double implanted emitter

For the optimization of IGBT's with a double implanted emitter (DIGBT) first the influence of the two n-implantations is investigated. For this the doping profiles are described by Gaussian profiles based on the results of process simulation. This is an easy and fast way for the variation of different parameters. One important condition during this investigations is the invariability of N_{Amax} for realizing a constant threshold voltage, so it was necessary to adapt the p-doping as well.

As second the influence of geometrical dimensions (p-base width, cell width etc.) is analyzed. For this we use the same doping profile that has been used for the investigations before. The purpose of the investigations is the optimization of the device in relation to low static losses and a good ruggedness.

A. Results of device process simulation

The basic process used for this simulation is shown in figure 2. The n-type substrate is the same as used for the standard IGBT's (thickness 250µm, doping density: $6 \cdot 10^{13}$). The spacer is formed by vertical anisotropic etching of an oxide layer with a thickness of 500nm. The p-doped emitter is unshorted. Holes and electrons have the same carrier lifetime of 50µs.

Figure 10 shows one of the simulated structures.

B. Influence of the n-implantations on device ruggedness

In table III the different doping parameters for the variation of the 1st n-implantation and their results are shown. How to expect the short circuit current is influenced by this implantation, but it is not usable for the adjustment of the current density caused by the weak influence. So this implantation is mainly necessary for setting the threshold voltage.

The used parameters for the variation of the 2nd n-implantation are shown in table IV. Similar to the previous investigations there is only a weak dependence between the short circuit current and the doping concentration.

Caused by this unsatisfactory results further investigations of the device properties are necessary.

TABLE III

I_{SHC} AND N_{A1MAX} IN DEPENDENCE OF N_{D1MAX}

N_{D1max} [cm^{-3}]	N_{A1max} [cm^{-3}]	I_{ShC} [A]
$5 \cdot 10^{18}$	$1.28 \cdot 10^{17}$	704
$3 \cdot 10^{19}$	$1.2 \cdot 10^{17}$	771
$6 \cdot 10^{19}$	$1.19 \cdot 10^{17}$	788
$8 \cdot 10^{19}$	$1.18 \cdot 10^{17}$	790

TABLE IV

I_{SHC} IN DEPENDENCE OF N_{D2MAX}

N_{D2max} [cm^{-3}]	N_{A2max} [cm^{-3}]	I_{ShC} [A]
$5 \cdot 10^{18}$	$5 \cdot 10^{19}$	789
$1 \cdot 10^{19}$	$5 \cdot 10^{19}$	792
$2 \cdot 10^{19}$	$5 \cdot 10^{19}$	810
$5 \cdot 10^{19}$	$5 \cdot 10^{19}$	814

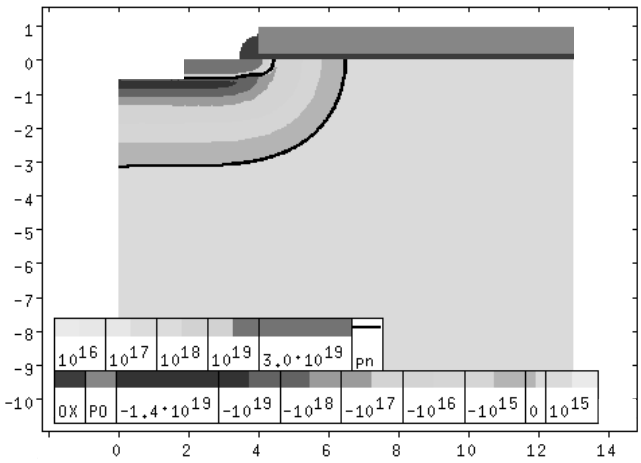


Fig.10: Simulated DIGBT structure

C. Influence of cell design

Here the influence of changes of the cell design is investigated. Figure 11 shows the surface region and the varied dimensions (half cell width w, contact hole width a, distance to poly gate b) of the device. For all investigations the same parameters during process simulation have been used.

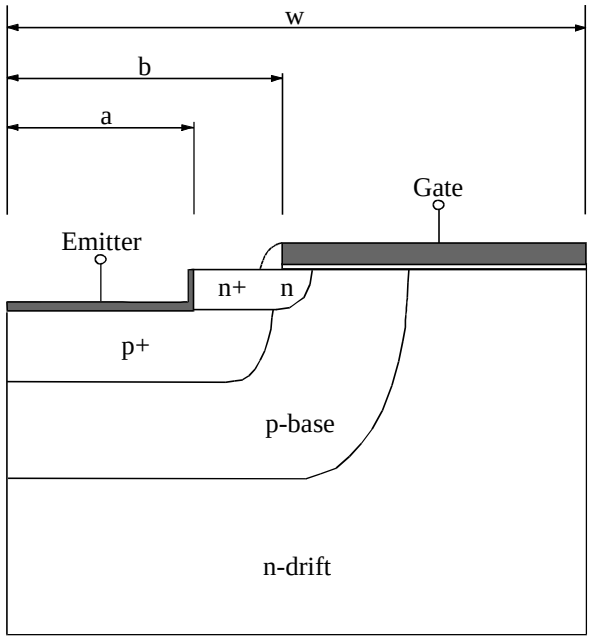


Fig.11: Varied dimensions of the DIGBT

First the cell width is changed. That means a variation of the drift region. By this the optimal cell width may be found. Parameters and results are shown in table V.

So a decrease of static losses does not cause an increase of the short circuit current. In comparison table VI shows the results for structures with shorter contact hole and poly gate distance. Here the second type has the lowest static losses, but even this cell has a high short circuit current. Although in case of an cell width of 11µm the JFET causes a strong increase of the losses, this cell shows the highest short circuit current.

Table VII shows some more results of the variation of contact hole width. It is interesting that the bigger contact hole causes a decrease of the short circuit current level by almost equal losses.

Furthermore table VIII shows the influence of the distance to the poly silicon gate b. Here the further increase of this design parameter leads to worse results than before.

TABLE V

VARIATION OF CELL WIDTH I

Cell width w [µm]	14	16	18
a [µm]	2.5	2.5	2.5
b [µm]	5.0	5.0	5.0
V_{CESat}(I= 50A/cm²)	2.7	2.5	2.3
V_{CESat}(I=100A/cm²)	3.6	3.3	3.15
I_{ShC}(V_G=15V)	870	790	680

TABLE VI

VARIATION OF CELL WIDTH II

Cell width w [µm]	11	13	15
a [µm]	1.5	1.5	1.5
b [µm]	4.0	4.0	4.0
V_{CESat}(I= 50A/cm²)	3.1	2.3	2.45
V_{CESat}(I=100A/cm²)	4.1	3.1	3.2
I_{ShC}(V_G=15V)	1300	1080	980

TABLE VII

INFLUENCE OF CONTACT HOLE WIDTH

a [µm]	2.5	3.5
b [µm]	5.0	5.0
Cell width w [µm]	17	17
V_{CESat}(I= 50A/cm²)	2.4	2.45
V_{CESat}(I=100A/cm²)	3.2	3.2
I_{ShC}(V_G=15V)	720	680

TABLE VIII

INFLUENCE OF DISTANCE TO POLY GATE

b [µm]	5.0	6.0
a [µm]	3.5	3.5
Cell width w [µm]	17	17
V_{CESat}(I= 50A/cm²)	2.45	2.55
V_{CESat}(I=100A/cm²)	3.2	3.4
I_{ShC}(V_G=15V)	680	740

A result of this simulations is that it is possible to optimize IGBT's with double implanted emitter for both, low losses and a good ruggedness as well. For the realization of devices with optimized characteristics it has to be

mentioned that a change in one of the parameters leads to a new optimization of the other parameters.

V. Conclusion

Different cell concepts for IGBT's and their essential steps of device technology have been introduced. Caused by the impossibility of a further reduction of forward losses hand in hand with a high ruggedness and Latchup resistivity this new cell types has been developed. The concept of an IGBT with double implanted emitter [3] realizes a good performance even in comparison with trench IGBT's by using a simpler technology.

Using two-dimensional process- and device simulation tools it has been shown, that a necessary reduction of the short circuit current level of double implanted IGBT's does not lead to an increase of forward losses. So this device concept is supposed to be the more important one in the next future.

Acknowledgement

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