Performance and Ruggedness of 1200V SiC - Trench - MOSFET

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***Abstract*— This paper describes a novel SiC trench MOSFET concept. The device is designed to balance low conduction losses with Si-IGBT like reliability. Basic features of the static and dynamic performance as well as short circuit capability of the 45 mΩ / 1200 V CoolSiC™ MOSFET are presented. The favorable temperature behavior of the on-state resistance combined with a low sensitivity of the switching energies to temperature simplify the design-in. Long-term gate oxide tests reveal a very low extrinsic failure rate well matching the requirements of industrial applications.**

Keywords—SiC, trench, MOSFET, reliability, ruggedness

I. INTRODUCTION

Wide band-gap semiconductors based on silicon carbide are most attractive for high power devices due to low losses, improved temperature capability and high thermal conductivity. Although SiC Schottky barrier diodes have been commercially available for more than a decade, active switches have only quite recently been ready for the market. Early research and development studies of SiC MOSFETs revealed that the switching performance of high voltage SiC MOSFETs is excellent and easy to handle [1] but there were show stopping issues regarding the MOS channel mobility and gate oxide reliability. Compared to this early stage of SiC MOSFETs the SiC JFET performs much better, is much more robust and very short circuit rugged [2]. However, the MOSFET was and is seen as the favorite SiC power switch compared to the JFET and BJT since it is normally-off and voltage controlled. Meanwhile the inversion channel mobility has been significantly improved e.g. by nitridation techniques using nitric oxide or nonplanar structures [3],[4]. Significant progress could be achieved in improving the extrinsic failure rate of the gate oxide. In addition, assets of a frontend fabrication process in 6-inch regarding reproducibility, stability, precision and efficiency are utilized effectively.

This paper shows typical static and dynamic characteristics of the newly developed SiC Trench-MOSFET combining all these achievements.

II. DEVICE CONCEPT

A. Challenges compared to silicon-based MOSFETs

Si and SiC both have a thermal oxide which is at a first glance the common way to create an almost ideal MOS interface. But there are some well-known challenges to making a SiC MOSFET. Carbon atoms at the interface tend to form clusters or dangling bonds and cause significantly lower field-effect channel mobility due to a much higher density of interface states compared to Si. Hence a much more sophisticated gate oxide process is needed to mitigate the negative effect of these interface states. The field-effect channel mobility is still in the range of only 5–50 cm²/Vs, which is a poor fraction of the bulk mobility of ~200 cm²/Vs (at a bulk doping level equal to the channel doping). Further defects are located near the interface but in the gate oxide (NIT) and these trap electrons. Due to their energy levels which are positioned somewhere within the larger bandgap of SiC, they can interact in a larger span of time constants by trapping or emitting electrons. The balance between trapping and emission rates of these NIT states causes higher threshold voltage shifts depending on the gate voltage profile and temperature [5]. Furthermore, as SiC devices allow roughly 10 times higher electric fields than their Si counterparts, the electric field in the gate oxide has to be limited in order to maintain a required reliability of the device.

B. Proposed cell concept

The CoolSiC™ MOSFET is, in contrast to the commonly used planar cell, a trench SiC MOSFET based on a novel asymmetric concept. Fig. 1 gives a sketch of both concepts.

In the trench device, only one side of the trench sidewall is

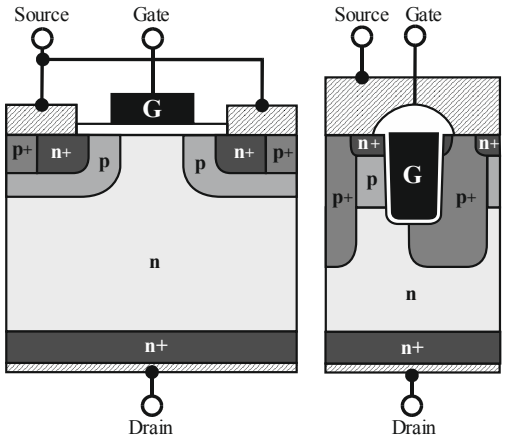

Fig. 1: Sketch of a commonly known planar-gate MOSFET (left) and the proposed trench SiC MOSFET cell (right)

used as MOS channel which is exactly aligned to the preferred <11$\bar{2}$0> crystal plane by a special process. Making use of this favorite crystal plane is seen as the key to achieving a minimum of interface states. It was shown experimentally that the channel mobility for this crystal plane is about two times better than for other crystal planes [6] and that high channel mobility can be realized. In combination with nitridation techniques to ensure a good interface state passivation, the channel mobility is further improved and shows reduced Coulomb scattering. At the same time, all these measures also minimize the amount of threshold voltage shift with temperature and improve the device reliability. Thanks to the improved channel properties the device can be driven at a sufficient low gate oxide field in the on-state. The oxide thickness is designed for the commonly used on-state gate-source voltage of V_{GS} = + 15 V.

Deep p-wells are used in order to limit the electric field in the gate oxide at the bottom and the corners of the trench. These p-type regions also serve as emitters of the body diode which can be used for freewheeling operation. This MOSFET structure is very compact, resulting in a low on-resistance which is about half the value of typical DMOS cells. This cell construction inherently has a favorable small ratio of the Miller charge Q_{GD} related to the gate-source charge Q_{GS}. Q_{GS} is comparably large since a large part of the trench contributes to it, i.e. the n+-type areas and all p-type areas which are connected via a well to the source. This allows for a well-controlled switching with very low dynamic losses [7]. In particular this feature is essential to suppress undesirable additional losses caused by a parasitic turn-on in topologies using half bridges.

The cell design also helps to obtain an adequate short-circuit capability. The JFET region formed by the adjacent p-emitter regions is not only good at limiting the oxide field in the trench corner, but also lowers the saturation current of the device by adjusting the distance between the p-type regions. A smaller distance supports both a lower saturation current and lower electric field in the gate oxide of the trench corner, but causes an additional contribution in the overall on-state resistance due to the JFET.

III. Results

The MOSFET shown is designed for a blocking voltage of 1200 V addressing e.g. photovoltaic applications and uninterruptable power supplies (UPS). TABLE I. lists key parameters of the device. It is tailored for long-term stability within a gate voltage range between -5 V and +15 V.

TABLE I. KEY PARAMETERS OF THE COOLSIC™ MOSFET

Parameter	*Value*	*Unit*	*Condition*
$R_{DS(on),\,typ}$	45 (75)	mΩ	Single die, T_j = 25°C (175°C) I_D = 20 A, V_{GS} = 15 V
V_{DSS}	> 1200	V	-55°C < T_j < 175°C
V_{GS}	-5 / +15	V	recommended range
V_{GS}	-10 / +20	V	maximum rating
V_{GSth}	4.5 (3.8)	V	T_j = 25°C (175°C) I_D = 10 mA, V_{GS} = V_{DS}
V_{SD}	3.3 (3.1)	V	T_j = 25°C (175°C) I_D = 20 A, V_{GS} = 0 V

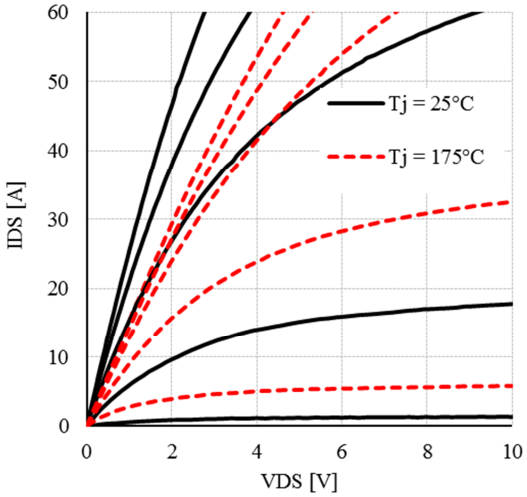

Fig. 2: Typical 1st quadrant output characteristics for gate voltages of V_{GS} = 17, 15, 13, 10, 7 V at 25°C (solid) and at 175°C (dashed)

A. Static Performance

The 1200 V CoolSiC™ MOSFET is optimized for an operation with standard gate driver voltage levels of -5 V to 0 V for the off-state and +15 V for the on-state. The output characteristics at two temperatures of 25°C and 175°C for selected gate voltages are shown in Fig. 2. The on-state strongly depends on the applied gate voltage, a feature which is common for SiC MOSFETs. The curves are nonlinear even for high gate voltages since both the resistance of the MOS channel and the resistance of the JFET being formed by the p-wells are voltage controlled and depend on V_{DS}. This JFET zone represents an additional resistance as it causes a locally reduced conduction area. Still it is needed to limit the electric field of the gate oxide in the trench corner in blocking mode.

The body diode shows a low forward-voltage drop below 4 V (V_{GS} = -5 V, channel off, I_D = 20 A, see Fig. 3). In reverse conduction the on-resistance amounts 33 mΩ at V_{GS} = 15 V. This I_D-V_{DS} curve is more linear than in the 1st quadrant due to the JFET effect formed by the p-wells.

Fig. 4 shows the temperature dependence of the on-resistance and of the threshold voltage. The on-resistance

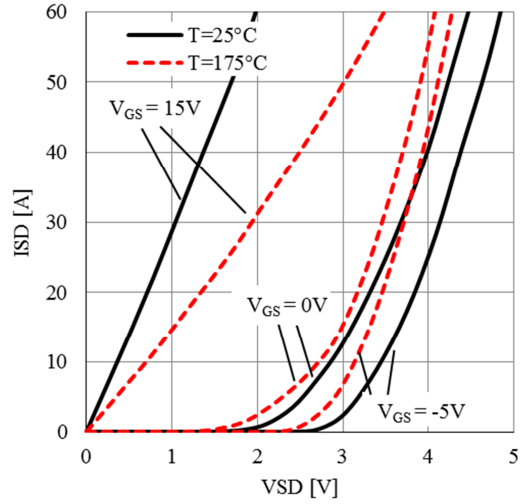

Fig. 3: Typical 3rd quadrant characteristics at 25°C (solid) and 175°C (dashed), V_{GS} = +15V, 0 V and -5V

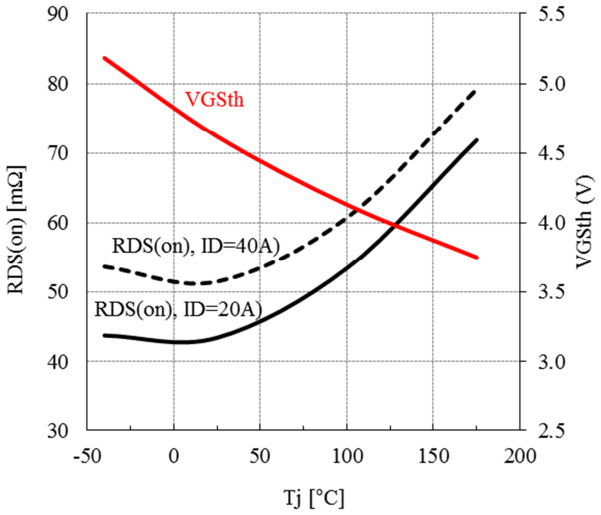

Fig. 4: Typical temperature dependence of $R_{DS(on)}$ at I_D = 20 A, 40 A and of V_{GSth} (V_{GS}=V_{DS}, I_D = 10mA)

increases by 70 % from 25°C to 175°C and as such shows the commonly found significant dependence on temperature as expected for MOSFET devices with small defect densities at the gate oxide interface. This behavior can be directly attributed to the advantageous channel orientation along the preferred crystal plane. The measured positive temperature coefficient is also beneficial for the paralleling of devices. The overall temperature behavior is determined by the temperature-dependent properties of the MOS channel, the JFET region and the drift layer. The MOS channel has a negative temperature characteristic mainly due to the threshold voltage decreasing with temperature whereas the n-type doped drift zone has a positive temperature coefficient. The increase of the resistance with load current is again explainable by the JFET. Typical transfer characteristics are shown in Fig. 5.

The p-wells which form the JFET region are also beneficial in order to limit the saturation current and make the device short-circuit rugged. Fig. 6 shows a typical short circuit test. The device is switched on / off between 0 V and +15 V under 800 V bus voltage and a case temperature of 175°C (i.e. short circuit type 1). After 5 µs the device is able to turn-off safely.

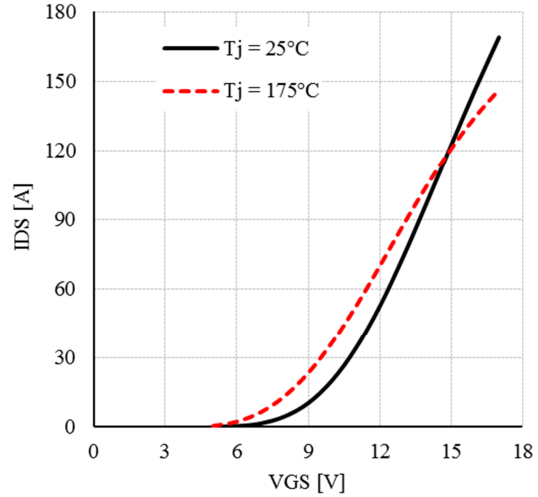

Fig. 5: Typical transfer characteristics at V_{DS} = 20 V at 25°C (solid) and 175°C (dashed)

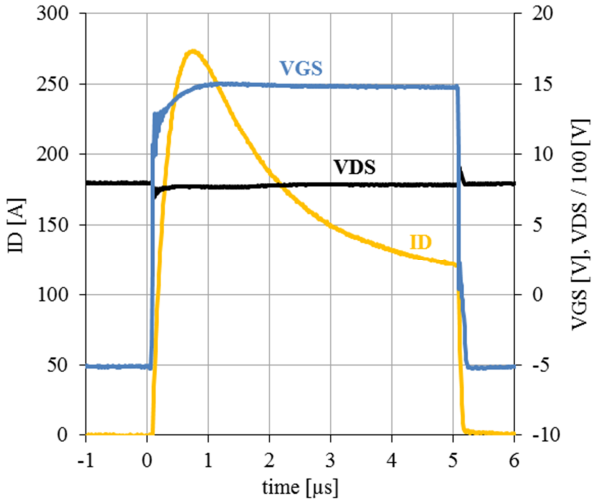

Fig. 6: Typical short circuit waveforms: the device withstands 5 µs in short circuit. Conditions: Tc = 25°C, R_G = 7.9 Ω, Vbus = 800 V, V_{GS} = -5 V / +15 V, package TO-247-4 pin.

B. *Dynamic behavior*

The capacitances and their dependencies on the drain-source voltage give key information about the switching behavior (Fig. 7). Due to the asymmetric p-well structure the Miller capacitance C_{rss} and the linked Miller charge Q_{GD} are quite small. This makes parasitic re-turn-on losses easy to suppress. Turn-on and turn-off energies for different load currents, temperatures and different free-wheeling devices are depicted in Fig. 8 and Fig. 9. The turn-on energies E_{on} dominate the switching losses and can be minimized independent of the temperature if the MOSFET is used in combination with an SBD diode (both curves in Fig. 8 overlap). Compared to the E_{on} of the MOSFET in half-bridge configuration, 30-50 % of the losses can be saved. In half-bridge configuration the body diode is active and shows an increasing impact with both a larger load current and a higher temperature. This is a bipolar effect linked to the build-up of a reverse recovery charge. However, the absolute values at the rated current of 20 A are still very small compared to 1200 V Si IGBTs.

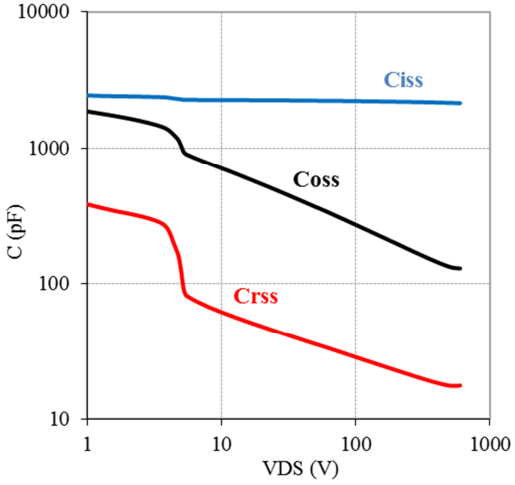

Fig. 7: Small signal capacities C_{iss}, C_{oss}, C_{rss} as function of V_{DS} measured at 1 MHz, V_{GS} = 0 V, internal gate resistor is typical 4 Ω.

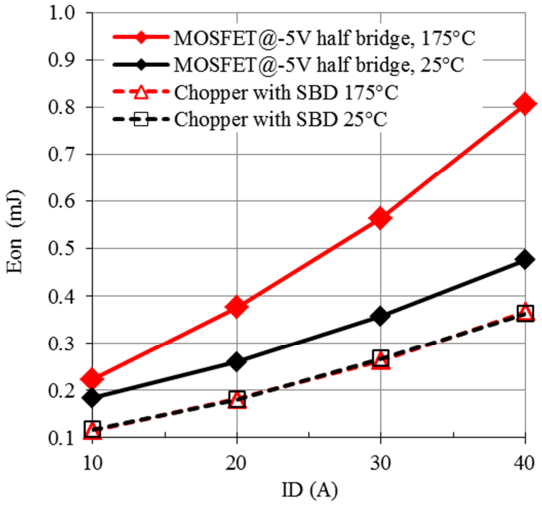

Fig. 8: Turn-on energy as function of drain current, measured in TO-247-4 pin (V_{DS} = 800 V, R_g = 2.2 Ω, V_{GS} = -5 V / +15 V)

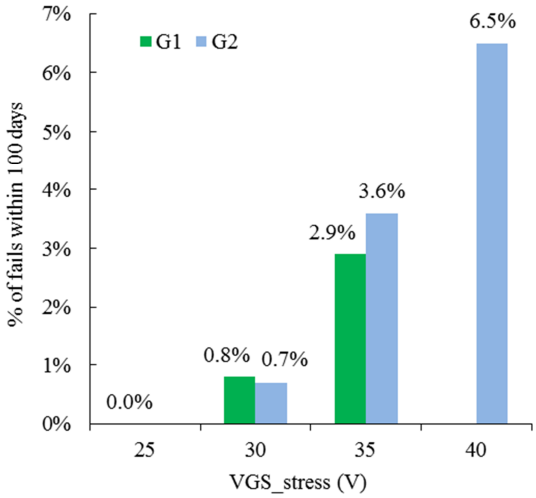

Fig. 10: Failure rate after 300 days long term gate stress test: 2 groups of 1000 MOSFETs were tested at 150°C with constant gate stress which was increased by 5 V after 100 days

C. *Reliability*

To investigate the gate oxide reliability over the targeted device lifetime of 20 years, long-time gate stress tests were performed with a large number of devices in order to determine the extrinsic gate oxide failure rates. The investigation was done for 2 groups consisting of 1000 discrete devices. The tests were performed at 150°C under constant gate bias stress for 300 days. During this test, the gate-source voltage was kept constant for 100 days and then increased by +5 V after each 100 day period. The time stamp of each failure was monitored. Fig. 10 shows the sum of fails after each 100 day sequence. In case of the 1st group G1 (green bars in Fig. 10), the test started at a gate-source voltage of +25 V and showed zero fails after 100 days. The test of group G1 ended at +35 V, which is +20 V above the recommended use voltage of +15 V, with in total 2.9 % fails after 300 days. The 2nd group G2 (blue bars in Fig. 10) started at 30 V, continued at 35 V and ended at 40 V, with 6.5 % fails in total.

As demonstrated in [8], these failure statistics fit well to the linear E-Model. By extrapolating this result to use conditions, i.e. V_{GS} = 15 V at 150°C, the model predicts a failure rate of less than 1 FIT per die. This experiment gives evidence of a typical reliability of the gate oxide as required for industrial applications.

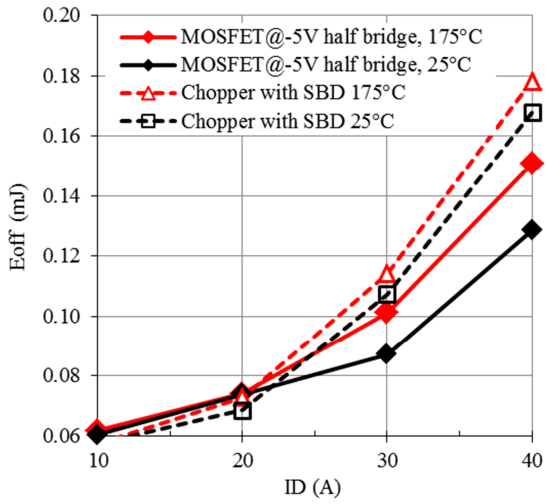

Fig. 9: Turn-off energy as function of drain current, measured in TO-247-4 pin (V_{DS} = 800 V, R_g = 2.2 Ω, V_{GS} = -5 V / +15 V)

IV. Conclusion

The new CoolSiC™ MOSFET based on an asymmetric trench cell concept combines excellent reliability features with attractive low on-resistance, threshold voltage and short circuit ruggedness.

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