Design considerations for charge-compensated power MOSFET in the medium-voltage range

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Abstract

Low-voltage power MOSFETs based on charge-compensation using a field-plate offer a significant reduction of the area-specific on-resistance. The extension of their blocking capability into the so-called medium-voltage range of 150 V - 300 V promises devices with excellent properties being attractive for a wide range of applications. There are two approaches how this voltage-range extension can be realized. Both concepts are linked to different device performance and different development effort. This work discusses both concepts on example of the 150 V device class and compares the gained performance on device and application level.

Keywords: MOSFET, power device, application requirements, device design, device performance

INTRODUCTION

The general trend in the industry towards the reduction in size of power systems imposes challenges on the design from the system down to the semiconductor level. The advances in power semiconductor technologies target to lower the system's associated losses. These allow for a general size reduction by various means ranging from the use of smaller magnetic components due to the use of higher switching frequencies to the possibility of reducing the size of, or even eliminating, the heatsinks.

This increase in power density translates into more and more challenging conditions for the power devices. Not only the on-resistance of the devices is reduced but also the general Figure of Merit ($FOM_G = R_{DS(on)} \cdot Q_G$), the Switching Figure of Merit ($FOM_{GD} = RDS(on) \cdot Q_{GD}$) and the Figure of Merit with respect to output charge ($FOM_{OSS} = RDS(on) \cdot Q_{OSS}$) are minimized. In many applications this results in large improvements of the switching speed, however this is usually linked to higher current and/or voltage slew rates (di/dt and dv/dt). At the same time the current density in the devices increases (see Fig. 1) which all calls for maintaining a high ruggedness of the devices.

Low-voltage power MOSFETs experienced dramatic improvements over the past decade thanks to the application of the charge-compensation principle to this device class. Stepping forward in the wafer manufacturing technology the breakdown voltage was extended over the years towards the voltage range between 150 V … 300 V.

Different to the lower voltage range where a large number of these devices are used in just one or two main application fields this is fundamentally different in the higher voltage range. Here the devices are used in many different topologies targeting a wide range of application fields, and markets are significantly more fragmented between the different types of application.
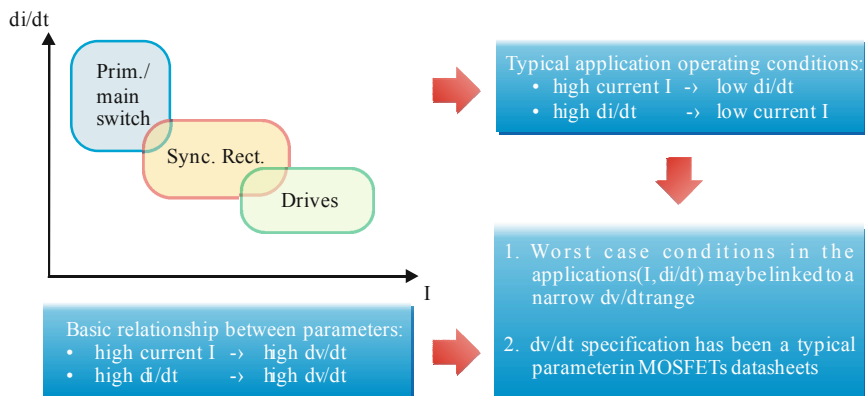

Fig. 1: Typical relationships between di/dt, dv/dt and current

APPLICATION REQUIREMENTS

In case of the 150 V device class, a bigger market segment is formed by power supplies for telecommunication appliances. Here the devices are usually found in the synchronous rectification stage of the AC/DC converter of power supplies (Fig. 2) and also at the primary side of the isolated DC/DC brick converters (Fig. 3). In both cases a high power density and a high efficiency are required. As voltage overshoots (spikes) should be minimized at the same time also the properties of the internal body diode are of importance. The MOSFETs are used both in hard- and soft-switching conditions.

Low-voltage drives running at a battery voltage of 72 V and 80 V are a second application field. Such devices are mainly used in forklifts and light electric vehicles (LEV), for example battery driven vehicles at airports and the like. In case of low-voltage drives as schematically illustrated in Fig. 4 high currents must be controlled and paralleling of devices should be easy. It is important to maintain a good thermal management and to offer a high ruggedness of the devices at a competitive price. Usually hard-switching topologies are used.

Micro inverters and power optimizers in solar applications (Fig. 5) form another major market segment. Main requirements for this application are a good reliability, a high efficiency, a high power density and a competitive pricing. Depending on the customer hard- and soft-switching topologies are found.

In addition a large number of industrial applications are found, each with varying requirements which makes it difficult to summarize the needs.

Due to the many different application fields a methodlogy is needed which helps to identify the device properties which are beneficial for all applications in order to focus on the improvement of the right device features. Such a methodology may also deliver if the device needs to be optimized in opposing directions for different applications, thereby indicating needs for technology derivatives.

Established methodologies for such an analysis are offered in general by the Quality Function Deployment [1,2]. The House-of-Quality Matrix as one part of it can be employed as an aid in determining how products live up to customer needs [3]. Fig. 6 illustrates the basic worksheet used in this process for analysing the relationship between customer wishes and product capabilities and their interactions, identifying development priorities and including a benchmarking of the new concepts against predecessor and competitor products. As the required inputs are delivered from different functional units such as marketing, engineering and manufacturing, the methodology also increases the cross-functional integration within the organization.

An example for the application of this procedure to analyse the application requirements with respect to power MOSFET development can be found in earlier work [4].
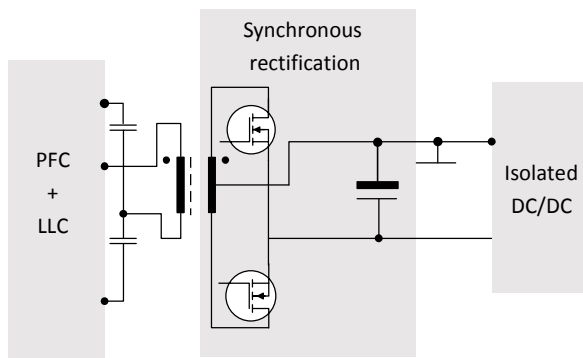

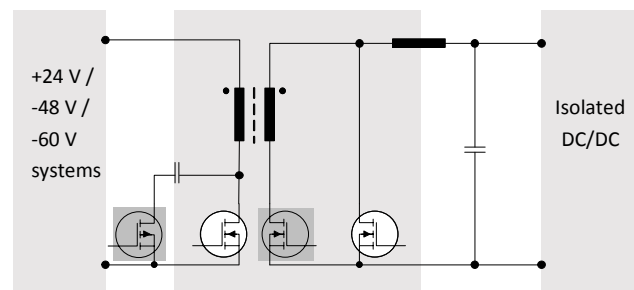Fig. 2: Synchronous rectification stage of a power supply unit

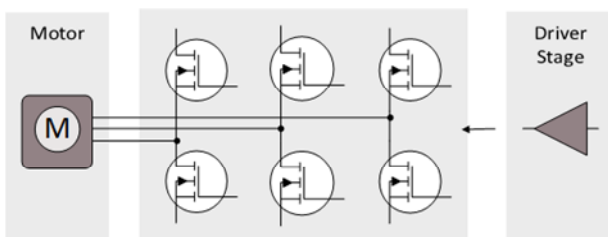Fig. 3: Isolated DC/DC brick converter

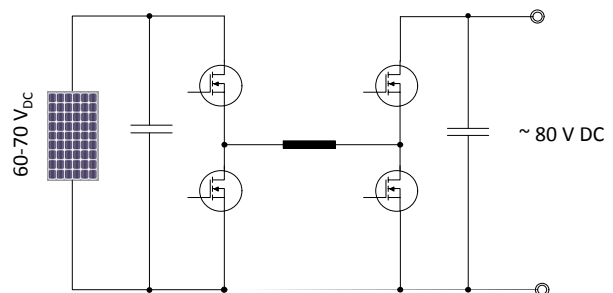Fig. 4: Low-voltage drives for forklift and LEV
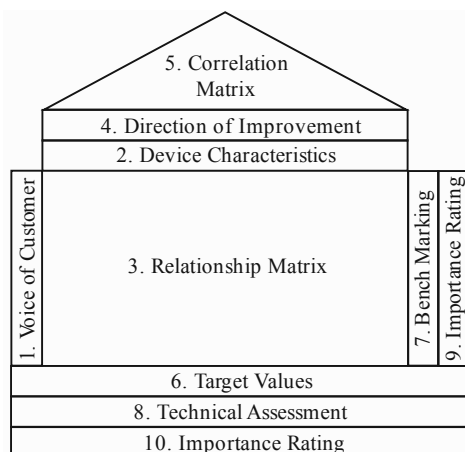

Fig. 5: Solar power optimizer

Fig. 6: House-of-Quality matrix

By help of the briefly described application requirement analysis, the optimization criteria for a 150 V MOSFET device intended to be used in the previously discussed application fields are derived. As such a suitable power MOSFET device should fulfil the following requirements:

- low on-resistance $R_{DS(on)}$
- low output charge Q_{OSS}
- low gate-drain charge Q_{GD}
- low reverse-recovery charge Q_{RR}
- high avalanche ruggedness
- wide package portfolio incl. SMD

DEVICE CONCEPT

Basics of charge-compensation using a field-plate

Low-voltage power MOSFETs based on charge-compensation using a field-plate offer a significant reduction of the area-specific on-resistance. Such devices entered the market more than 10 years ago and developed into a kind of standard technology for fast-switching devices. The basics and properties of these devices have been discussed in various details in many publications
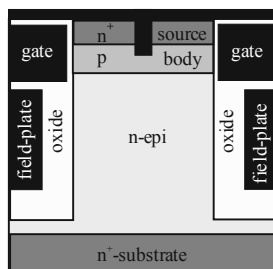

Fig. 7: Schematic cross section of a charge-compensated device using a field-plate
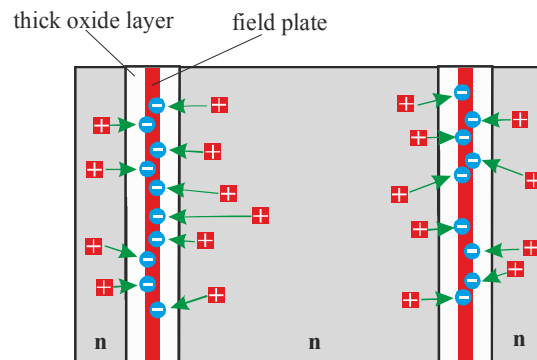

Fig. 8: Principle of charge-compensation by a field-plate

over the years, e.g [5] - [13]. Fig. 7 gives a schematic cross section of such a device.

In field-plate type devices, an isolated field-plate provides the mobile charges required to compensate the drift region donors under blocking conditions as indicated in Fig. 8. Compared to a device using a simple planar pn-junction, the electric field now also has a component in the lateral direction. Fig. 9 explains the basic differences in the electric field for a simple pn-junction and for the case where a field-plate compensates the donors in the drift region.

The application of a field-plate leads to an almost constant field distribution in the vertical direction since the ionized dopants in the drift region are laterally compensated by mobile carriers in the field-plate, thereby reducing the necessary drift region length and increasing the allowed drift region doping for a given breakdown voltage. Both contribute to the significantly reduced area-specific on-resistance. Since the field-plate electrode is connected to the source electrode of the MOSFET and the gate is formed by a separate electrode, such a device offers an outstanding area-specific on-resistance and a low gate-charge at the same time.

Directions of further device improvements

To improve the overall efficiency in most applications both on-resistance and switching losses, need to be minimized at the same time in order to meet the efficiency targets at low and medium load conditions. It was shown that those targets can be reached by the use of improved manufacturing setups linked to better process control capabilities in combination with an optimized cell structure leading to an increase of the overall efficiency level without compromising the ruggedness of the device [14].

The extension of the breakdown voltage range of devices based on the principle is without doubt very attractive, however a number of problems related to manufacturability and device characteristics impose a number of challenges.
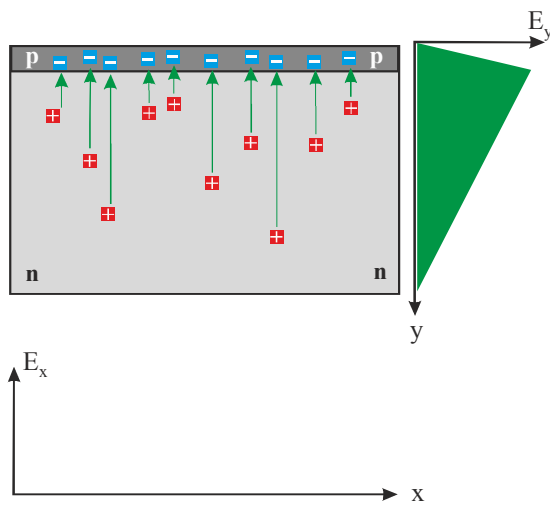
Fig. 9: a) Electric field for a pn-junction

b) Electric field for a field-plate structure

Approach 1 – additional epi layer

The targeted additional blocking capability can be realized by a second lower-doped drift region under the actual compensation structure as schematically shown in Fig. 10. This allows the reutilization of an existing cell, but the expected area-specific on-resistance will be higher as only a part of the structure is charge-compensated. Additionally such an approach may also help to avoid wafer bow issues. Fig. 11 indicates the rising wafer bow with increasing blocking voltage within a given device manufacturing technology using the field-plate approach. The wafer bow is a critical issue as above a certain limit the wafers cannot be processed anymore. The main reasons for the rise of the bow are given by the increasing trench depth and increasing field-oxide thickness. So if the wafer bow is close to the limit, the additional lower-doped drift region is an easy way to circumvent related problems while targeting higher blocking voltages.

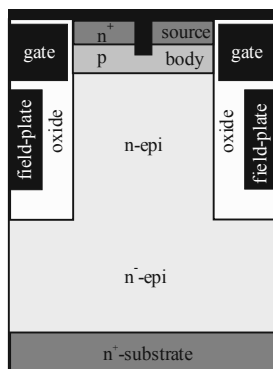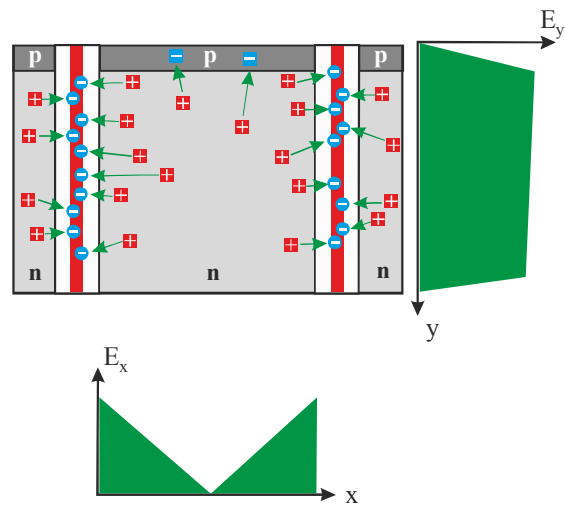However, there is still the need for some additional development effort as an appropriate edge-termination

structure is needed. Once this issue is addressed such an approach allows a comparatively fast development of different voltage classes at the cost of performance, especially at cost of area-specific on-resistance.

Approach 2 – full redesign of device

The required higher blocking capability can be achieved by an appropriate design of the device as depicted in Fig. 12. Among other measures, the trench depth as well as the thickness of the field oxide layer inside the trench must be increased. Without countermeasures, this might be linked to one or all of the following problems:

- the wafer bow will become too large for the wafers to be handled in the production facilities as already discussed
- the induced stress by the mismatch of oxide and silicon in the trench exceeds the material limits and leads to cracks as shown in Fig. 13
- the control of the trench depth which is important for an acceptable parameter tolerance becomes either

Fig. 10: Schematic cross section of a charge-compensated device with increased blocking due to an additional drift layer
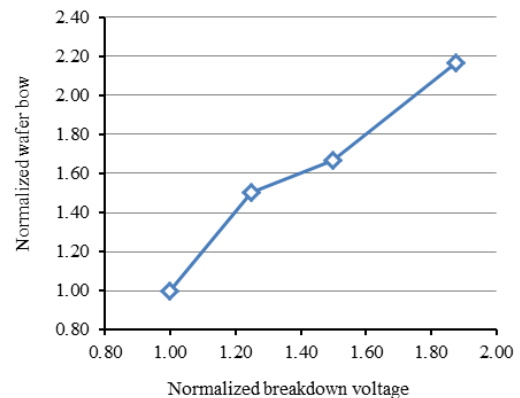

Fig. 11: Increase of wafer bow with breakdown voltage for charge-compensated devices using a field-plate
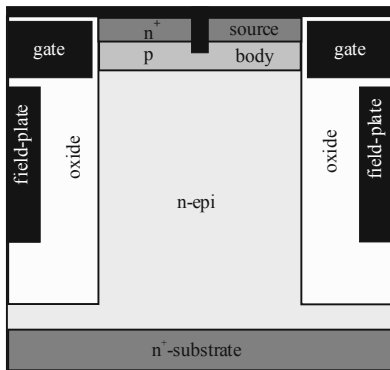
Fig. 12: Schematic cross section of a charge-compensated device designed for a higher blocking voltage

   more difficult or leads to long process times linked to higher costs

On the other hand, this device will offer the best area-specific on-resistance as the full drift-region length is compensated. As such the concept enables the best possible optimization of the device with respect to different application requirements. Obviously, any effort which was spent before to gain better control over process parameters to improve the device parameters [15] will be helpful here as well. The aforementioned problems related to wafer bow and cracks may be solved by a careful optimization of process parameters, appropriate selection of used material or even a reordering of process steps.

COMPARISON OF DEVICE PROPERTIES

For choosing the right approach it is of interest to evaluate the realized device performance on product level which includes the package contribution to the overall on-resistance of the device. The comparison presented in this work is done for fully processed devices with a nominal blocking voltage of 150 V.
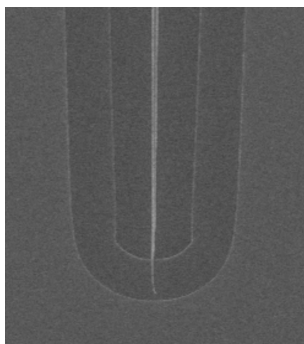

Fig. 13: Stress-induced crack through a thick oxide in the field-plate trench
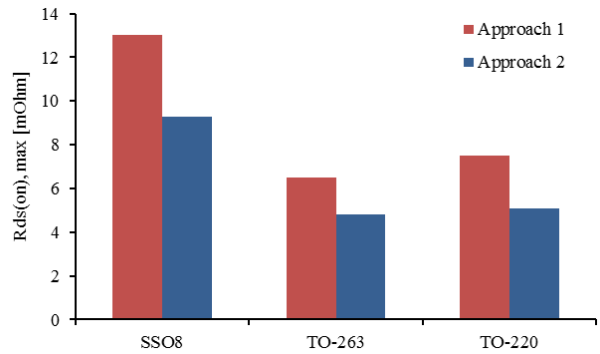

Fig. 14: Comparison of the product on-resistance of 150 V devices with respect to the discussed concept approaches

Fig. 14 compares the on-resistance in different packages. All devices are so-called best-in-class devices. This means that for each package type the largest possible chip area is used. As to be expected the devices based on a full redesign with respect to the targeted nominal blocking voltage (approach 2) show a clearly reduced on-resistance for the product.

Fig. 15 shows important figure-of-merits in order to evaluate the dynamic device properties. This comparison is important as the devices are widely used in applications where fast-switching is required and high switching frequencies are demanded. As such the better on-resistance of the device must not be compromised by a high gate-charge, a large miller capacitance or an increased output charge. The comparison is done for best-in-class devices in a SSO8 package. Also for the dynamic properties the devices based on a full redesign yield improved device parameters.

Since a good avalanche ruggedness is required by many applications it is interesting to see if there is a difference in the behaviour for the two different approaches. For this investigation, devices with different active areas were characterized. In the UIS (unclamped inductive switching) test different values of the avalanche inductor were used
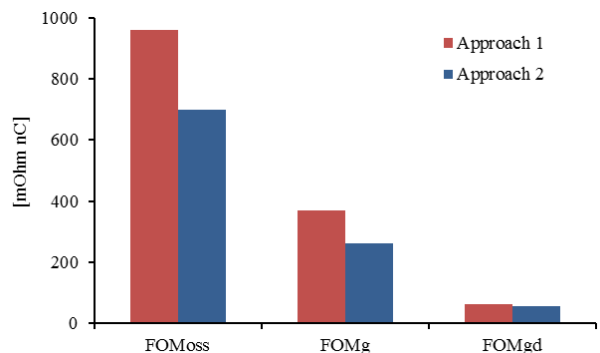

Fig. 15: Comparison of the most important figure-of-merits of best-in-class devices in a SSO8 package with a nominal blocking voltage of 150 V
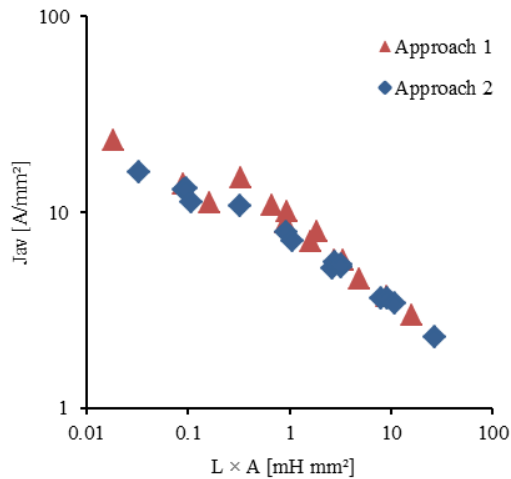
Fig. 16: Comparison of avalanche destruction current densities for devices according to approach 1 and approach 2

Fig. 17: Basic schematic of the secondary side of the power supply unit using two interleaved LLC stages

to cover a large range of current densities and test conditions. Fig. 16 gives the comparison between both device concepts and does not reveal a significantly different avalanche ruggedness.

Based on the presented numbers it can be concluded that the additional technological development effort spent on a dedicated device design for the respective voltage class is paid-off by significantly better overall device properties.

DEVICE PERFORMANCE IN APPLICATION

The improvement of the device parameters gives a clear indication that the use of the design approach 2 is advantageous. However, it is finally important how the different device properties will impact the behaviour of the real application. A lowered on-resistance can help to reduce the number of needed components which simplifies the circuitry, but also lowered voltage overshoots during the switching of the device may reduce design-in efforts or helps saving costs on the passive component size. A better efficiency may simplify the cooling concept and enable additional savings here.

Device performance in synchronous rectifier stage

Test platform. The used test board represents the AC/DC converter of a power supply using two interleaved LLC stages with 1500 W output power each. Details on the basic concept of this approach may be found in literature [16]. The switching frequencies of both stages run asynchronously, the current sharing is controlled digitally. The primary side uses a half-bridge topology. On the secondary side, where the devices under test are located, a center-tapped topology is used. The LLC uses a digital control loop with automatic compensation of the total
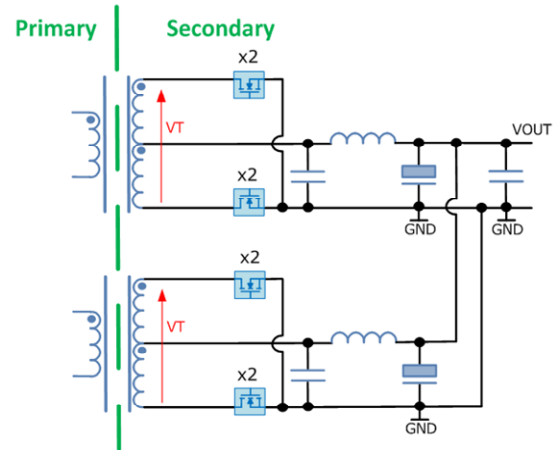
output capacitance. The DC input voltage is nominally 380 V, the output voltage is nominally 54 V and the output current is between 0 A and 55 A. The switching frequency varies in the 100 kHz range. Fig. 17 shows the basic schematic of the secondary side of the power supply for better understanding.

Test results. Fig. 18 shows the efficiency measurement for each of the two design approaches. The efficiency curves show some kinks which are related to the operation of the LLC converter with its two stages:

- the 1st kink shows up when the 2nd LLC stage gets activated
- the 2nd kink is caused by the activation of synchronous rectification in the 1st LLC stage
- the 3rd kink is due to the activation of synchronous rectification in the 2nd LLC stage
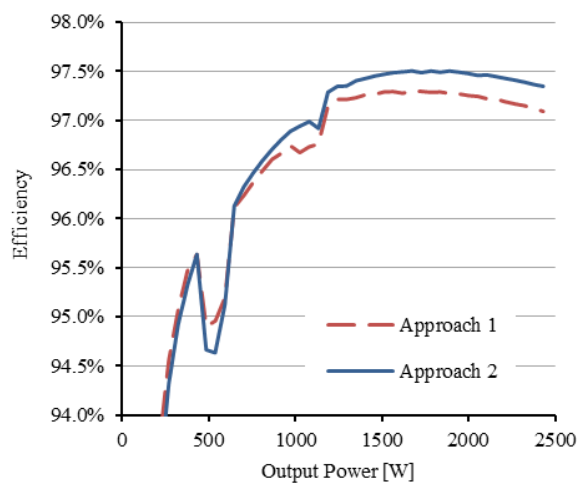

Fig. 18: Comparison of the efficiency of the AC/DC converter stage using 150 V devices of app. identical area with different design approaches
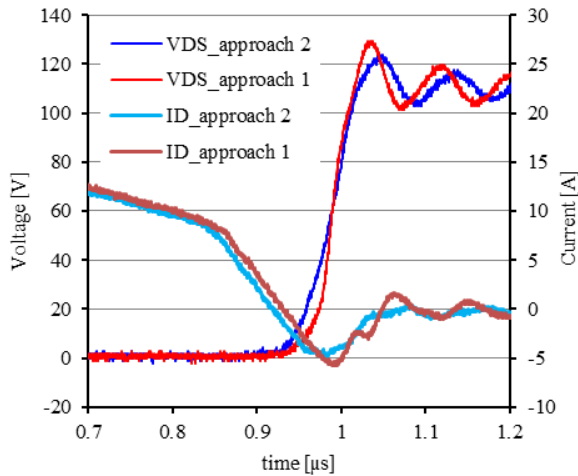
Fig. 19: Comparison of voltage overshoot due to body diode commutation using 150 V devices of identical on-resistance with different design approaches (V_{IN} = 390 V, I_{OUT} = 20 A)

The higher effort to realize the device approach 2 gives a clear benefit in this application – the peak efficiency is increased by 0.2 % while the efficiency at full load increases even by 0.25 %.

Fig. 19 indicates the voltage overshoot linked to the body diode commutation. For the device following approach 2 the voltage overshoot is reduced by 5 V while at the same time the reverse recovery current peak is smaller.

Device performance in hard-switched applications

Test platform. The test board used to assess the devices performance in hard-switched applications is a 250 W buck converter board. The board reproduces the operation of a solar power optimizer as shown in Fig. 5 being operated in buck mode, an approach being discussed in
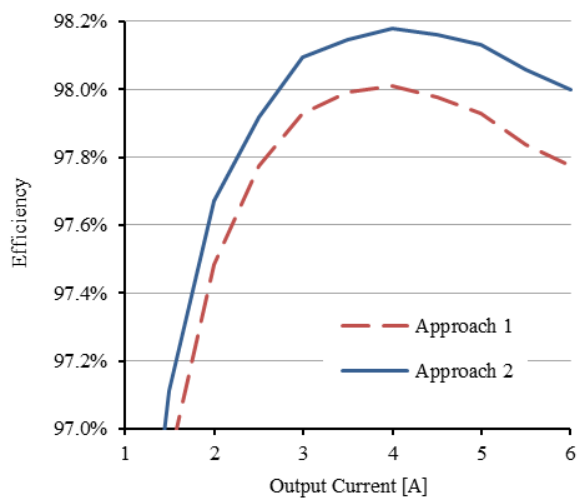

Fig. 20: Comparison of the efficiency of the buck converter using 150 V devices of app. identical area with different design approaches.
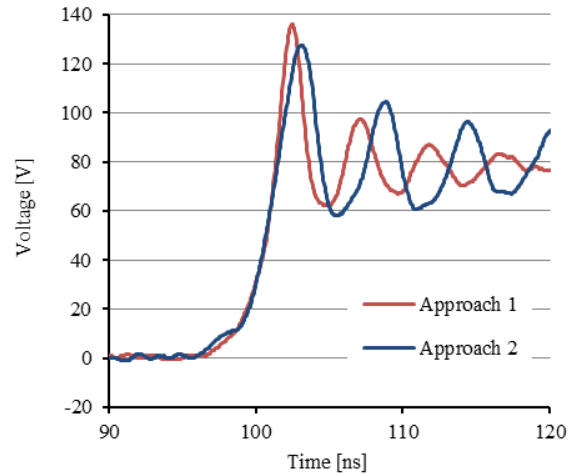

Fig. 21: Comparison of the half-bridge phase node voltage overshoot due to the body diode commutation using 150 V devices of identical on-resistance (V_{IN} = 75 V, I_{OUT} = 4 A).

more details in literature [17,18]. The input voltage is 75 V, the output voltage is 42 V and the switching frequency is 200 kHz. All switches have an identical on-resistance.

Test results. Fig. 20 shows the efficiency measurement for each of the two MOSFET design approaches. Once again, the approach 2 shows better performance even in hard-switched applications: the peak efficiency is increased by almost 0.2 % while the efficiency at full load increases slightly above it. Fig. 21 shows the voltage overshoot linked to the body diode commutation. For the device following the approach 2, the voltage overshoot is reduced by 8 V.

CONCLUSION

This article discusses two different device design approaches for extending the blocking voltage capability of low-voltage power MOSFETs based on the charge-compensation principle using a field plate. The discussed devices intend to meet the so-called medium-voltage range of 150 V – 300 V. Potential target applications include primary side switches and synchronous rectification stages of switch-mode power supplies, motor drives or solar power optimizers. Devices are used both in hard- and soft-switching topologies.

The first and simpler approach achieved the required additional blocking capability by having a second lower-doped drift region added under its actual compensation structure. This allowed the reutilization of existing cells at the expense of increased area-specific on-resistance but requires the development of a suitable edge termination structure.

The second approach is based on an appropriate design of the device. Among other measures, increased trench depth and an adapted field oxide layer thickness has been shown to meet the required blocking capability. This approach offers the best area-specific on-resistance as the full drift-region length is compensated. As such it is expected that this second design concept enables the best possible optimization of the device performance with respect to a wide range of different application requirements.

Both design concepts were compared by example of devices with a blocking voltage of 150 V. As confirmed by the presented experimental results for synchronous rectification and hard-switched applications, the second approach based on a specific design for a given voltage class delivers a better overall performance. Consequently, the higher development effort is clearly justified by the better properties and behaviour of the realized power MOSFET.

ACKNOWLEDGEMENTS

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