Simulating the Avalanche Behavior of Trench Power MOSFETs

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Abstract

The avalanche behavior of a new Trench Power MOSFET was investigated by means of measurement and electro-thermal simulation. Two different destruction regimes were identified experimentally: energy-related destruction and current-related destruction. Possible simulation approaches to account for the different effects are proposed. They are in good agreement with measured results. Furthermore, the experimentally found dependence on design parameters was also possible to predict qualitatively by means of simulation.

Keywords: MOSFET, Trench, Avalanche Ruggedness

INTRODUCTION

The industry's demand for devices with lower on-state resistance and good switching behavior continues to exist. The application fields for low-voltage devices are for example in DC-DC power supplies, AC-DC adapters as well as in Class-D amplifiers. In all these applications, atypical switching conditions, particularly high voltage peaks, can occur driving the device into avalanche mode. The aim of this work is to predict, by means of numerical simulations, the maximum avalanche current I_{as} the transistor is able to sustain. As well known, this current strongly depends on the load inductance L_{load} and decreases with increasing inductance. The on-state resistance and I_{as} are inversely proportional to each other thus a trade-off exists. To simulate this trade-off for different cell design parameter variations significantly accelerates the development process and the finding of a desired optimum.

DEVICE CONCEPT

To meet the requirements aforementioned the principle of charge balancing by means of field plates is employed in the new OptiMOS®2-family [1]. In contrast to standard trench MOS structures that exhibit a linearly decreasing electric field with a maximum at the body/drift region pn-junction, the electric field distribution employing the field plate principle is almost constant. A deep trench penetrates the whole drift region. A highly conductive region (field plate) insulated from the drift region provides mobile charges to balance the drift region donors under blocking conditions. The blocking capability is mainly determined by the insulator thickness at the trench bottom and not by the doping density in the drift region thus making it stable to process tolerances. The drift-region doping can be increased, leading to a clearly reduced on-state resistance even below the so-called "silicon limit" which is the on-state resistance of an ideal abrupt pn-junction at a given breakdown voltage not limited by termination structure.

ASPECTS OF IMPACT IONIZATION MODELS

Mobile charges (electrons, holes) are accelerated in the presence of an electric field thus gaining kinetic energy. These carriers suffer collisions with the lattice and transfer energy to the lattice. If the transferred energy is higher than a certain threshold (at least the bandgap energy) an electron hole pair (EHP) is generated.
This process of impact ionization can be regarded as inverse Auger effect [2]. Analytical considerations

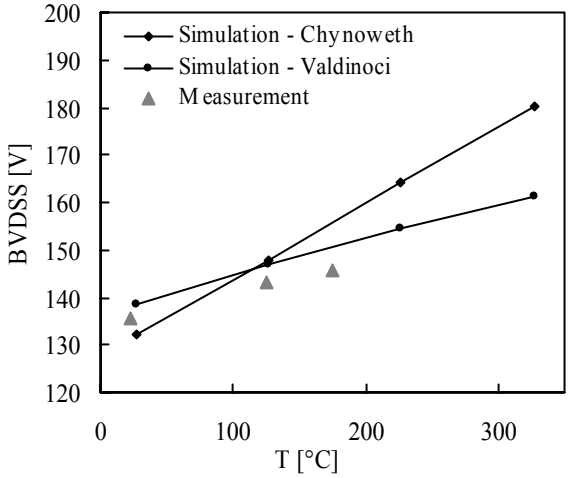

Fig.1: Measurement of BVDSS as function of temperature compared to simulated values obtained with impact ionization models of Chynoweth and Valdinoci, respectively

showed an inversely proportional dependence of ionization rate to electric field [2]:

$$\alpha \sim \exp\left(-1/E^{x}\right) \quad (1)$$

with x = 1 at low electric fields and x = 2 at relatively high electric fields [3]. Avalanche breakdown occurs if the so-called ionization integral approaches 1.
Several models have been developed to account for this effect in numerical simulations, for example [4,5,6]. The widely used Chynoweth model [5] with the parameters obtained by van Overstraeten and de Man [7] was compared to the recently proposed model by Valdinoci [8] and to experimental results. Measurements performed on manufactured devices revealed a temperature coefficient (TC) of breakdown voltage of ~0.50‰/K. As depicted in Fig. 1, Valdinoci's model delivers better temperature dependence than Chynoweth's model compared to measurement, with temperature coefficients of ~0.54‰/K and ~1.22‰/K, respectively.

MEASUREMENT SETUP

In certain applications a failure mode called unclamped inductive switching (UIS) can occur. The aim of the UIS test is to determine the maximum avalanche current the device is able to sustain. Fig. 2 shows the circuit used for the measurements and simulations.
It consists of a voltage source, an external switch, a freewheeling diode, an inductance and the device under test (D.U.T.). While the transistor is turned on (V_{GS} = 20V) and the external switch is closed, the current ramps up according mainly to the inductance and the applied voltage. After turning off the device (and at the same time disconnecting the voltage source), the energy stored in the inductance must be dissipated in the transistor. Since the current continues to flow through the inductance the transistor is forced to maintain the current. Thus it is driven into avalanche mode.
The ramping process is iterated for a higher current until the device fails. By repeating this process with different inductances the UIS behavior can be well characterized, in particular the dependence of maximum avalanche current I_{as} on load inductance in the circuit.

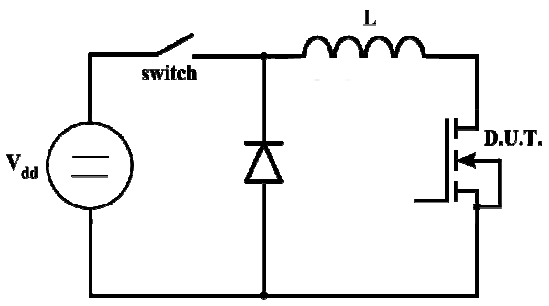

Fig. 2: Principle circuit to determine the unclamped inductive switching behavior of a transistor. The voltage source is disconnected when the transistor turns off.

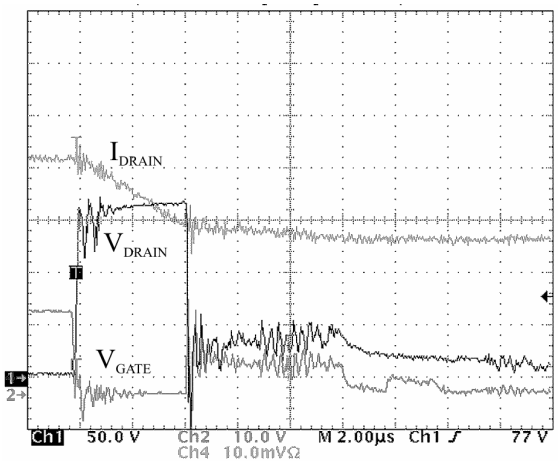

Fig. 3: Measurement of energy-related destruction. The fast decay of V_{DRAIN} indicates destruction.

DESTRUCTION MECHANISMS

The first mechanism is related to the heat dissipation capability of the device and thus will be called energy-related destruction. A typical example is shown in Fig. 3.
After the gate is turned off, the current cannot change instantaneously. To maintain the current, the device is driven into breakdown and the current decreases at a rate:

$$\frac{di}{dt} = \frac{V_{DS} - V_D}{L} \quad (2)$$

Due to the presence of a high electric field and high current density, the lattice temperature increases, as described by the heating term:

$$\frac{P_{th}}{V} = \vec{E} \cdot \vec{J} \quad (3)$$

The breakdown voltage V_{br} rises due to increased carrier-phonon interaction caused by the increase in temperature, i.e. V_{br} exhibits a positive temperature coefficient. This supports a homogenous current distribution since no filament is expected to build up. The temperature continues to rise until it gets in the vicinity of the so-called intrinsic temperature T_{int}. It is defined as the temperature at which intrinsic carrier concentration $n_i(T)$ equals background doping N_D and can empirically found to be [10]:

$$n_i(T) = 3.88 \cdot 10^{16} \cdot T^{\frac{3}{2}} \cdot \exp\left(-\frac{7000K}{T}\right) \cdot cm^{-3} \quad (4)$$

At this point, the device is not able to dissipate more energy thus if the current continues it will be destructed due to intrinsic conduction effects induced by too high a temperature. Of course, this value serves only as an upper limit. The intrinsic conduction sets in at a somewhat lower temperature thus the intrsinsic

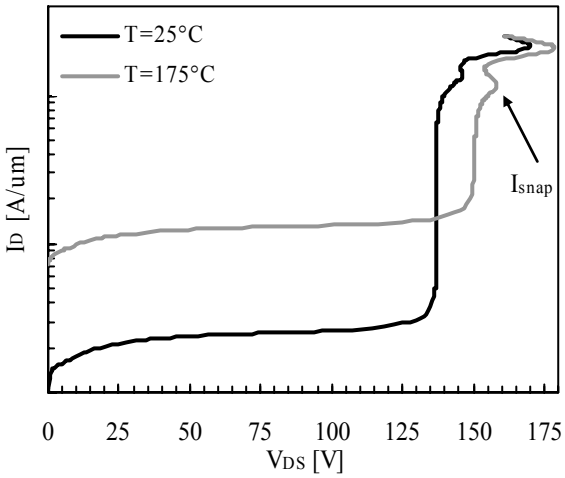

Fig. 4: Simulated breakdown curves for two different temperatures

temperature T_{int} can only be regarded as a soft limit. T_{int} can also be extracted by measuring the avalanche current I_{as} at different temperatures and for various inductances. All curves, if extrapolated, intersect the abscissa at the same point, this point being the intrinsic temperature for this particular technology Fig. 5 shows measured values and their respective extrapolation for the new trench technology (OptiMOS®2) and the planar predecessor technology (SIPMOS®) [1]. The trench technology exhibits a higher T_{int} due to a higher doping of the epitaxial layer. A narrow distribution of the avalanche current I_{as} over a large number of devices is characteristic for this mechanism.

The second mechanism that results in the destruction of MOSFET devices is called current-related destruction since it typically occurs at higher current densities. It is caused by the turn-on (latch-up) of the parasitic npn-

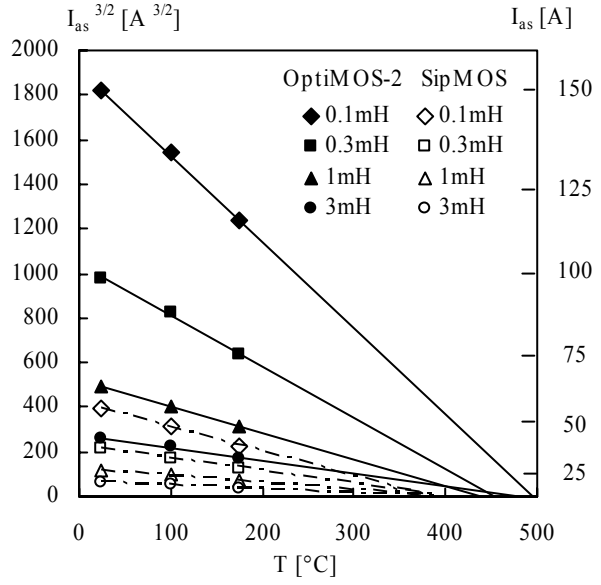

Fig. 5: Measured I_{as} for the new trench technology (OptiMOS®2), older planar technology (SIPMOS®) and respective extrapolation of intrinsic temperature.

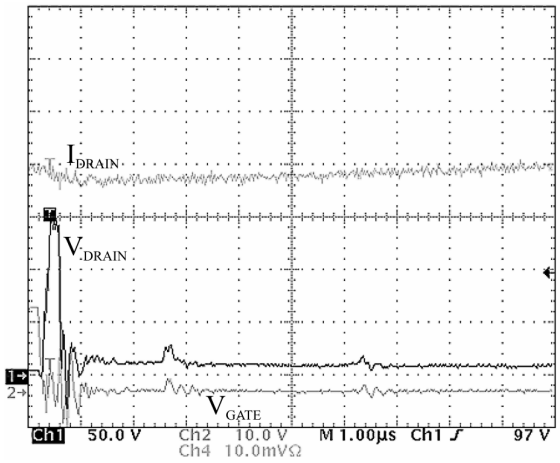

Fig. 6: Measurement of current-related destruction. The short time to destruction is apparent.

transistor. The holes generated by impact ionization flow through the p-body region of the n-channel MOSFET thus creating a potential drop in the base region of the parasitic bipolar transistor. If this potential drop exceeds the built-in potential of the base-emitter diode the parasitic BJT will turn-on, i.e. latch-up. Since a BJT has a negative temperature coefficient of breakdown voltage latch-up is self-amplifying, thus the current concentrates on a small region of the device. Fig. 6. depicts a current-related destruction behavior of a device. The short transient time (<<1µs) until the device is destroyed indicates a different mode than energy-related destruction. A rather broad distribution of measured I_{as} over large number of devices is characteristic for this mechanism.

The breakdown characteristics for two different temperatures can be seen in Fig. 4. A region with negative differential resistance (NDR) does exist and causes the voltage to decrease. This snapback effect is related to the second breakdown of the MOSFET. The current at which this snapback occurs shall be defined as snapback current I_{snap}. It does not only depend on the temperature but also on cell design as was determined experimentally and outlined in the next section. Furthermore, the voltage starts to increase again thus confining the region of NDR to certain current values.

EXPERIMENTAL RESULTS

Three different device types A, B and C were used to investigate the influence of structural variations on

	A	B	C
Measured I_{as}	22.5A	56.8A	64.5A
Simulated I_{as}	46.5A	58.4A	60.0A

Tab. 1: Comparison of measurements and simulation results for devices with different cell designs at L_{load} = 10µH.

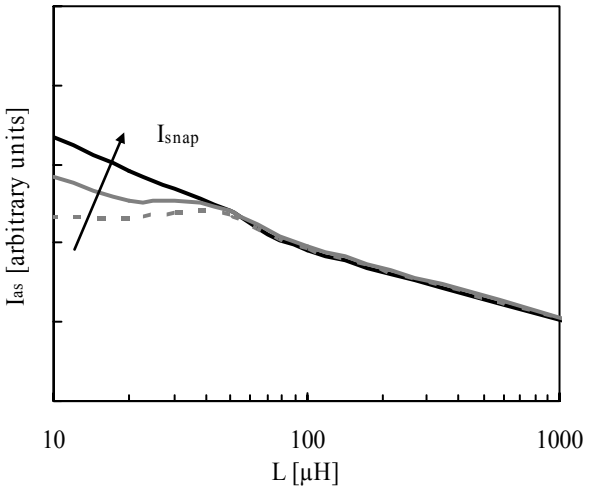

Fig. 7: Measurement results indicating the relation between snapback current I_{snap} and avalanche current I_{as} for smaller inductances

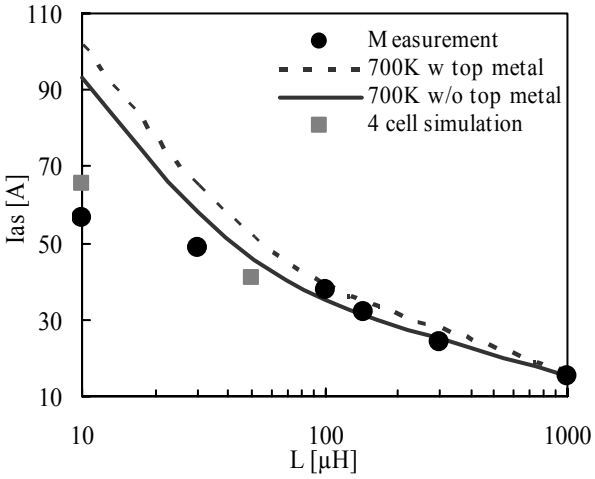

Fig. 8: Measurement and simulation of avalanche behaviour showing two different destruction regimes and simulation results obtained with two different approaches

device performance with $I_{snapA} < I_{snapB} < I_{snapC}$. The measurement and simulation results are summarized in Tab. 1. Measurements showed a significant influence of the snapback current I_{snap} on the avalanche current I_{as} for inductances smaller than $L_{load} = 50\mu H$ as can be seen in Fig. 7.
Concerning larger inductances, the devices sustain basically the same current, regardless of device type thus an energy-related destruction mechanism is dominant. Two approaches to simulate the different destruction mechanisms will be discussed in the next section.

SIMULATION RESULTS

Device simulations including the solution of the heat transport equation were performed using the 2D device simulator MEDICI [9]. We used two different simulation methods to determine the transient unclamped inductive switching behavior:

- single cell simulation
- monolithical integration of (2 or more) cells in one structure

All simulations were performed according to Fig. 2. The maximum lattice temperature T_{max} reached in the device during the transient was extracted. We defined a destruction limit $T_{max} = T_{int}$, with $T_{int} = 700K$. This value was determined experimentally as explained in the last section (Fig. 5). A thermal electrode was placed on top of the device and ideal heat flow was assumed ($R_{th} = 0$). Due to the short pulse times no thermal electrode at the bottom part (backside) was necessary. The influence of the top metal layer deposition on the heat dissipation was also accounted for. Reflecting boundary conditions were used in all simulations.

Energy-Related Destruction

Single Cell simulations proved to be sufficient to predict the behavior under UIS conditions if energy-related destruction is dominant. The transient behavior was simulated for different initial current values until $T_{max} = 700K$. Fig. 8 compares measurement and simulation results of the avalanche current for different inductances $I_{as} = f(L_{load})$. Obviously, the experimentally chosen value for the intrinsic temperature $T_{int} = 700K$ in simulation leads to good simulative prediction of avalanche current I_{as}. The graph also shows the influence of the top metal layer. Analytical 1d approximations revealed a dependence of avalanche current I_{as} on inductance L_{load} as follows:

$$I_{as} \propto L_{load}^{-\frac{1}{3}} \tag{5}$$

whereas simulation yields an exponent of app. -0.39. The transition region between the two different destruction mechanisms is at $L_{load} = 80\mu H$. For smaller inductances (higher currents) the results obtained by means of single cell simulations deviate significantly from measurements. This led us to the assumption that another destruction mechanism is dominant and cannot be described by single cell simulations. A different approach became necessary and will be outlined in the next section.

Current-Related Destruction

Fig. 9 shows the maximum temperature T_{max} as function of initial current with a load inductance $L_{load}=10\mu H$ for a single cell and four cells monolithically integrated for device types A, B and C. The curves obtained with the single cell approach are identical. However, the results for four cells show significant differences. They all show an increase in temperature indicating effects of current concentration as will be discussed later.

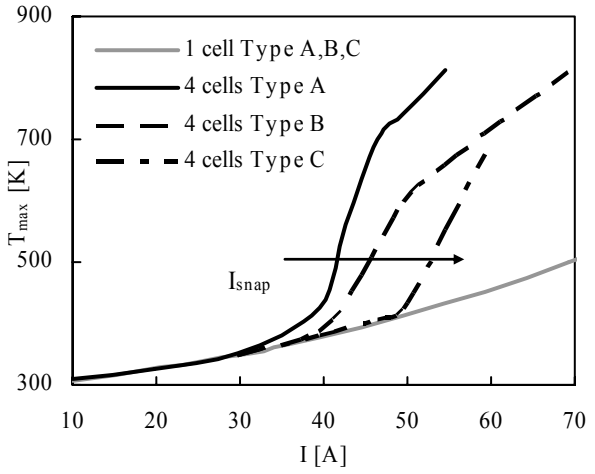

Fig. 9: simulated maximum temperature over current in single cell simulation and in four cell simulations with L=10µH

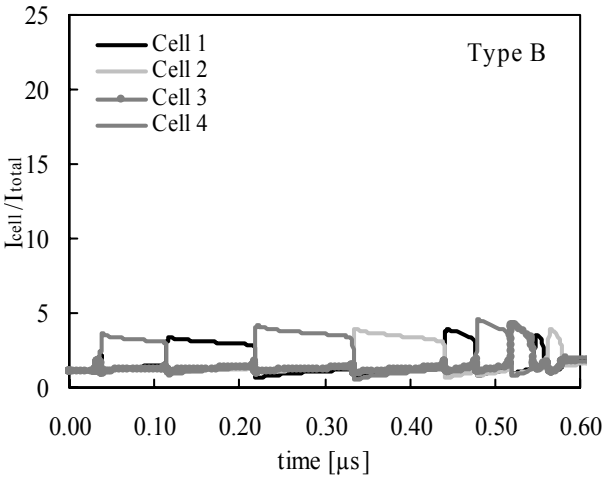

Fig. 11: Type B: Simulated normalized currents of four cells extracted at trench bottom with I_{as} = 20A and L_{load} = 10µH. The differences in cell current are large (more than factor 15)

The onset of this effect obviously depends on the structure. If again an intrinsic temperature of T_{int} = 700K is considered as criterion for destruction, the maximum current is 46.5A for type A, 58.4A for type B and 60A for type C, respectively. The metallization also leads to a difference of app. 7A as can be seen in Fig. 8 and is accounted for in the obtained simulation results.
At low applied currents, the current is evenly distributed over the cells. If the applied current is increased, the current concentrates to one cell but then starts to "oscillate". This was also observed in planar structures, but only at much higher temperatures [11]. The effect is shown for device types B and A in Fig. 10 and Fig. 11, respectively. Shown are the maximum cell currents, extracted at the trench bottom, normalized to the total device current. The current crowding effects are obviously more pronounced (by a factor 3) for structures with lower snapback current I_{snap}. The device is destructed, i.e. exceeds an intrinsic temperature of T_{int} = 700K, if the filament does not move about any more but rather sticks to one cell which occurs for higher currents. In reality, this effect is expected to be even stronger as a real device consists of a very large number of cells. The oscillation sets in when certain cells of the device array must support a current higher than their respective snapback current I_{snap}. If these cells leave the zone with NDR due to current crowding or self-heating, the current is able transfer to another cell.

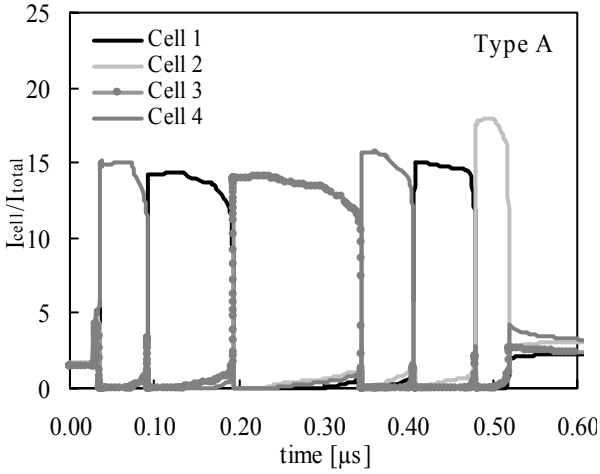

Fig. 10: Type A: Simulated normalized currents of four cells extracted at trench bottom with I_{as} = 20A and L_{load} = 10µH . The differences in cell current are small (less than factor 5)

CONCLUSION

We examined the unclamped inductive switching behavior of Trench Power MOSFETs. Measurements of the maximum sustainable avalanche current as function of load inductance revealed different destruction regimes.
The first one is solely related to the heat dissipation capability of the device and occurs at relatively large inductances greater than 100µH. A good agreement between measurement and simulation results was achieved.
For current-related destruction, dominant at smaller inductances, simulations incorporating four cells yielded qualitatively good results. The destruction mechanism strongly depends on cell design and shows effects of current crowding.
Further work is necessary to achieve quantitatively good results. This includes the influence of thermal resistance and metallization as well as further investigation of other device parameter variations.

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