Experimental Study and Simulations on Two Different Avalanche Modes in Trench Power MOSFETs

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Abstract

The avalanche behaviour of a new trench power MOSFET was investigated with the help of measurement and electro-thermal device simulation techniques. Two different destruction regimes were identified experimentally: Energy-related destruction and current-related destruction. Possible simulation approaches to account for the different effects were proposed. The corresponding results agreed well with measurements. Furthermore, simulation qualitatively predicted the experimental results' dependence of avalanche behaviour on design parameters.

1 Introduction

There is an ongoing demand for devices with lower on-state resistance and good switching behaviour. For example, low-voltage devices are found in DC-DC power supplies, AC-DC adapters, and Class-D amplifiers. The operating frequency in such systems incorporating transistors with a high switching speed may be limited by external circuits, especially as a result of stray inductances. At turn-off, the energy stored in these inductances needs to be dissipated, for example by entering the avalanche mode [1]. Furthermore, atypical switching conditions can occur, particularly high-voltage peaks, driving the devices into the avalanche mode. The aim of this work is to predict, by means of numerical simulations, the maximum avalanche current I_{as} that a transistor in one of these circuits is able to sustain. It is well-known that this current strongly depends on the load inductance L_{load} and decreases with increasing inductance. The on-state resistance R_{on} and avalanche current I_{as} are inversely proportional to each other; thus a trade-off exists. To simulate this trade-off for different cell-design parameter variations significantly accelerates the development and optimization process.

2 Device Concept

To meet the aforementioned requirements, the principle of charge balancing by means of field plates is employed in the new OptiMOS®2-family [2].

Charge balancing for power MOSFETs was introduced in commercially available products in 1998 with the 600 V CoolMOS™ Technology [3]. The basic principle behind the drastic reduction of specific on-resistance R_{ON}·A compared to conventional power MOSFETs is the compensation of n-drift-region donors by acceptors located in p-columns, as shown schematically in Fig. 1a. The compensating acceptors are located in lateral proximity to the drift-region donors, in contrast to a large vertical distance at which the acceptors are positioned in the body region. In addition, the acceptors are evenly distributed over the total drift-region length, in contrast to a strong localization in the body region, which leads to a very homogeneous electric field distribution over the entire voltage-sustaining region. The requirement for precise lateral n- and p-dose compensation limits the n-drift region doping. Therefore, this kind of compensation is typically used in power MOSFETs with breakdown voltages of several hundred Volts.

For breakdown voltages below 200 V, field-plate trench MOSFETs are an excellent alternative [2]. A deep trench penetrates the whole drift region. A highly conductive region (field plate) insulated from the drift region provides mobile charges to balance the drift-region donors under blocking conditions, as shown in Fig. 1b. Therefore, precise lateral drift-region compensation is ensured under all operating conditions. The field-plate isolation has to withstand the full source drain blocking voltage of the device at the trench bottom; therefore oxide thicknesses in the micron range have to be regulated carefully with a special focus on avoiding thinning at the bottom trench corners and preventing generation of stress-induced defects. The blocking capability is mainly determined by the insulator thickness at the trench bottom and not by the doping density in the drift region, thus making the blocking voltage stable to process tolerances. The drift-region doping can be increased, leading to a clearly reduced on-state

resistance even below the so-called “silicon limit,” which is the on-state resistance of an ideal abrupt pn-junction at a given breakdown voltage not limited by termination structure.

3 Aspects of Impact Ionisation Models

Mobile charges (electrons, holes) are accelerated in the presence of an electric field, thus gaining kinetic energy. These carriers collide with the lattice and hence transfer energy to the lattice. If the transferred energy is higher than a certain threshold (at least the bandgap energy) an Electron Hole Pair (EHP) is generated.

This process of impact ionisation can be regarded as an inverse Auger effect [4]. Analytical considerations show an exponential dependence of ionisation rate on electric field strength [4]:

$$\alpha \sim \exp\left(-1/E^{x}\right) \tag{1}$$

with $x = 1$ at weak electric fields and $x = 2$ at relatively strong electric fields [5]. Avalanche breakdown occurs if the so-called "ionisation integral" approaches 1.

Several models [6,7,8] have been developed to account for this effect in numerical simulations. The widely used Chynoweth model [7] with the parameters obtained by van Overstraeten and de Man [9] was compared to the recently proposed model by Valdinoci [10] and to experimental results. Measurements performed on manufactured devices revealed a temperature coefficient (TC) of breakdown voltage of ~0.50 ‰/K. As depicted in Fig. 2, Valdinoci's model delivers better temperature dependence than Chynoweth's model when compared to measurements, with temperature coefficients of ~0.54 ‰/K and ~1.22 ‰/K, respectively.

4 Measurement Setup

In certain applications, a failure mode called Unclamped Inductive Switching (UIS) can occur. The aim of the UIS test is to determine the maximum avalanche current the device is able to sustain under these conditions. Fig. 3 shows the structure of the circuit used for the measurements and simulations.

It consisted of a voltage source V_{dd}, an external switch, a freewheeling diode, a load inductance L_{load} and the Device Under Test (DUT). When the transistor was turned on (V_{GS} = 20 V) and the external switch was closed, the current ramped up in proportion to the inductance and the applied voltage. After turning off the DUT, the energy stored in the inductance $E = \frac{1}{2} \cdot L \cdot I^2$ had to be dissipated in the transistor. A special control circuit made sure that at the same time, V_{dd} was disconnected by opening the external switch. Since the current continued to flow through the inductor and could not change instantaneously, the transistor was forced to maintain the current. Thus it was driven into the avalanche mode.

The ramping process was repeated for higher currents until the device failed. Failure was detected by a rapid decay of breakdown voltage. By repeating this process with different inductances, the UIS behaviour could be well characterized, in particular the dependence of maximum avalanche current I_{as} on load inductance L_{load} in the circuit.

5 Destruction Mechanisms

The first mechanism is related to the heat-dissipation capability of the device and thus will be called energy-related destruction. A typical example is shown in Fig. 4.

After the gate is turned off, the current cannot change instantaneously. To maintain the current, the device is driven into breakdown and the current decreases at a rate described by Equation (2) with breakdown voltage V_{br}:

$$\frac{di}{dt} = -\frac{V_{DS} - V_D}{L} \approx -\frac{V_{DS}}{L} \approx -\frac{1.3 \cdot V_{br}}{L} \tag{2}$$

Due to the presence of electric field and high current density, the lattice temperature increases, as described by the Joule heating term that can be derived from inspection of the Poynting vector [11]:

$$\frac{P_{th}}{V} = \vec{E} \cdot \vec{J} \tag{3}$$

The breakdown voltage V_{br} rises due to increased carrier-phonon interaction caused by the increase in temperature, i.e. V_{br} exhibits a positive temperature coefficient. This supports a homogenous current distribution since no filament is expected to build up. The temperature continues to rise until it approaches the so-called intrinsic temperature T_{int}. This temperature is defined as the temperature at which the intrinsic carrier concentration $n_i(T)$ equals the background doping value N_D, which can empirically found to be [12]:

$$n_i(T_{int}) = 3.88 \cdot 10^{16} \cdot T_{int}^{\frac{3}{2}} \cdot \exp\left(-\frac{7000K}{T_{int}}\right) \cdot cm^{-3} = N_D \tag{4}$$

At this point, the device is not able to dissipate more energy, so if the current continues to flow, the device will be destroyed due to intrinsic conduction effects induced by too high a temperature. Of course, this value serves only as an upper limit. The intrinsic conduction sets in at a somewhat lower temperature; thus the intrinsic temperature T_{int} can only be regarded as a soft

limit. The intrinsic temperature T_{int} can also be extracted by measuring the avalanche current I_{as} at different temperatures and for various inductances. All curves, if extrapolated, intersect the abscissa at the same point, which is the intrinsic temperature for this particular technology. Fig. 5 shows measured values and their respective extrapolation for the new 100 V trench technology (OptiMOS®2), and the earlier planar 100 V technology (SIPMOS®) [2]. The trench technology exhibits a higher intrinsic temperature T_{int} due to a higher doping of the epitaxial layer (cf. Eqn. 4). A narrow distribution (small standard deviation) of the avalanche current I_{as} over a large number of devices is characteristic for this mechanism.

The functional relationship between avalanche current I_{as} and several parameters such as inductance L, temperature difference $\Delta T = (T_j - T_{start})$, breakdown voltage $V_{br,}$ and pulse length t_{as} can be derived if the solution of the 1D heat diffusion equation is taken into consideration. Assuming a rectangular power pulse with an average power $P = \frac{1}{2} \cdot V_{br} \cdot I_{as}$ yields [13]:

$$\Delta T \propto \frac{1}{A_{chip}} \cdot V_{br} \cdot I_{as} \cdot \sqrt{t_{as}} \tag{5}$$

Under the assumption $\frac{di}{dt} = \text{const}$, and considering the circuit in Fig. 3, the pulse length t_{as} can be calculated to:

$$t_{as} = \frac{I_{as} \cdot L}{V_{br}\left(1 - \frac{V_{dd}}{V_{br}} - \frac{V_D}{V_{br}}\right)} \tag{6}$$

Inserting Eqn. (6) into Eqn. (5) gives the relationship of avalanche current I_{as} for L = const :

$$I_{as} \propto A_{chip}^{\frac{2}{3}} \cdot \Delta T^{\frac{2}{3}} \cdot L^{-\frac{1}{3}} \cdot V_{br}^{-\frac{1}{3}} \cdot \left(1 - \frac{V_{dd}}{V_{br}} - \frac{V_D}{V_{br}}\right)^{\frac{1}{3}} \tag{7}$$

If the voltage source V_{dd} is disconnected during UIS and with V_D being the forward voltage drop of the diode in Fig. 3, the last term in Eqn. (7) changes to $\left(1-\frac{V_D}{V_{br}}\right)^{\frac{1}{3}}$. With $V_D << V_{br}$ this term can be neglected.

The second mechanism that results in the destruction of MOSFET devices is called current-related destruction since it typically occurs at higher current densities. It is caused by the turn-on (latch-up) of the parasitic npn-transistor. The holes generated by impact ionisation flow through the p-body region of the n-channel MOSFET, thus creating a potential drop in the base region of the parasitic bipolar transistor. If this potential drop exceeds the built-in potential of the base-emitter diode, the parasitic BJT will turn on, i.e. latch-up. Since a BJT has a negative temperature coefficient of breakdown voltage, latch-up is self-amplifying, thus concentrating the current on a small region of the device. Fig. 6. depicts the current-related destruction of a device. The short transient time ($<< 1$ μs) until the device is destroyed indicates a different mode than energy-related destruction. A rather broad distribution (large standard deviation) of measured avalanche currents I_{as} over a large number of devices is characteristic of this mechanism, because of doping variations and thus variations in the built-in potential of the parasitic bipolar transistor.

The simulated static breakdown characteristics for two different temperatures can be seen in Fig. 7. A region with Negative Differential Resistance (NDR) does exist and causes the voltage to decrease. This snapback effect is related to the second breakdown of the MOSFET. The current at which this snapback occurs is defined as snapback current I_{snap}. It depends on the temperature as well as on cell design, as determined experimentally and outlined in the next section. Furthermore, the voltage starts to increase again at higher current levels, thus confining the region of NDR to certain current values.

6 Simulation and Measurement Results

Device simulations including the solution of the heat transport equation were performed using the 2D device simulator MEDICI [14]. We used two different simulation methods to determine the transient unclamped inductive switching behaviour:

- Single-cell simulation
- Monolithic integration of (2 or more) cells in one structure

All simulations were performed using a circuitry according to Fig. 3. The maximum lattice temperature T_{max} reached in the device during the transient was extracted. We defined a destruction limit $T_{max} = T_{int}$, with intrinsic temperature $T_{int} = 700$ K. This value was determined experimentally (Fig. 5). A thermal electrode was placed at the bottom side of the device (drain), and ideal heat flow was assumed ($R_{th} = 0$). Due to the relatively short pulse times, a thermal resistance at the drain showed no influence on temperature behaviour. The influence of the top metal layer thickness on avalanche current I_{as} and variation of intrinsic temperature T_{int} was investigated as well. Having no thermal electrode on the top of the device imposed a worst-case scenario because no heat flow could take place through the top. Reflecting boundary conditions were used in all simulations.

6.1 Device overview

Device types A, B, and C were used to investigate the influence of structural variations on device performance with snapback currents $I_{snapA} < I_{snapB} < I_{snapC}$. The devices differed in the manner the epitaxial layers were processed, with A = Epitaxy Variation 1, B = Epitaxy Variation 2 and C = Epitaxy Variation 3. It will be shown that different epitaxial layers strongly influenced the avalanche behaviour.

The measurement and simulation results are summarized in Table 1. Measurements at room temperature showed a significant influence of the snapback current I_{snap} on the avalanche current I_{as} for inductances smaller than L_{load} = 50 µH, as can be seen in Fig. 8.

At larger inductances, the devices sustained basically the same current regardless of device type; thus an energy-related destruction mechanism was dominant.

6.2 Energy-related Destruction

First, the influence of top metal layer thickness d_{Metal} and different maximum lattice temperatures T_{max} on simulated avalanche current I_{as} was investigated. The top metal layer thickness d_{Metal} had the greatest impact for small inductances, that is short transients. The avalanche current I_{as} increased monotonically with top metal thickness d_{Metal} and maximum lattice temperature T_{max}, as shown in Fig. 9.

Single-cell simulations proved to be sufficient to predict the behaviour under UIS conditions if energy-related destruction is dominant. The transient behaviour was simulated for different initial current values until maximum lattice temperature T_{max} = 700 K. Fig. 10 compares measurement and simulation results of the avalanche current for different inductances revealing a functional dependence $I_{as} = f(L_{load})$. Obviously, the experimentally chosen value for the intrinsic temperature T_{int} = 700 K in simulation led to good simulative prediction of avalanche current I_{as}. As shown in Eqn. 7, analytical 1D approximations revealed a dependence of avalanche current I_{as} on inductance L_{load} as follows:

$$I_{as} \propto L_{load}^{-\frac{1}{3}} \tag{8}$$

whereas simulation yielded an exponent of app. -0.39. Similar results were obtained in [15], but neglecting deviations for smaller inductances. The transition region between the two different destruction mechanisms was about at a load inductance L_{load} = 80 µH. For smaller inductances (higher currents), the results obtained by means of single-cell simulations deviated significantly

from measurements. This led us to the assumption that another destruction mechanism was dominant that could not be described by single-cell simulations. A different approach became necessary.

6.3 Current-related Destruction

Fig. 11 shows the maximum temperature T_{max} as function of initial current with a load inductance L_{load} = 10 µH for a single cell and four cells monolithically integrated for device types A, B and C. The curves obtained with the single-cell approach are identical. However, the results for four cells show significant differences. They all show an increase in temperature, indicating effects of current crowding.

The onset of this effect depended on the structure. If again an intrinsic temperature of T_{int} = 700 K was considered as the criterion for destruction, the simulated maximum current was 46.5 A for type A, 58.4 A for type B and 60 A for type C, respectively. The metallisation also led to a difference of approximately 7 A (Fig. 9), which was accounted for in the simulation results.

At low applied currents, the current is evenly distributed over the cells. If the applied current is increased, the current concentrates on one cell but then starts to "oscillate." This was also observed in planar structures, but only at much higher temperatures [16]. The effect is shown for device types A and B in Fig. 12 and Fig. 13, respectively. Shown are the maximum cell currents, extracted at the trench bottom, normalized to the total device current. The current crowding effects are obviously more pronounced (by a factor 3) for structures with lower snapback current I_{snap}. The device is destroyed, i.e. exceeds an intrinsic temperature of T_{int} = 700 K, if the filament does not move about any more but rather sticks to one cell, which occurs for higher currents. In a real device, this effect is expected to be even stronger, as a real device consists of a very large number of cells. The oscillation sets in when certain cells of the device array must support a current higher than their respective snapback current I_{snap}. These cells reach a higher temperature than the other ones do. If the temperature difference among cells is too high, the maximum

current transfers to a cell with lower temperature. This cell in turn heats up faster due to higher current density. If the temperature gets too high again, the current filament moves again.

Yet, in some cases (e.g. Type A) there is a great discrepancy between measurements and simulation results. This suggests the existence of other effects not accounted for in the present modeling approaches. Currently under investigation are effects of asymmetric switching, including the influence of parasitic elements in the external circuitry. Furthermore, it continues to be a demanding task to quantitatively predict the actual device's behaviour with numerical simulations, since every simulation model is based on simplifications. Our main goal was to explore the main effects that determine the avalanche behaviour.

7 Conclusion

We examined the Unclamped Inductive Switching (UIS) behaviour of trench power MOSFETs. Measurements of the maximum sustainable avalanche current as function of load inductance revealed different destruction regimes.

The first one was solely related to the heat-dissipation capability of the device, and occured at relatively large inductances (greater than 100 μH). A good agreement between measurement and simulation results was achieved.

For current-related destruction, dominant at smaller inductances, simulations incorporating four cells yielded qualitatively good results. The destruction mechanism strongly depended on cell design and showed effects of current crowding. The proposed simulation approach is not limited to a distinct technology but is applicable to other technologies as well.

Detailed investigations of other device parameter variations have to be done to better understand the underlying processes that lead to destruction. A very important goal will be the determination of avalanche current capability by merely investigating the static isothermal behaviour of the transistors.

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Figures

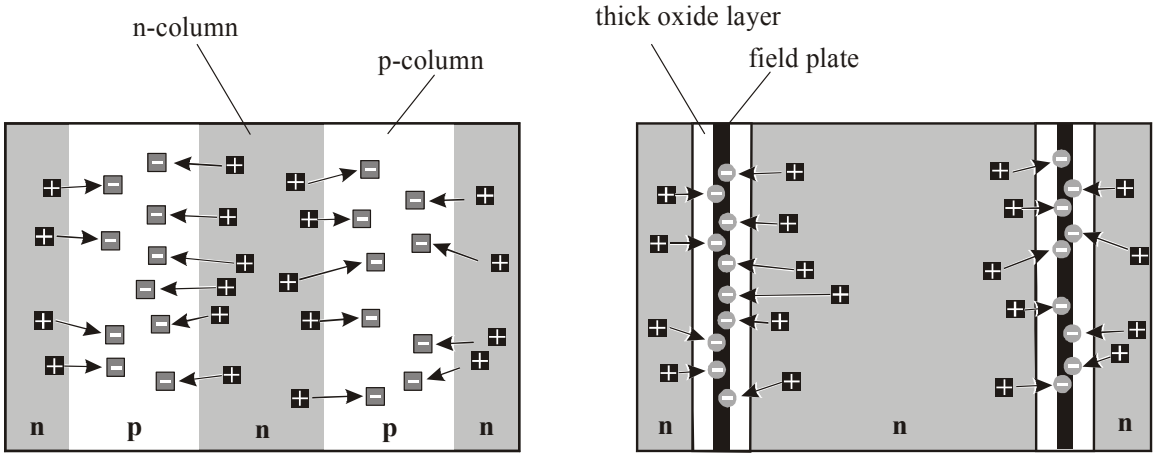

Fig. 1: a) Compensation by p- and n-columns (left)

b) Compensation using a field-plate structure (right)

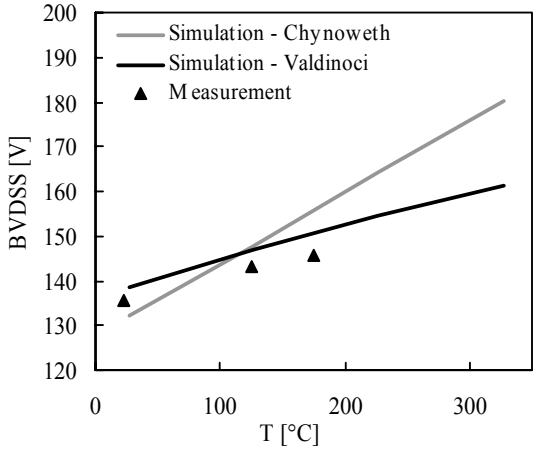

Fig. 2: Measurement of breakdown voltage BVDSS as function of temperature compared to simulated values obtained with impact ionization models of Chynoweth and Valdinoci, respectively

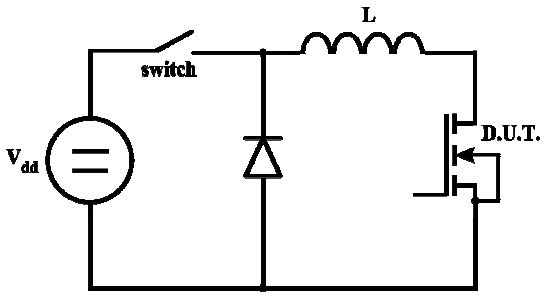

Fig. 3: Circuit to determine the unclamped inductive switching behaviour of a transistor. The voltage source is disconnected when the transistor (D.U.T) turns off.

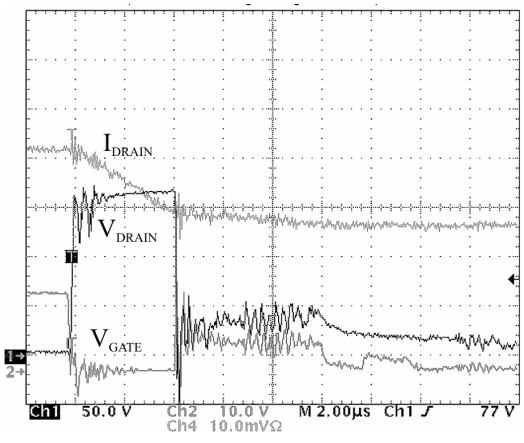

Fig. 4: Measurement of energy-related destruction. The fast decay of V_{DRAIN} indicates destruction.

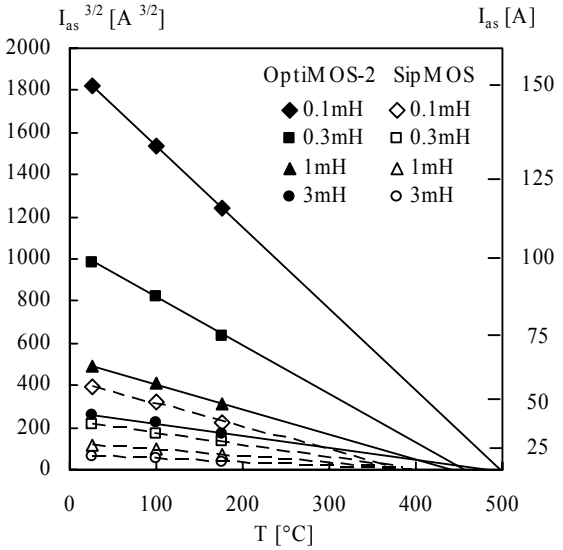

Fig. 5: Measured avalanche current I_{as} for the new trench technology (OptiMOS®2), older planar technology (SIPMOS®), and respective extrapolation of intrinsic temperature.

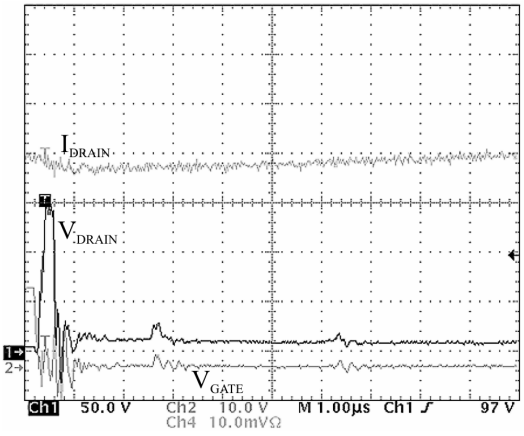

Fig. 6: Measurement of current-related destruction. The short time to destruction is apparent.

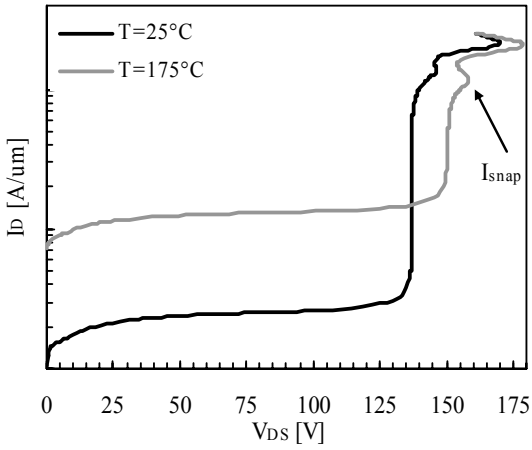

Fig. 7: Simulated breakdown curves for two different temperatures

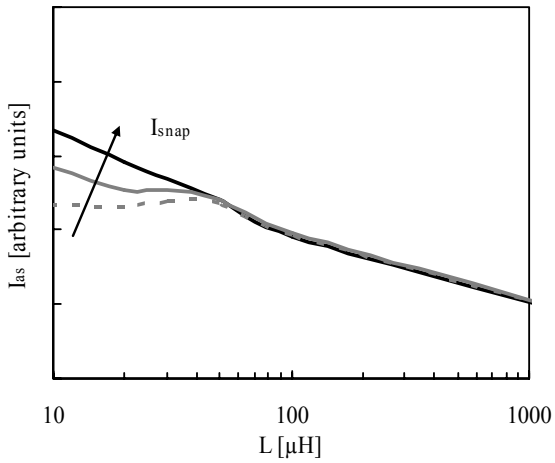

Fig. 8: Measurement results indicating the relation between snapback current I_{snap} and avalanche current I_{as} for smaller inductances

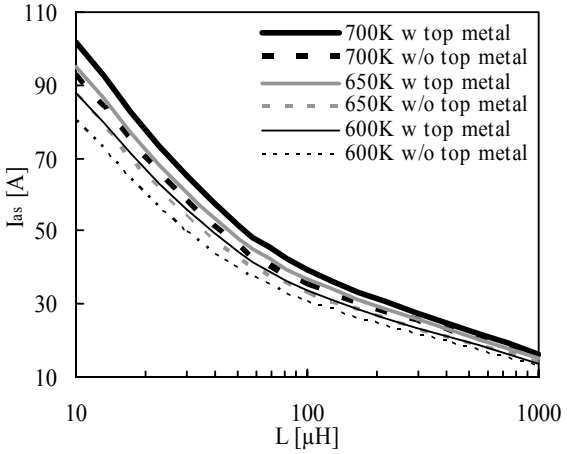

Fig. 9: Simulations indicating the influence of different values of maximum temperatures inside cells with and without a top metal layer. The influence of top metal layer thickness d_{Metal} is highest for small inductances.

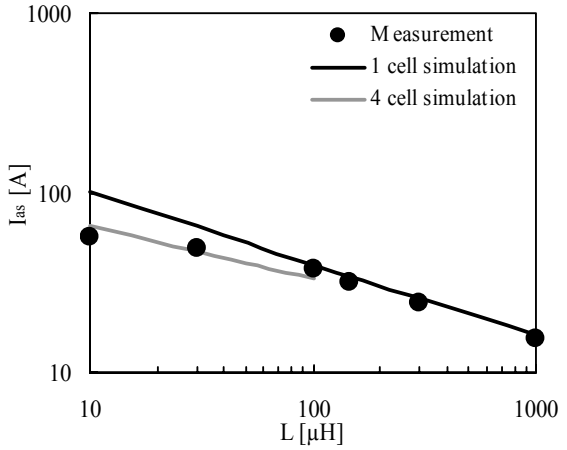

Fig. 10: Measurement and simulation of avalanche behaviour indicating two different destruction regimes and simulation results obtained with two different approaches.

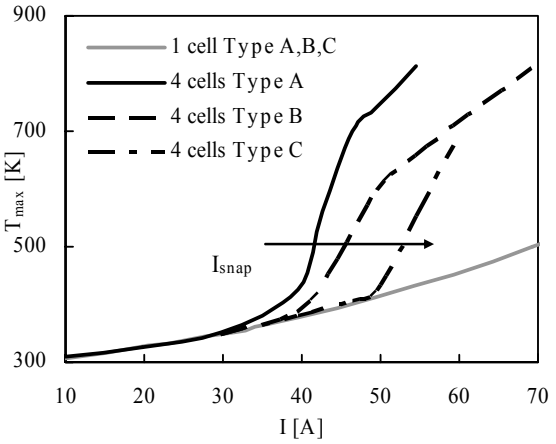

Fig. 11: Simulated maximum temperature over current in single-cell simulation and in four-cell simulations with L_{load} = 10 µH

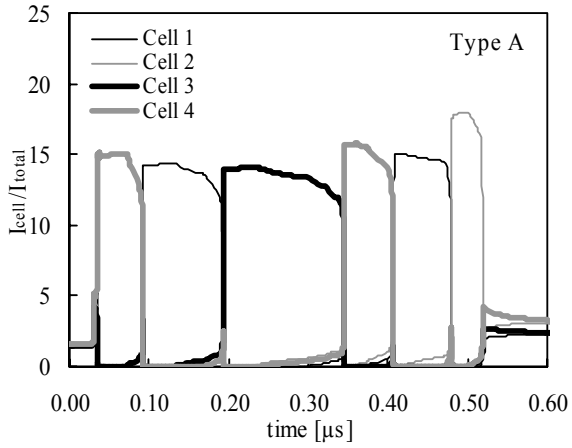

Fig. 12: Type A: Simulated normalized currents extracted at trench bottom of four cells with I_{as} = 20 A and L_{load} = 10 µH . The differences in cell current are large (more than a factor of 15)

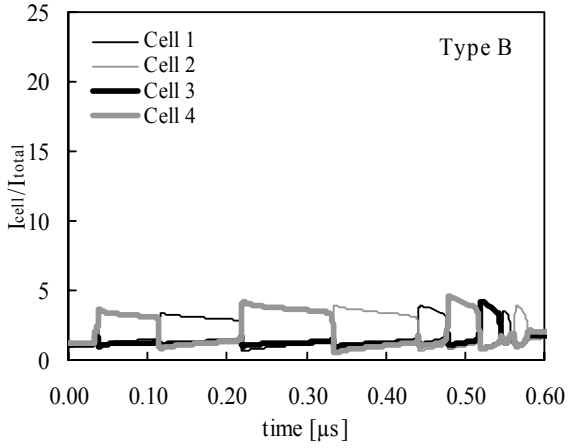

Fig. 13: Type B: Simulated normalized currents extracted at trench bottom of four cells with I_{as} = 20A and L_{load} = 10µH. The differences in cell current are small (less than a factor of 5)

Tables

	A	B	C
Measured I_{as}	22.5 A	56.8 A	64.5 A
Simulated I_{as}	46.5 A	58.4 A	60.0 A

Table 1: Comparison of measurements and simulation results for devices with different cell designs at L_{load} = 10 μH at room temperature.