Avoidance of RF Plasma Extraction Transit-Time Oscillations using 3D EMC Simulation – Chances and Limits

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Abstract

3D EMC simulation, based on the solution of the Maxwell Equations, is used for the characterisation of power modules with respect to possible resonance points. It is shown that under certain conditions RF oscillations may occur during the turn-off of the single power device chips which are related to the plasma extraction transit-time (PETT) effect. 3D EMC simulation is used to investigate changes of the power module layout which result in a shift of the resonance point of the power module and therefore effectively suppress the unwanted RF oscillations.

1 Introduction

Pett (plasma extraction transit time) oscillations are high-frequency oscillations which may occur in the tail phase of the turn-off of bipolar power devices. This phenomenon became more important with relevance regarding EMC issues recently [1], but the effect itself is already known for a certain time [2]. Pett oscillations were found in power modules with paralleled IGBT chips [1], but they also occur in modules with paralleled freewheeling diodes (FWD) or even in case of single IGBT chips [3]. Recent work shows that these oscillations should be avoided due to their adverse influence regarding EMC issues [4].

The analysis of this type of oscillation brings evidence that the occurrence of this effect is related to complex dependencies between the power semiconductor devices as well as the parasitic elements in power module interconnections [5]. In this work, the mechanism of the origin of the pett oscillation is explained. The complete power module is characterised by means of 3D EMC simulation to find resonance points which are necessary preconditions for the occurrence of the pett oscillation. Changes in the module layout are proposed and their influence with respect to resonance points is investigated.

2 Experimental Setup

2.1 Devices

For investigations concerning pett oscillations, especially set-up experimental power modules provided by SEMIKRON were used. The ratings of both module types, GAR (high-side switch) and GAL (low-side switch), are given in table I. In these devices, two freewheeling diodes (FWD) as well as two IGBTs are either paralleled in one group at one DCB (direct copper bonding) substrate, while again two groups are paralleled in one module to gain the desired current capability. Figure 1 shows the equivalent schematics as well as the layouts of the two modules.

2.2 EMC Measurement Setup

The permissible limit as well as the measuring method for ISM equipment (includes industrial, scientific and medical but excludes, for instance, telecommunication or information technology equipment, traction drives, equipment with electric drives etc. – in these cases, additional standards have to be taken into account) are defined by the European standard EN55011 (international standard IEC CISPR 11) [6]. This standard was taken into account for the EMC measurements, but according to the objective target of the measurements some changes were applied:

- The measurements were done in a usual, unshielded lab because of the high effort for transportation of the whole equipment needed for the transient characterisation of fast-switching, high-voltage power devices. Therefore, the so-called environmental electromagnetic emission caused by typical emission sources such as mobile phones, broadcast, computers etc. has to be considered and is shown in the measurement

- The distance between D.U.T. and antenna is reduced to 3m instead of 10m
- The measurements were taken in a frequency range of 200MHz-3GHz instead of 30MHz-1GHz

Figure 2 shows the basic configuration for the EMC measurements. For the measurements we used a logarithmic-periodical antenna manufactured by EMCO, Model 3147, and a Rohde&Schwarz spectrum analyser, Model ESPI3.

3 Simulation Model

3.1 Device Simulation

For device simulation, the 1D system ADIOS is used [7]. ADIOS solves the common semiconductor equations and further considers recombination centres which arise from the use of carrier lifetime control techniques. In case of the investigations done in this work, this becomes important since the FWDs of the power modules are CAL diodes (Controlled Axial Lifetime). The properties of CAL diodes are strongly improved by irradiation-generated recombination centres for carrier lifetime control which implies the use of an extended recombination model in device simulation. The properties of the relevant recombination centres were determined in previous work [8,9].

For the simulation of the reverse recovery process, the diode structure was switched from forward conduction state to the reverse voltage via a time-dependent resistor. The time-dependence of the resistor was chosen to be as similar to an IGBT turn-on characteristic as possible.

3.2 EMC Simulation System

The analysis of the power modules was performed using the 3D EMC Simulator FLO/EMC [10]. The system solves the complete Maxwell equations:

$$rot\vec{E} = \frac{-\delta\vec{B}}{\delta t} = -j\omega\,\mu\vec{H} \tag{1}$$

$$rot\vec{H} = \vec{J} + \varepsilon\frac{\delta\vec{E}}{\delta t} = \kappa\vec{E} + j\omega\,\varepsilon\vec{E} \tag{2}$$

$$div\vec{D} = \rho \tag{3}$$

$$div\vec{B} = 0 \tag{4}$$

FLO/EMC uses a Transmission Line Matrix (TLM) for an efficient solution in the time domain. In the TLM method, space is divided into cells which are modelled as the intersection of orthogonal transmission lines. The simulation proceeds in time from an initial field or voltage excitation. Voltage pulses are transmitted and scattered at each cell, the electric and magnetic fields are calculated from voltages and currents on the transmission lines at each time step.

FLO/EMC offers the possibility to apply an excitation at several ports inside the model. For the characterisation of the power modules, the excitation in form of a delta pulse was applied across a freewheeling diode. In this way can be calculated the scattering parameters, namely the input impedance [10]. There is no possibility to include real semiconductors into FLO/EMC. Therefore, a simplified model is used which reproduces the correct junction capacitance (FWD) or on-state resistance (IGBT) of the devices.

Figure 3 shows the complete 3D-Model of a characterised power module, a 1.2kV/600A high-side switch GAR, including the simulation grid provided for the calculations presented in this work.

4 The Mechanism of Pett Oscillation

Figure 4 shows the measurement of a pett oscillation which occurs during the turn-off of the power module GAR. Since the oscillation can not be measured directly, an antenna was used to detect the electromagnetic field generated by the oscillations. It is also possible to find this effect in device simulation. Figure 5 shows the simulation using ADIOS [7] of the turn-off of a single FWD under a condition where pett oscillations occur.

The mechanism of the pett oscillation is related to the mechanism of the baritt diode [11]. In difference to baritt devices, the punch-through condition is not fulfilled here. Instead, the carrier injection into the space charge region is caused by the stored excess carriers in the remaining plasma in the device during the turn-off process as it is shown schematically in case of a freewheeling diode in figure 6 [1]. The holes, flowing with the drift velocity v_d and having the density,

$$p = \frac{j}{q \cdot v_d} \tag{5}$$

will increase the effective doping to,

$$N_{eff} = N_D + p \tag{6}$$

Consequently, the gradient of the electrical field dE/dw is changed. The discontinuous flow of the holes in form of packets causes an increase in the dE/dw in the location of the packet and a decrease in the remaining part of the middle zone as to be seen in fig. 6. This results in a small negative resistance for the transition of a carrier packet. In a simplified view, oscillations occur if this negative differential resistance is larger than all other positive resistances in the complete circuit. The oscillation frequency is in the range of the large-signal frequency of the baritt diode which is given by [12],

$$f_T \approx \frac{3 \cdot v_d}{4 \cdot w_{sc}} \tag{7}$$

w_{sc} giving the space charge region width of the semiconductor device and v_d the drift velocity of the carriers. It is important to note, that the phase shift of the generated ac current plays an important role whether oscillations may occur or not depending on the resulting active power will excite or attenuate the RF power. Unfortunately, an exact analytical description is very difficult [1].

Oscillations will only occur if there is a resonance circuit, formed by the junction capacitance and an inductance mainly caused by the bond wires, whose resonance frequency has to be in the order of the transit frequency f_T (eq.7) The onset of this oscillation further depends strongly on external parameters such as temperature (which considerably influences the value of the carrier drift velocity) or voltage. It should be noted that pett oscillations will not occur as long as the number of remaining excess carriers remains very large as it is in the beginning of the turn-off process. At this time the hole current flow through the SCR remains large, consequently the impedance of the SCR is low. Under this condition, no negative differential resistance is found which prevents the onset of pett oscillations.

In the simulation in figure 7, the hole density is shown along the vertical axis for several points in time. From figure 7, the cycling of carrier packets is clearly indicated. The hole concentrations found in the simulation are reasonably larger compared to the electron concentrations which gives evidence to the hole extraction from the remaining excess carriers stored at the nn^+-junction of the device [5]. Nevertheless even the number of the drifting holes is rather low in this process, which gives an explanation of the small amplitude of this oscillation.

The occurrence of pett oscillations depends on a wide number of parameters. The carrier drift velocity v_d is sensitive to the temperature and the electric field strength E as well.

The effective width of the space-charge region w_{sc} mainly depends on the applied voltage. The number of the remaining stored excess carriers depends on the forward current density while the carrier removal process is strongly influenced by the current change in time di/dt which again depends on a number of parameters (gate resistor applied to IGBT, stray inductances etc.). Due to the high frequencies, which are related to the power device structure, pett oscillations are more likely to occur in modules realising low parasitic inductances between the semiconductor chips.

The resonance frequency of the parasitic LC circuit also depends on a number of parameters. The inductance arising from the bond wires depends on length, diameter, material and number of the bond wires. The capacitance of the power device is governed by the active area and the width of the space-charge region showing the already addressed dependencies. Furthermore, the inductive and capacitive parasitics of the power module itself, depending on the chosen layout, are from some influence.

5 EMC Compatibility Issues

Pett oscillations were observed in the high-side switch GAR. The oscillations occur in the tail current as shown in figure 4. Figure 8 gives the comparison of EMC measurements of both module types as well as the environmental measurement.

The Pett oscillation during the turn-off of GAR causes two sharp peaks in the frequency spectrum, appearing at 700MHz and 1.4GHz, respectively, which could be assigned to the fundamental frequency and the second harmonic. The emitted power is relatively small, but app. 15dB larger than the signals found by turning off the low-side switch GAL. Although the spurious radiation caused by Pett oscillation is rather low, an exceeding of the EMC limits may easily occur. Especially, this is expected if more than one power module is used - the typical case in power electronic equipment.

5 EMC Simulation Results

5.1 Unchanged Power Module

The unchanged power module GAR was characterised using 3D EMC simulation. Figure 9 shows the layout of one of the two FWD groups in detail. Figure 10 shows the simulation results for the impedance (as seen from the FWD where the excitation was applied to) of the power module GAR as shown in figure 1. The module has a resonance point at a frequency of about 700MHz which is in accordance with the oscillation frequency as given by the transit-time of the FWD. This resonance point is a necessary condition for the appearance of pett oscillation. 3D EMC simulation can be employed to predict resonance points.

Figure 11 shows the calculated impedance for the module GAL. Although pett oscillations do not occur in this power module, a resonance point in the same frequency range as in case of the module GAR is found. Therefore, an existing power module resonance point in the range of the transit-time frequency of the semiconductor does not necessarily result in pett oscillations. The comparison of both of the modules shows that the current path in the power module GAL is different from the current path in module GAR. Thus, the location of the time-variable RF current might be significantly different in both modules. This effect is not considered in FLO/EMC, because only a voltage pulse can be used for the excitation of the simulation model. Nevertheless the different RF current path might result in a damping of the complete circuit and therefore might prevent the occurrence of the oscillation in the module GAL.

For a reliable prevention of the occurrence of pett oscillations, the resonance point of the power module should be different from the transit-time frequency of the power semiconductor. Chances for a realization are given by changes in the module layout or by changing the parasitic inductance formed by the bond wires.

5.2 Influence of bond wires

As first, two of the bond wires are removed as shown in figure 12. Due to the increase of the total inductance of the bond wires, the resonance point is shifted towards a lower frequency (see figure 13). Consequently, an increased number of bond wires should result in a lower inductance and therefore in a higher resonance frequency.

An obvious and efficient way for realising a low inductance is given by providing additional shorts between the anode contact areas as shown in figure 14. This results in a clear suppression of the module resonance (figure 15) and is in accordance with comparable results published previously [2].

Figure 16 shows another module variation, where additional bond wires are applied to one FWD. As to be seen in figure 17, this is much less efficient compared to the application of direct connecting bond wires.

Another alternative is to provide additional bond wires to both of the FWDs, which are connected via a separate small area of the DCB as shown in figure 18. Here it is observed that the resonance point shifts to a frequency of approximately 900MHz (see figure 19). The area which connects the bond wires might also be connected with the anode area of the DCB without noteworthy changes in the impedance over the frequency.

5.3 Influence of Power Module Layout

Another question is how the impedance of the module depends on the capacitance which is formed by the module itself.

For this investigation, a part of the copper metallization of the DCB carrying the FWDs is separated. Figure 20 shows the resulting layout in detail. According to the simulation

results, the separation of a part of the copper area of the DCB does not cause any significant change of the resonance point (see figure 21). Moreover, also the complete removal of the whole area does not show any effect. This means, that the capacitance provided by the DCB areas takes almost no influence on the resonance frequency.

As a last example, figure 22 shows a module with a completely changed layout. This layout allows to double the number of the bond wires and therefore to clearly decrease the inductance. It is expected that the resonance point shifts towards higher frequencies. The EMC simulation shows that the changed layout now results in an increased number of resonance points, shown in figure 23. The device properties are substantially deteriorated.

6 Conclusion

High-frequency transit-time oscillations in bipolar power semiconductor devices may occur during the tail current phase of the turn-off process. The oscillations investigated in this work are caused by carrier packets extracted from the remaining excess carrier region. These carrier packets are transported through the already formed space-charge region and result in oscillations due to interaction with parasitic LC circuits. Resonance frequency of the power module and transit-time of the carriers have to match to effect oscillations. To prevent the occurrence of plasma extraction transit-time oscillations, the resonance point of the power module must be different from the transit-time frequency governed by the power device structure. In general, chances for an avoidance of this effect are given by a change in the parasitic inductance formed by the bond wires, by a changed active area of the power semiconductor itself or by changes in the power module layout.

The use of a 3D EMC simulation tool for the analysis of the complete power module itself provides a means for detecting the resonance frequency and allows to incorporate improvements to the module layout. Although not all effects can be considered by such simulations, the occurrence of pett oscillations is reliably prevented if the resonance point, found in simulation, differs from the transit-time frequency of the power device.

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Tables

Table I: Device Overview

Device	Type	Nominal Current	Nominal Voltage
GAR	High side switch	600A	1200V
GAL	Low side switch	600A	1200V

Figures

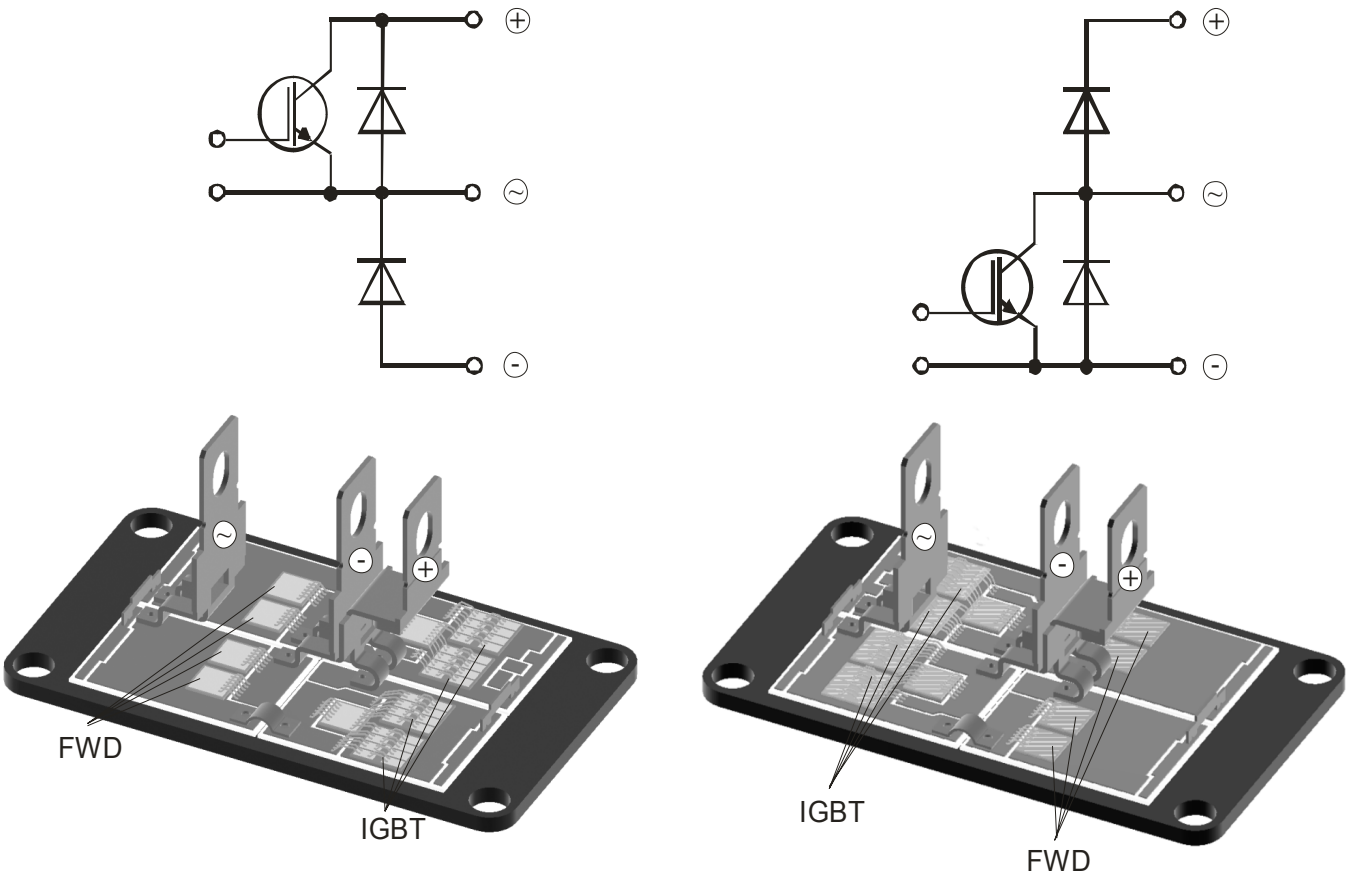

Figure 1: Internal circuit and layout of investigated power modules:

a) High-side switch GAR (left)

b) Low-side switch GAL (right)

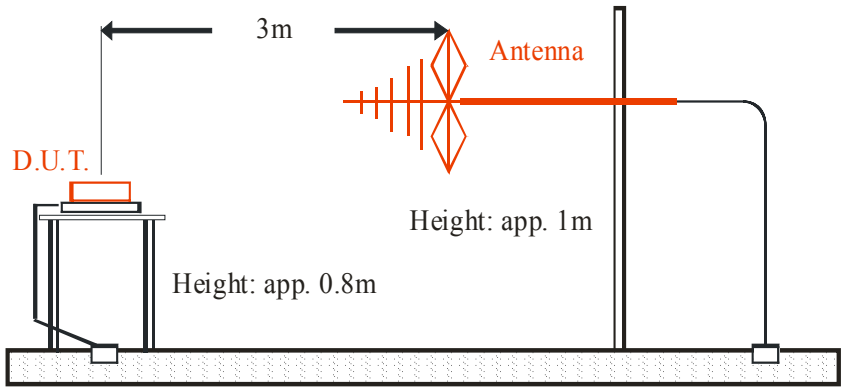

Figure 2: EMC measuring configuration

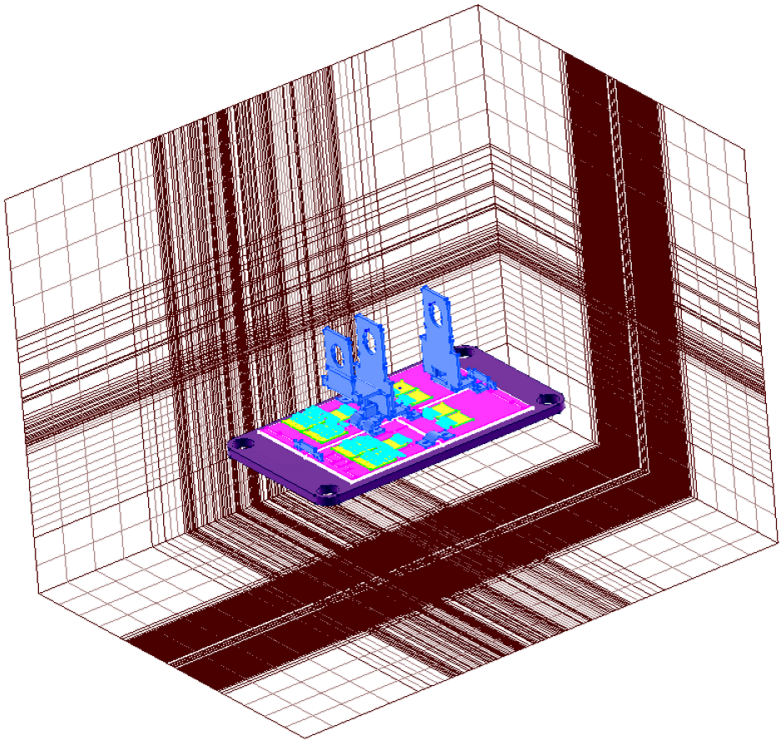

Figure 3: Grid for 3D EMC Simulation

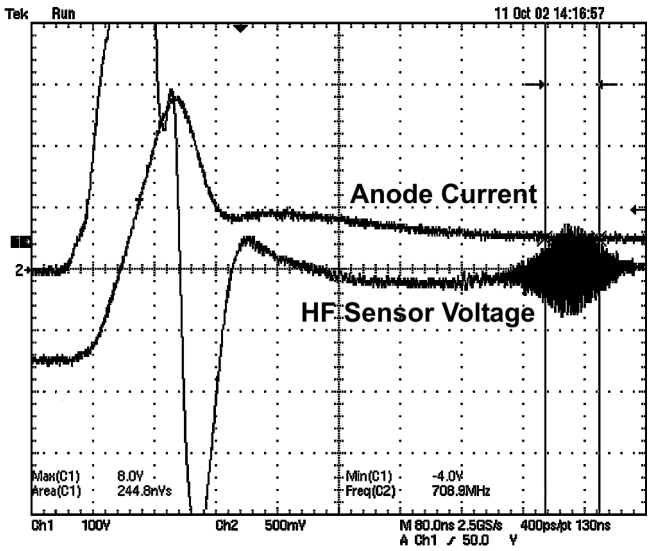

Figure 4: Measurement of a pett oscillation in power module GAR (V_R=600V, I_F=200A, di/dt=4000A/µs, T=300K)

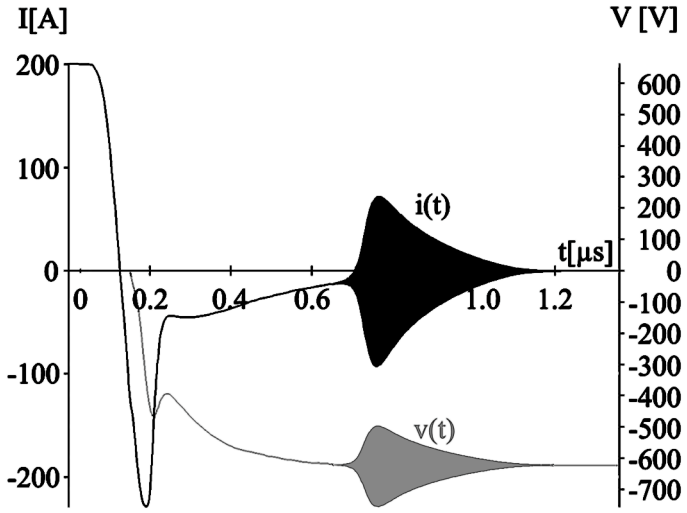

Figure 5: Pett oscillation as result of device simulation with ADIOS [7]

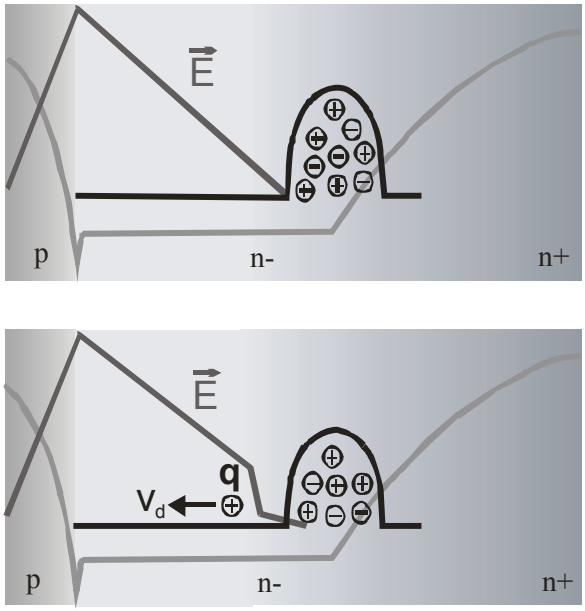

Figure 6: Origin of pett oscillation due to hole carrier extraction out of a region with high carrier density

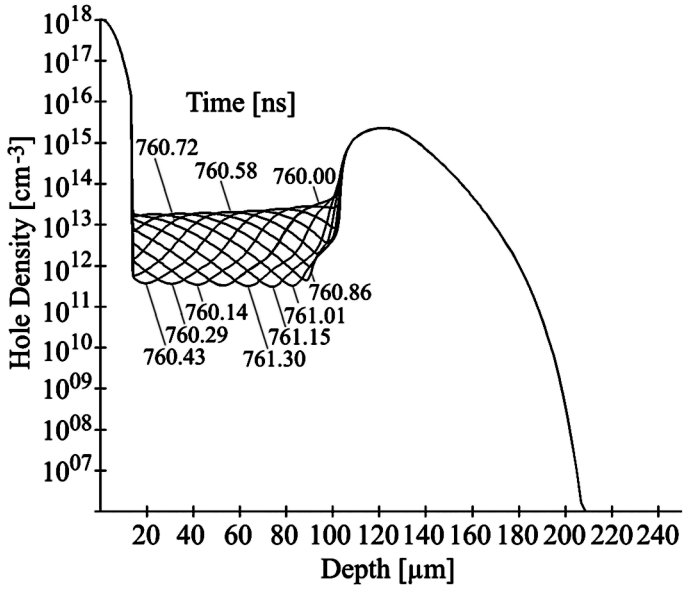

Figure 7: Hole density along vertical axis at different points in time (ADIOS simulation [7])

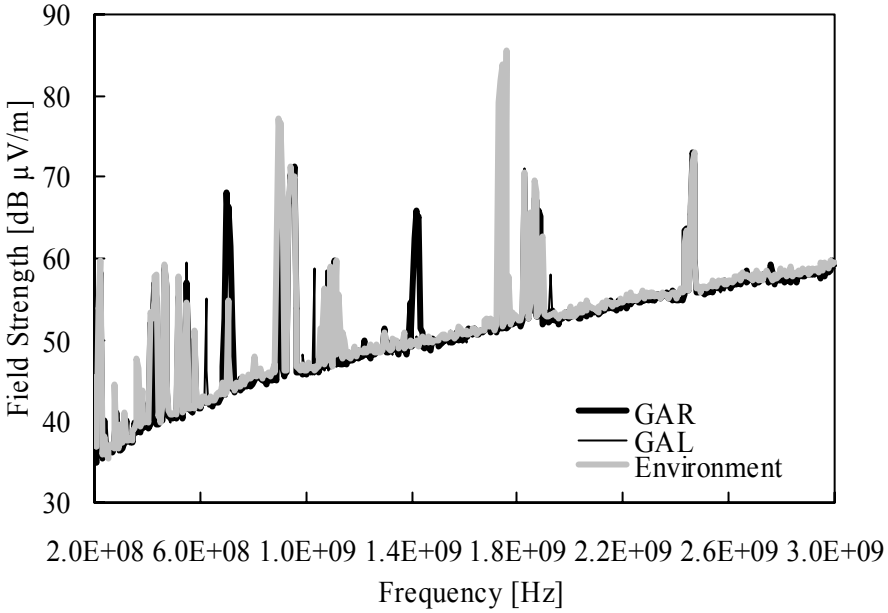

Figure 8: EMC measurement of power modules GAR (PETT) and GAL in comparison with environment

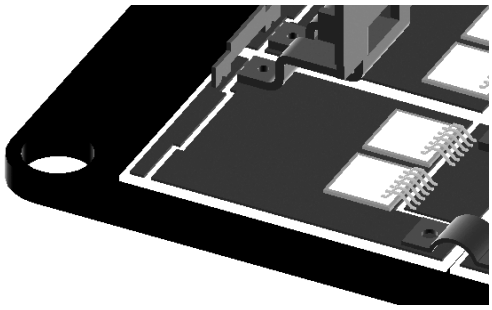

Figure 9: Module layout for one FWD group, module GAR

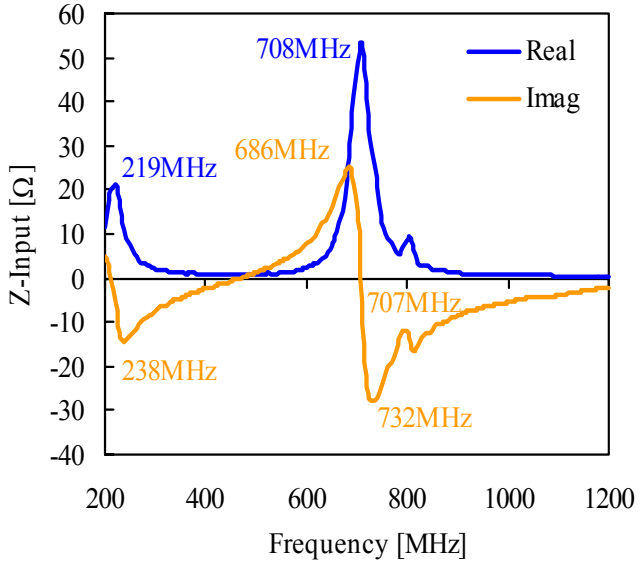

Figure 10: Impedance of the unchanged power module GAR

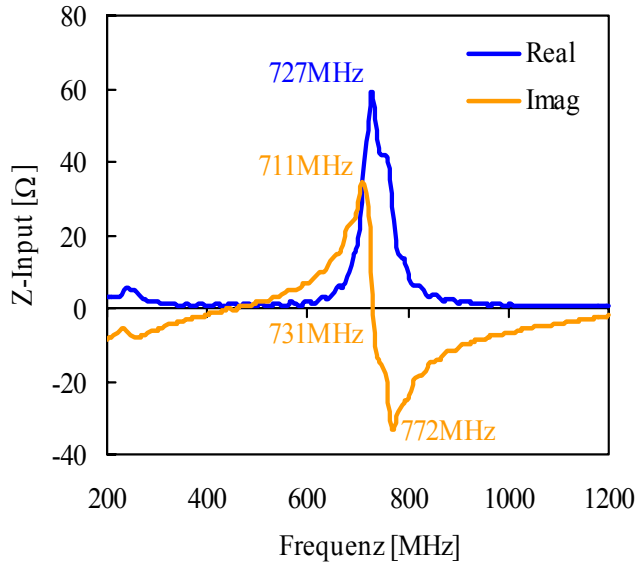

Figure 11: Impedance of the power module GAL

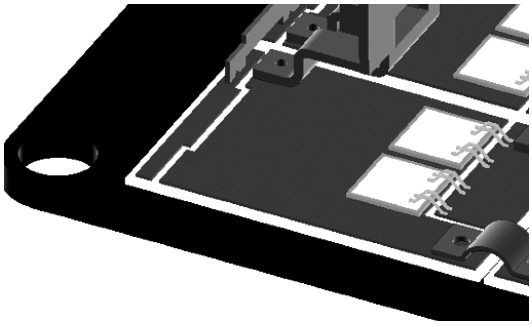

Figure 12: Module with removed bond wires

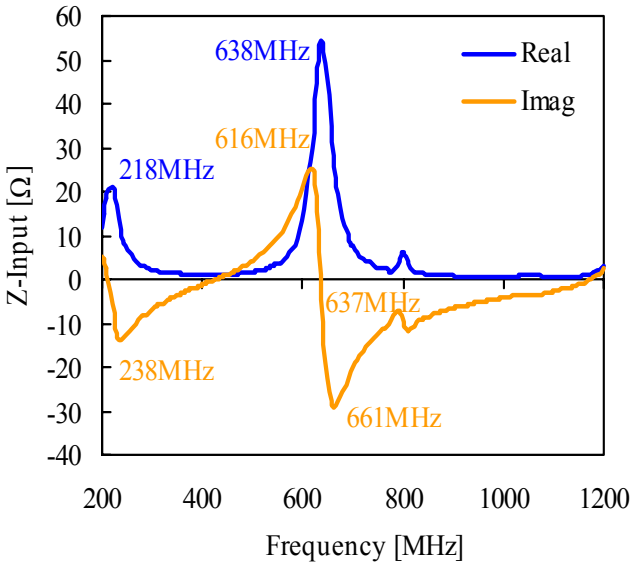

Figure 13: Impedance of the module with removed bond wires as shown in figure 12

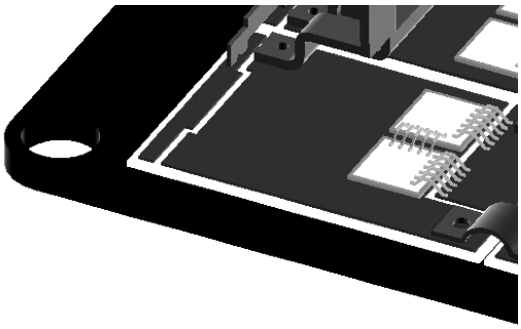

Figure 14: Module with additional bond wires shorting the anode contact areas of the two FWDs

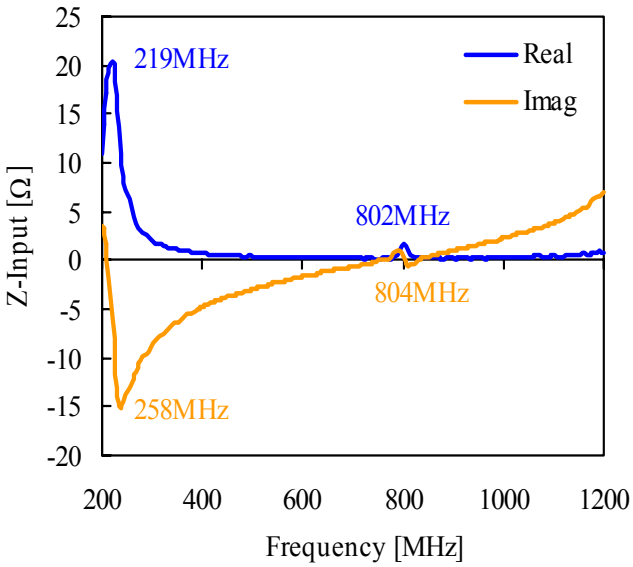

Figure 15: Impedance of the module with connecting bond wires as shown in figure 14

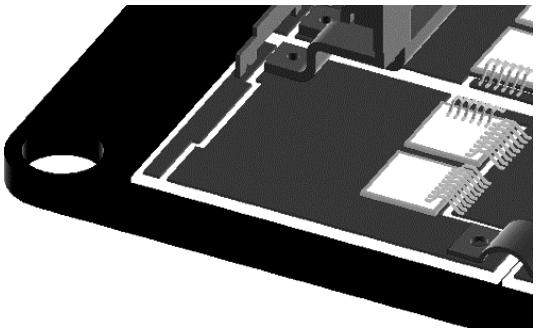

Figure 16: Module with additional bond wires for one FWD only

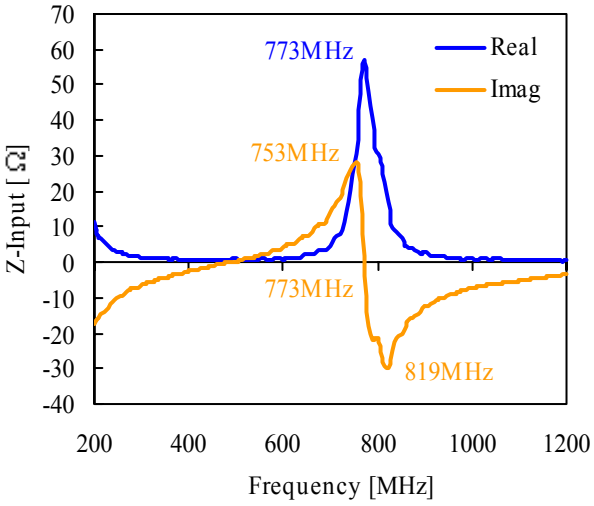

Figure 17: Impedance of the module with additional bond wires as shown in figure 16

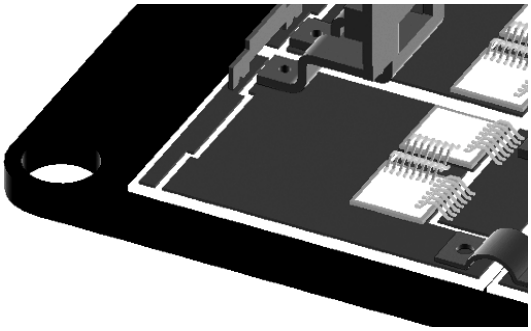

Figure 18: Module with additional bond wires connecting the anode contacts of the two FWDs via a separate area

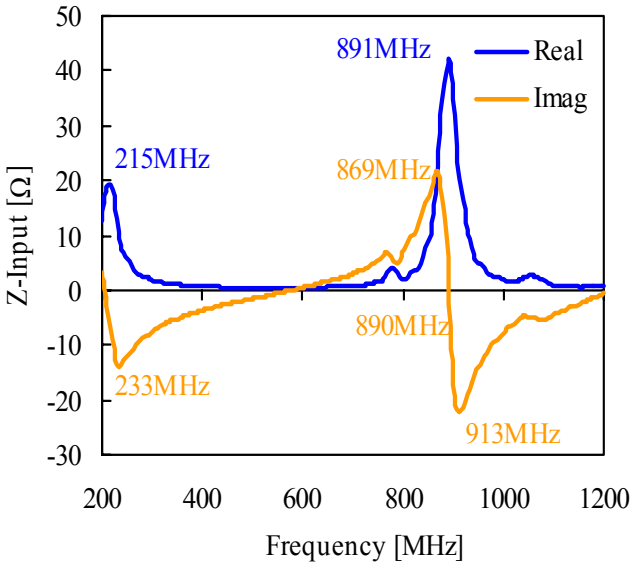

Figure 19: Impedance of the module with as shown in figure 18

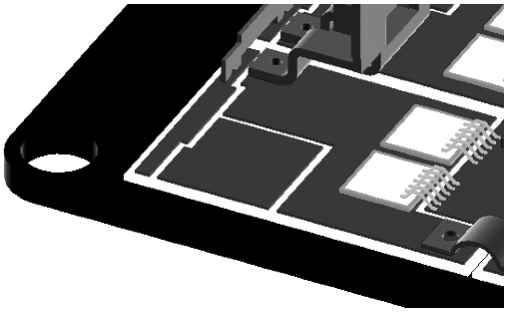

Figure 20: Module with changed capacitance of DCB

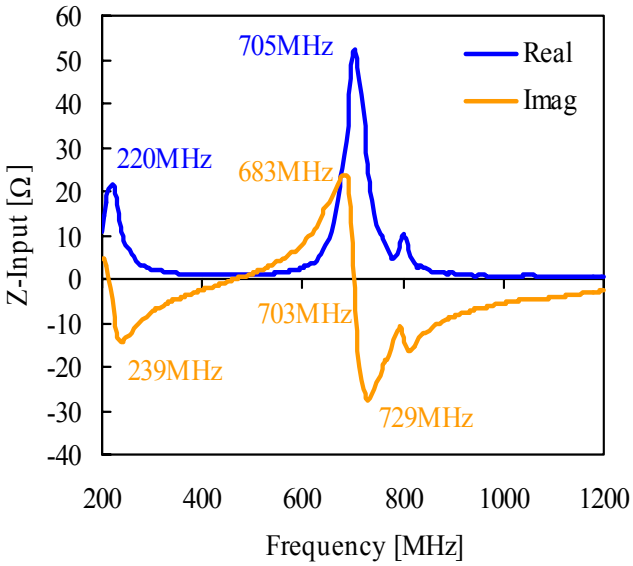

Figure 21: Impedance of the module with changed capacitance of the DCB as shown in figure 20

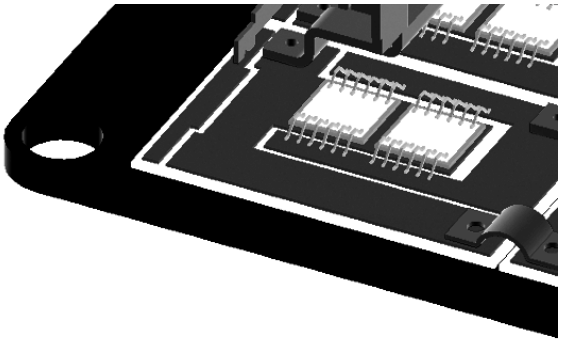

Figure 22: Module with changed layout and increased number of bond wires

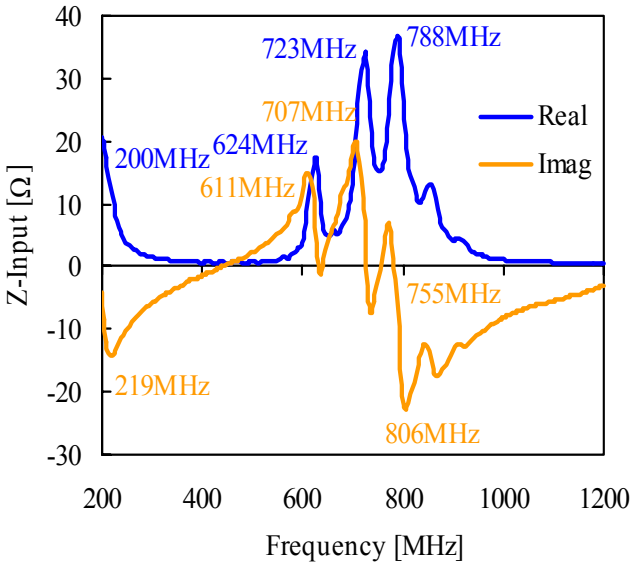

Figure 23: Impedance of the module with changed layout and increased number of bond wires as shown in figure 22