MOSFET Technology as a Key for High Power Density Converters

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***Abstract*— The rapidly increasing computation-capability, data-density and functionality of electronic systems are the driving forces for high-efficiency high power-density converters. Electronic systems are continuously increasing the demand for power, while simultaneously available space and cooling capability stays constant. This requires smaller form factors of the individual converter, higher efficiencies and higher output powers. To meet these demands, new power architectures, new converter-topologies and new MOSFET technologies are developed. In this paper we will review the basic operational modes for low-voltage semiconductors and mirror the resulting requirements with the capabilities of recent MOSFET technology developments.**

I. Introduction

Even though the power-consumption of the individual functions or processes of an electronic system is decreasing continuously, the power demand of the overall system is still growing. The complexity of electronic systems outgrows the power-reduction of the individual functions. Telecommunication and data-networking systems face exponentially growing data-volumes that need to be relayed and stored. Additionally, to process all this data, more capable computing systems are required. Other electronic systems show similar developments. Increased functionality leads to higher power consumption. In a few years drive-by-wire systems, including electronic power steering, power breaking and improved monitoring functions, i.e. tyre-pressure monitoring will be standard. In contradiction to this increase in power requirement stands the need for energy saving and limited space.

This challenge is met in several ways: new power-architectures as i.e. the IBA (intermediate bus architecture) in telecom and data-networking systems are reducing losses on system level. Improving converter-level efficiency is usually realised by more complex and more efficient topologies for AC/DC power-supplies and DC/DC converters. Now, new MOSFET technologies are available that allow the design of converters with higher power-density and efficiency. In this paper we will focus on n-channel enhancement MOSFET technologies in the range of 20 V to 150 V. We review the requirements for new low-voltage MOSFET technologies according to their different functions in power-conversion systems. We evaluate the requirements for switches in isolated and non-isolated converters, power-switches in or-ing circuits and MOSFETs in synchronous rectification.

II. MOSFET Operation Modes

In the following, we will focus on the operation modes that apply to the applications stated above. In all of those, the MOSFETs will be operated as switches. Operation in the linear region and its effects will be neglected. For continuous conduction three states are important: forward conduction (device fully turned on, current flowing from drain to source), reverse conduction (device fully turned on, current flowing from source to drain) and diode-conduction (body diode active). Equally important are the transitions from the conduction states to the off-state and vice versa.

MOSFETs in forward and reverse conduction mode can be modelled by their R_{DSon}. The calculation of the respective losses is simple. However, for a given technology, the R_{DSon} is linked to the R_{th} and Z_{th} of the device. Combined with effects of packaging and cooling-concepts, the R_{DSon} is the key-parameter of a MOSFET technology under static conditions. In opposite, the understanding of the behaviour and loss-generation under

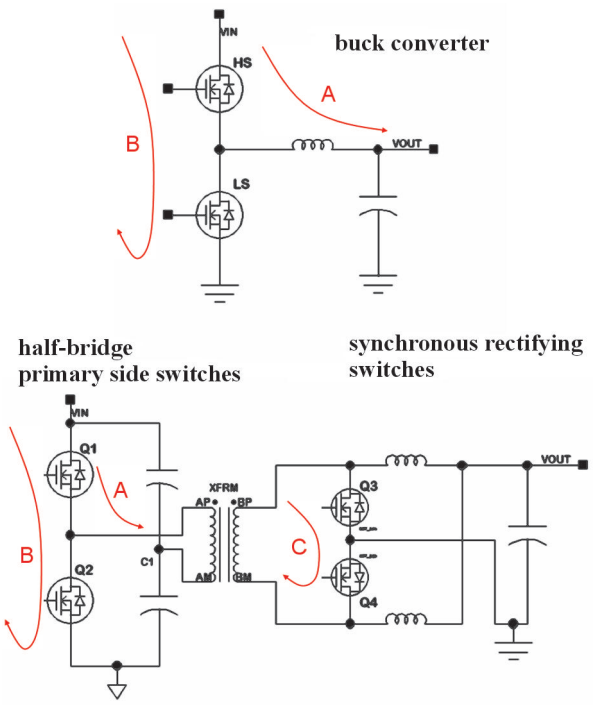

Fig. 1. Functional circuits of a buck-converter and a half-bridge converter with synchronous rectification. A,B,C mark the passes of current change during switching

TABLE I
MAIN APPLICATIONS FOR LOW VOLTAGE MOSFETS IN THE RANGE FROM 20 V TO 150 V
"+/0/-" INDICATE APPLICATIONS THAT ARE TYPICAL/SUITABLE/RARE

	buck/boost control	buck/boost sync.	isol. DC/DC and prim. side switch	isol. AC/DC and DC/DC sync. rect.	power switch
20 V	+	+	-	+	+
30 V	+	+	-	+	+
40 V	+	+	0	+	-
60 V	0	0	0	+	0
80 V	0	-	+	+	+
100 V	0	-	+	+	+
150 V	-	-	+	0	-

transition proves to be difficult. The MOSFET interacts with the surrounding circuitry. Switching behaviour and losses depend on MOSFET parameters as well as on the circuit. This interaction results in different MOSFET requirements for every type of transition. Additionally not only the steady states of the MOSFETs are important but equally the way how the transition is controlled by the external circuit.

In the following, we will discuss which operation modes are relevant in the application and what are the respective key parameters of the MOSFET. The findings are then compared with recent MOSFET developments for typical voltage classes.

Low voltage MOSFETs are used in a wide variety of applications. Applications range from dc-brush and brushless-dc motor-control over power-switches for power distribution to AC/DC and DC/DC SMPS. A volume growth of 10% worldwide is predicted for these devices [1]. The majority of the MOSFETs are used in power-management and power-supply applications. In this paper, we will focus on the requirements and possibilities of the basic applications of low-voltage switches: non-isolated and isolated dc/dc conversion, synchronous rectification in AC/DC switched mode power-supplies (SMPS) and power-switches as listed in Tab. I. The five applications listed in Tab. I can be further grouped according to the three basic functions mentioned earlier. Power switches are mainly characterised by their forward conduction capability, including thermal aspects. Synchronous rectifying switches and synchronous MOSFETs in buck/boost converters act as switched active diodes and primary side switches in isolated converters as well as the control MOSFETs of the buck/boost converters act as control MOSFETs. Functional circuits of the latter two applications are shown in Fig. 1.

A. Power Switches

Power switches are used to protect areas of the circuitry or for power distribution to turn parts of the power system on and off. Devices are selected either to achieve target efficiencies or to stay within the limits of the junction temperature T_j. In case the devices are also used as surge current protection, certain ruggedness for linear operation is required, which is not discussed here in further detail. Conduction losses can be easily calculated as ohmic losses $I^2 \cdot R_{DSon}$, taking into account the R_{DSon} at T_j during operation. To estimate the junction temperature, the knowledge of cooling capability in the system is vital. The $R_{th(j-a)}$ (thermal resistance of junction to ambient) of the device is in series with the thermal resistance of the heatsink, PCB or another cooling path. The sum of the resistances limits the flow of the thermal energy from the silicon to the ambient. The T_j calculates then as:

$$T_j = T_a + I^2 \cdot R_{DSon} \cdot \left(R_{th(j-a)} + R_{th(heatsink)}\right)$$

with ambient temperature T_a and heatsink thermal resistance $R_{th(heatsink)}$.

This equation shows that the overall performance of a power switch is a combination of the R_{DSon} , $R_{TH(j-a)}$ and the attached heatsink. As the die-size is usually shrunk from one MOSFET generation to the next, the $R_{th(j-a)}$ increases for a given R_{DSon}. Fig. *2* shows the R_{DSon} required by a technology that effectively reduces the on-resistance by 50% compared to the reference technology (a 5mOhm device is used as an example) in dependence on the cooling capability. The common limit of both devices is $T_j = T_{jmax}$. It can be seen, that for very good cooling conditions, as achievable with a large heatsink, a substantially lower-ohmic device must be used. This is necessary to prevent the device from exceeding

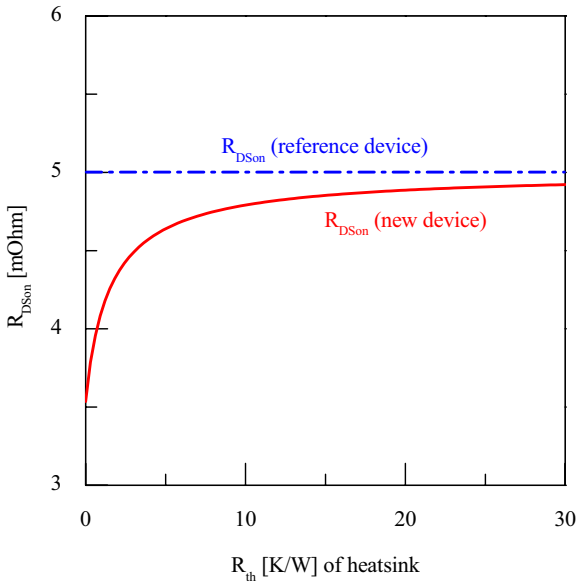

Fig. 2. R_{DSon} required by a technology with a lower $R_{DSon} \cdot A$ than the reference technology, dependent on the heatsinking capability in the application

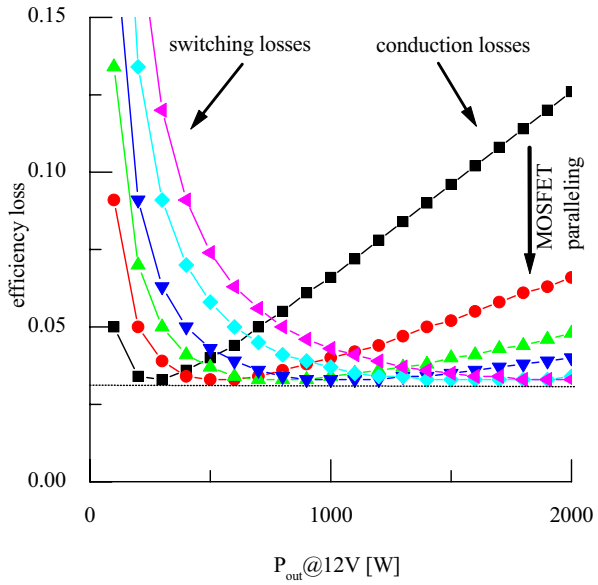

Fig. 3. Efficiency loss in the synchronous rectifying stage of a SMPS with 12V output voltage

the maximum allowed junction temperature T_{jmax}. For SMD parts with an effective cooling of $\sim 30K/W$, the R_{DSon} can be identical for both technologies - without any significant change in T_j. From the above analysis, the R_{DSon} in combination with the R_{th} can be derived as the key parameters for power switches.

B. Switched Active Diodes

The replacement of diodes with MOSFETs to achieve a lower forward voltage-drop during conduction is the inevitable step to reduce losses. For the conduction mode, all considerations done for the power switches are also valid. However, if the MOSFET is operated at high switching frequencies, as it is the case for synchronous rectifying switches in SMPS or the low-side MOSFET in a buck-converter, switching losses and characteristics become important (Fig. 3). If the MOSFET technology used is not sufficiently optimized for this type of operation, it is even possible that no improvement whatsoever is achieved compared to diodes. Often, losses are not the only issue when MOSFETs are used as active diodes. Ringing and overshoots during turn on and off become sometimes more critical than the highest possible efficiency.

As the MOSFET is used instead of a diode, it is possible to leave the device turned-off all the time. The internal body-diode of the MOSFET is, in principle, electrically sufficient. Consequently, the device is always turned-on and -off while the body-diode is in an active state (current flowing from source to drain). Thus all switching of a synchronous MOSFET is therefore effectively zero-voltage switching. Switching losses are not related to simultaneous current and voltage across the device, but due to gate drive, reverse recovery of the body-diode and the output capacitance C_{OSS}. The gate drive losses are often small compared to the other losses. Improved efficiency especially at light loads and lower requirements for the driving circuit are still advantages for a low gate-charge technology. The main switching losses occur during turn-off of the conducting body-diode [2]. At first, the body-diode is conducting, then the externally controlled current changes polarity and the drain-source voltage V_{DS} across the device increases until the final blocking voltage is reached. During these transitions, two charges need to be removed by the MOSFET: the Q_{RR}, which is the stored charge in the body-diode, and the Q_{OSS}, the charge required to charge the C_{OSS} to the blocking voltage. The path of the current changing from Q3 to Q4 is indicated in Fig. 1 as C. As shown in Fig. 4, both Q_{RR} and Q_{OSS} do not completely contribute to the switching losses. The Q_{RR} is removed during the zero-voltage phase (Fig. 4, $t = 40ns$) and does therefore not directly generate losses. The Q_{OSS} stored in the C_{OSS} is fed back to the power-circuit at the subsequent turn-on of the switch. Losses are instead related to the reverse-recovery current flow. Until the blocking voltage is reached, the Q_{RR} and Q_{OSS} feed the reverse current, limited only by the inductances in the loop. When the blocking voltage is reached for the first time (Fig. 4, $t = 64ns$), Q_{RR} and Q_{OSS} are completely removed. However, energy is now stored in the stray inductances in the circuit which is approximately related to the reverse-recovery current peak I_{RRM}:

$$E_{stray} = \frac{1}{2} I_{RRM}^2 L_{stray}$$

This dynamically stored energy appears as ringing after the turn-off and is dissipated in snubber-circuits (if present) and in the ohmic series-resistances. The maximum reverse-recovery current I_{RRM} depends strongly on the circuitry, choice of components and also the way how the di/dt is controlled - either passively limited by the inductances in the circuit, or actively by controlled switching. Fig. 3 shows the efficiency lost in

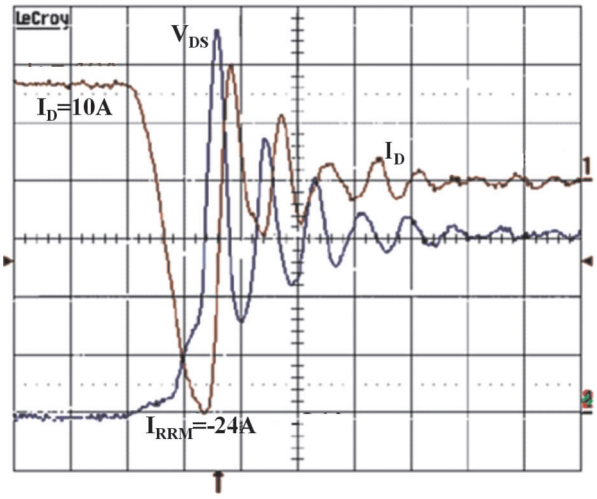

Fig. 4. V_{DS} and I_D at turn-off of body-diode ($16V/div$, $6A/div$, $20ns$)

the synchronous rectifying stage. The switching losses form the lower limit that cannot be improved without changing MOSFET technology or improving the circuitry. The more MOSFETs are paralleled (lower R_{DSon}) the better is the performance under high loads on the cost of higher switching losses reducing efficiency under light loads. Key parameters for the operation as switched active diodes are therefore: R_{DSon}, $R_{th(j-a)}$, $Q_{RR}\,(I_D,\, di/dt)$ and Q_{OSS}.

C. Control Switches

When used as a control switch, the original function of controlling the current through the device is utilized. This is the key function for all kinds of switched-mode power conversion and at least one device operating in this mode is required for this type of application. Loss generation depends on the type of switch, currents, voltages and the overall power-conversion concept. During on-time, all considerations from the power-switch section also apply to the control switch. For transitions, any losses additional to those from the gate-drive strongly depend on the external circuitry and the exact operating conditions. Basically, switching can be divided into hard-switching and soft-switching. Under soft-switching conditions losses are minimized by reducing or even cancelling the voltage (ZVS: zero voltage switching) or current (ZCS: zero current switching) across the device [3]. Hard-switching does solely control the current in the circuit by forcing the gate (hard) on and off when required. This usually leads to switching losses, because voltage and current are simultaneously non-zero across the device during transition. For the further evaluation, only hard-switching transitions are considered, as losses are highest under these conditions.

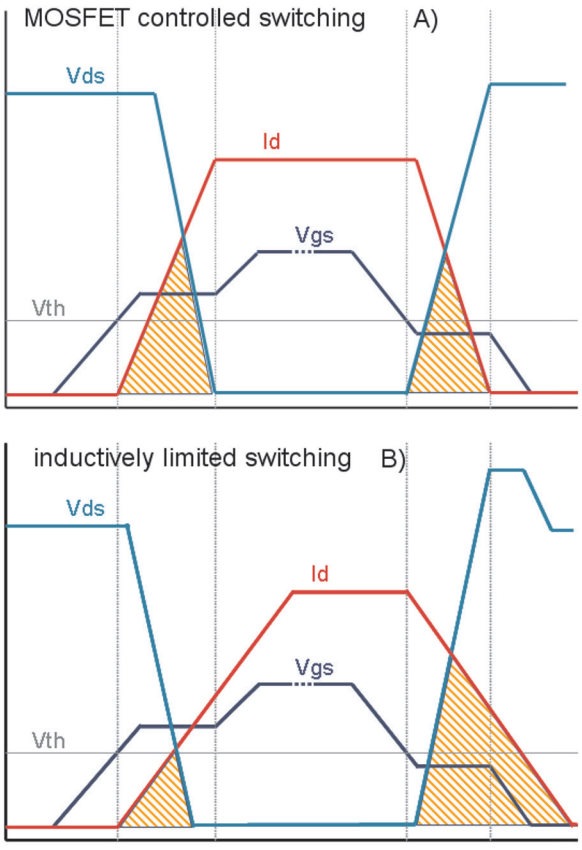

Fig. 5. Current and voltage of control switch under A) MOSFET controlled switching and B) inductively limited switching

MOSFET technologies to be used in SMPS have very low gate-charges (Q_g, Q_{gd}) to switch very fast and have a very low R_{DSon} [4]. This can lead to the situation that the device itself is able turn on and off significantly faster than it takes for the current to rise or drop (Fig. 5 B). Under these circumstances, the switching is inductively limited by the external circuit (including the source- and drain-inductances of the package of the MOSFET). If instead the time to turn the MOSFET on and off is significantly larger than the commutation time for the current, the switching is controlled by the device and is further referred to as MOSFET controlled switching (Fig. 5 A).

The most common applications are the control switches in buck/boost converters or the primary-side switches in the various topologies of isolated DC/DC converters. We will discuss the effects for the half-bridge, similar conditions apply to most other topologies [5]. Examples of the basic schematics are shown in Fig. 1. It is important to understand where the current commutation happens and which inductances limit the switching speed. For the buck/boost converter in discontinuous mode and the hard-switched half-bridge, the turn-on is limited by the output inductor or the leakage inductance of the transformer, respectively. These are typically large compared to the stray inductances in the circuit and packages. The current path is indicated by A in Fig. 1. The turn-on of the buck/boost in continuous conduction mode (CCM), as well as the turn-off for both applications only see the low-inductive loop through the input-capacitance [6]; the current path is indicated by B in Fig. 1. While the typical buck/boost converter operating under CCM sees the same inductance during turn on and off, the situation changes for the half-bridge for turn-on and -off.

MOSFET controlled switching is the transition mode that is described in most textbooks. Losses are generated in the channel region of the device, while voltage and current across the device are non-zero (Fig. 5 A). With the latest low-Qg technologies available, this can be avoided even for very low-inductive circuits. Even with a $di/dt \geq 3000\,A/\mu s$ in a buck-converter operating at 12 V, using the lowest inductive SMD packages and a low-inductive layout, it is possible to operate in the inductively limited regime. This greatly reduces the overall switching losses on the cost of a potentially stronger ringing and increased EMI. MOSFET controlled switching is the preferred choice in applications sensitive to these effects. For inductive switching, the turn-on losses are minimal, as the device switches under quasi zero-current conditions (Fig. 5 B). The turn-off losses usually exceed the turn-on losses, as the energy stored in the inductances $E_{stray} =$

$\frac{1}{2}\, I_{RR}^2\, L_{stray}$ of the circuit needs to be dissipated. This may occur in different ways:

- ringing after turn-off
- device entering avalanche-mode
- dynamic turn-on via coupling of the source inductance in the gate circuit.

Furthermore, some or all of these mechanisms may occur simultaneously. A reduction of switching losses is mainly driven by low gate charges Q_g and Q_{gd} combined with a low-inductive package and layout.

III. MOSFET TECHNOLOGY

Despite all efficiency improvements realized by advanced power architecture concepts and improved converter topologies, power MOSFETs are the key component to achieve higher efficiencies in a power converters. Therefore, the performance of power MOSFETs did advance at impressive rates over the past decade. Modern devices in general have to offer a low on-resistance and low switching-losses, but depending on the application a number of other parameters such as the body-diodes reverse-recovery charge or avalanche ruggedness are from equal importance.

While it is essential for the achievement of a low on-resistance R_{DSon} to employ a trench-gate concept, there are nevertheless different competing device concepts in development or already available on the market:

1) dense-trench MOSFETs [7]
2) MOSFETs using shallow trenches with deep implants and high cell density [8]
3) field-plate trench MOSFETs [9]
4) trench MOSFETs employing floating p-islands [10]

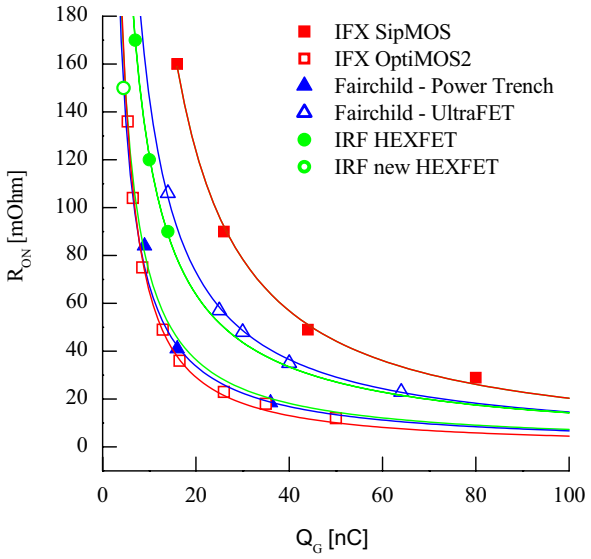

Fig. 6. Device performance comparison chart for different 100 V MOSFET technologies of Infineon, Fairchild and International Rectifier (based on data-sheet values, package TO-220)

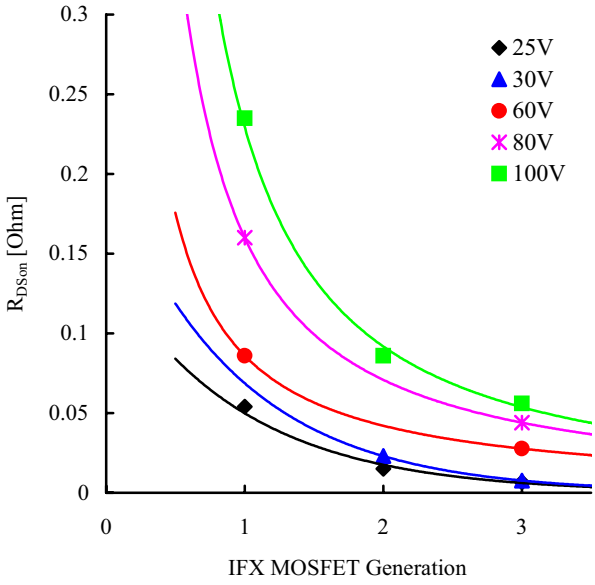

Fig. 7. Evolution of Infineon's low-voltage power MOSFET technologies

Depending on the employed concept, some devices benefit from well-engineered manufacturing technology and/or from newly-developed concepts using charge-compensation principles in different ways.

As an example, Fig. 6 gives a comparison of elder and up-to-date 100 V power MOSFET technologies of three semiconductor manufacturers. As can be seen, all their latest technologies, although based on different device concepts, show rather comparable performance in terms of FOM. Nevertheless there are differences leaving the devices more or less optimized towards specific application fields.

Future technologies will continue to focus on on-resistance improvements, but probably spend more care on overall performance (in terms of FOM) in dependence of the targeted application fields. Already now the devices with lowest per-area on-resistance not necessarily show the best FOM. Especially, an increase in cell density reduces the on-resistance, but in same time increases the total gate-charge. An improvement of both basic parameters needs more advanced cell concepts and higher technological efforts. Another limiting factor is related to the thermal behaviour of the device. An increase in current density due to lower on-resistance leads to higher power-densities. Simultaneously, the available area for cooling becomes smaller. Especially the performance under critical operation conditions, such as avalanche events, might suffer. Consequently there is a need for advanced packaging concepts ensuring higher current capabilities, better cooling and lower package-related on-resistance.

For instance, Fig. 7 depicts the evolution of power MOSFET technologies at Infineon Technologies, covering the last three generations and including some general landmarks for the current developments. By employing charge-balancing principles as explained in [9], the on-

resistance is shifted below the so-called silicon-limit line (breakdown voltage of an ideal planar pn-junction). Note that the values shown in Fig. 7 do not consider the substrate resistance which naturally becomes more significant as the blocking voltage decreases.

IV. Packaging

With silicon technology moving rapidly forward the package becomes an important part for low-voltage MOSFETs. As discussed in the sections II and III, the package inductance can play a major part in loss generation and for the overall device performance. Additionally, the on-resistance of the latest technologies has become so low spurring the need for low ohmic packages to avoid a limitation of the device by the package characteristics. 30 V technologies from most vendors today allow for MOSFET dies in a TO-220 with a lower on-resistance than the package resistance. Latest 55 V technologies on the market allow for devices with a package contribution of 30% and even for 100 V technologies the package can account for almost 20%, given a package resistance of 1 mOhm. The package resistance not only limits the minimum on-resistance achievable in a package. Additionally, a larger die is required for a given R_{DSon} which increases the Q_g and thus slowing down the device. Package contributions for devices with maximum die-size for the most common low-voltage MOSFET classes are shown in Fig. 8. To follow the route towards denser and more efficient power converter designs, new package types, such as the SuperSO8, need to replace the leaded SMD or through-hole devices for low-voltage MOSFETs.

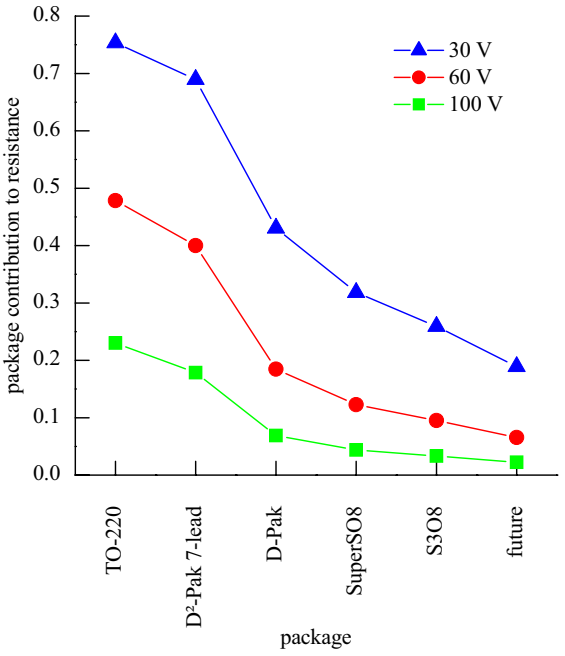

Fig. 8. Package contribution to overall package resistance for devices with maximum die-size for state of the art technologies in 30 V, 60 V and 100 V

It is easily possible to estimate the losses due to package inductance for the turn-off. As example, a buck-converter with an output current of 30 A, operating at 250 kHz, generates 0.7 W of losses in a D-Pak design due to the total package inductance of 6nH. With a low inductive package like the SuperSO8, showing an inductance of just 0.5 nH, the losses drop below 0.1 W.

V. Summary

In this paper we discussed the main operation modes of low-voltage MOSFETs utilized in power conversion and power management applications. It was shown that the continuing roadmap towards lower and faster switching technologies has already brought many applications to a point where the limits are no longer the MOSFETs but external components, the layout and the choice of package. While this roadmap will still yield a benefit for most applications, it comes at the cost of higher thermal resistances, diminishing the effect of the reduced R_{DSon} and the expected cost-down. For future MOSFET technologies a higher degree of specialisation for individual applications is required, merging the silicon and packaging technology and layout guidelines into an overall concept.

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