# A new fast and rugged 100 V power MOSFET

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***Abstract*— A new, rugged 100 V power MOSFET of the OptiMOS$^{TM}$2-family is described. By applying compensation principles, a device technology was developed that combines low on-state resistance $R_{ON}$ with outstanding switching properties. The technology also offers a small gate charge $Q_G$ and a small gate resistance $R_G$. In addition, the internal body diode, when acting as freewheeling diode, reveals a soft reverse-recovery with a small reverse-recovery charge $Q_{RR}$. Therefore, the technology is particularly suitable for a variety of applications, including highly efficient DC-DC and AC-DC converters, telecommunication and server topologies, Class-D amplifiers, and motor control.**

## I. Introduction

The performance of semiconductor power switches continues to advance at impressive rates. In parallel, new device generations are developed with increasing focus on particular power applications. This development of new power MOSFET devices is driven by the ever-increasing performance requirements of electronic switches in a variety of power applications. In order to offer small and energy-efficient solutions, such devices in general have to offer a low on-state resistance as well as low switching losses [1], [2], [3].

The new device family presented in this work is mainly intended for switching applications such as DC-DC power supplies for telecommunication base stations or industrial servers and AC-DC adapters for notebooks and plasma screens. Other possible application areas are motor drives for fork-lifts and hybrid-electric vehicles, or Class-D amplifiers.

DC-DC power supplies used in telecommuncation base stations often employ an active-clamp forward topology.

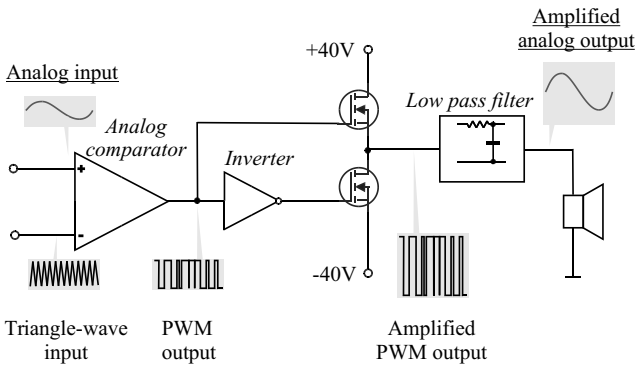


Fig. 1. Functional diagram of Class-D amplifier

Here the 100 V MOSFET on the primary side of the circuit benefits from the low switching losses and minimized on-state resistance for further reduced conduction losses. In order to reduce the total switching losses, low values of the gate resistance $R_G$ are necessary to enable short transient times. Voltage peaks due to atypical operating conditions require a sufficient avalanche ruggedness of the device.

In AC-DC adapter applications, MOSFET switches in the voltage range between 80 V and 150 V are applied on the secondary side for synchronous rectification. Here, main requirements are a low on-state resistance and the capability for fast switching. A fast turn-off is especially important to prevent a shoot-through during current commutation [4].

Class-D amplifiers, whose functional diagram is shown in Fig. 1, demand fast switching frequencies up to 500 kHz. They require low on-state resistance and the capability for very fast switching (low total gate charge) and a low reverse-recovery charge as well as soft reverse-recovery behavior of the body diode.

For motor-drive applications, a low on-state resistance is more important, since switching frequencies are generally lower. Special care should be taken to ensure a soft reverse-recovery behavior of the body diode; this is essential to minimize voltage overshoots related to inductances.

## II. Advanced Device Concept

The compensation principle for power MOSFETs was introduced in 1998 in commercially available products with the 600 V CoolMOS$^{TM}$ Technology [5]. The basic principle behind the drastic $R_{ON} \cdot A$ reduction compared to conventional power MOSFETs is the compensation of n-drift region donors by acceptors located in p-columns. The compensating acceptors are located in lateral proximity to the drift region donors, in contrast to a large vertical distance when the acceptors are positioned in the body region. In addition, the acceptors are distributed over the total length of the drift region, in contrast to a strong localization in the body region, which leads to a very homogeneous electric field distribution over the entire voltage-sustaining region. The requirement for precise lateral n- and p-dose compensation limits the n-drift region doping. Therefore compensation power MOSFETs are typically used for breakdown voltages of several hundred Volts.

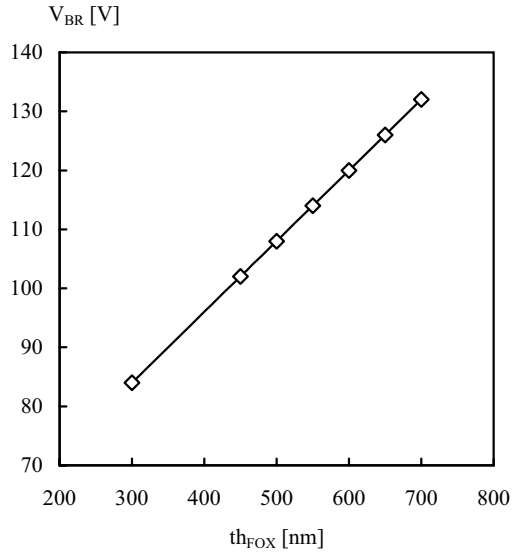


Fig. 2. Stationary breakdown voltage in dependence of field oxide thickness for a given background doping

For breakdown voltages below 200 V, trench field-plate MOSFETs are an excellent alternative [6]. The device comprises a deep trench penetrating most of the n-drift region. An insulated field plate provides mobile charges required to balance the drift region donors under blocking conditions. A voltage source dynamically provides electrons on the field plate and therefore the charges in the lateral drift region are precisely balanced under all operating conditions. The field-plate insulation has to withstand the full source drain blocking voltage of the device at the trench bottom. Consequently, oxide thicknesses in the micron range have to be regulated carefully with a special focus on avoiding thinning at the bottom trench corners and preventing generation of stress-induced defects.

The combination of a field-plate and a trench-gate further improves the device's performance and makes it possible to employ all advanced capabilities of such power MOSFET structures. In contrast to standard trench MOSFET structures that exhibit a linearly decreasing electric field with a maximum at the body/drift region pn-junction, the field-plate principle leads to an almost constant field distribution, thereby reducing the necessary drift-region length for a given breakdown voltage. Unlike in a state-of-the-art trench-gate or planar-gate device, the carriers are first removed in the mesa region between the trenches by a lateral electric field. If the nominal blocking voltage is reached, the complete mesa region is depleted. In addition, the drift-region doping can be increased, resulting in a clearly reduced on-state resistance. In fact, $\mathrm{R_{ON}} \cdot \mathrm{A}$ is even reduced below the so-called "Silicon Limit," which is the on-resistance of an ideal abrupt $\mathrm{p^+n}$- junction at a given breakdown voltage not limited by any edge termination structure. The reduced drift-region length and increased doping concentration also significantly improves the performance of the body diode, because a reduced amount of charge is stored in the device as described later in chapter IV.

In the device concept presented here, the stationary breakdown voltage for a given doping density is controlled by the thickness of the field-oxide layer in the bottom of the trench, as shown in Fig. 2. Other parameters such as drift-region doping etc. show only weak influence on the blocking capability. Thus, the breakdown voltage of the device was found to be outstanding stable over a large number of manufactured development lots (cp. Fig.3).

## III. Ruggedness

For all applications that have to handle inductive loads, the capability of the MOSFET to drive unclamped inductive loads is essential. In this case, the voltage over the devices is driven to the breakdown voltage by the inductance.

Ideally, the avalanche current is spread uniformly across the whole active device area which is supported by the positive temperature coefficient of breakdown voltage. The device finally fails because the dissipated energy due to the current flow leads to a temperature at which the

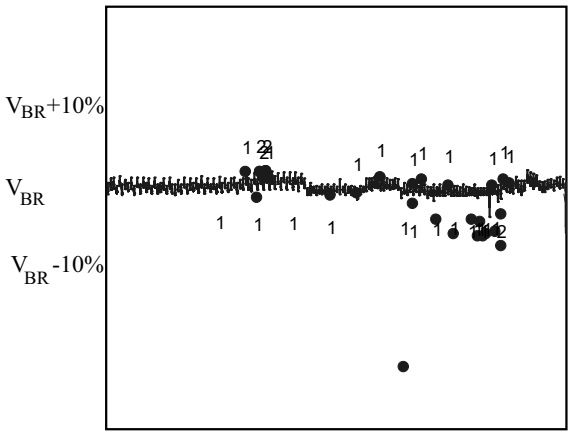


Fig. 3. Breakdown voltage over development lots

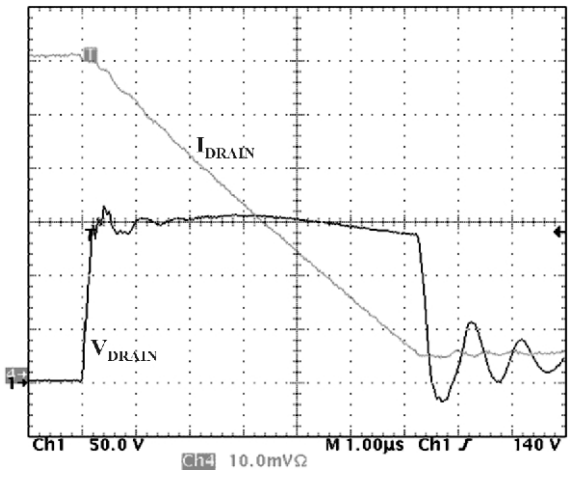


Fig. 4. Thermal destruction of a 100 V device due to avalanche

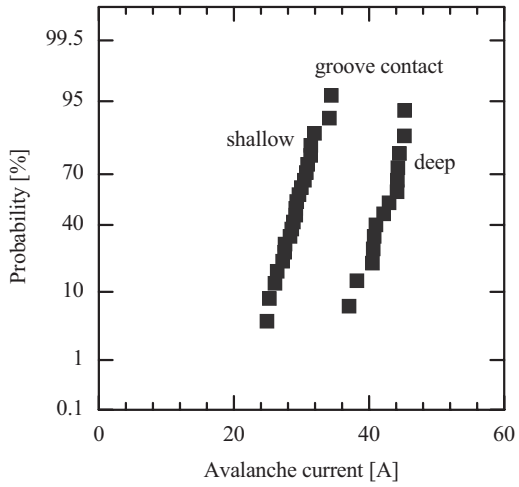


Fig. 5. Probability plots of measured avalanche currents for devices with shallow and with deep groove contact

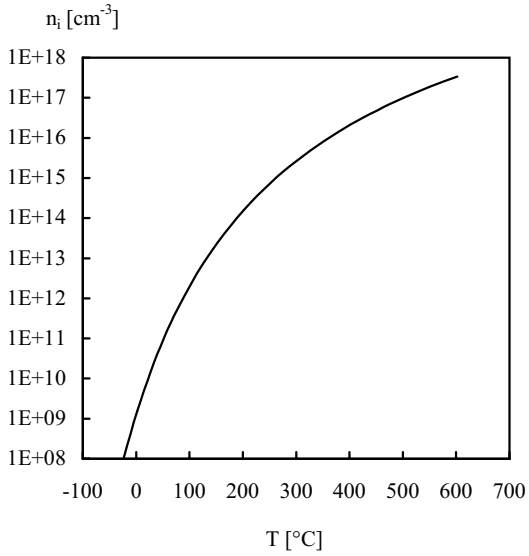


Fig. 7. Temperature dependence of the intrinsic carrier density

carrier concentration becomes too large and the device behaves intrinsic. This failure mechanism is known as thermal destruction; a typical measurement is shown in Fig. 4. In principle, device failure at a current slightly below destruction current can not be avoided for large inductances in which a large energy amount is dissipated at low current densities.

The second mechanism that results in the destruction of MOSFET devices is called non-thermal destruction, and is related to the turn-on (latch-up) of the parasitic npn-transistor. This effect is caused by the current flow through the p-base. As soon as the voltage drop across this region is large enough to forward-bias the base-emitter barrier, the transistor turns on. Unlike the avalanche generation rate, the latch-up of the npn-transistor shows a negative temperature coefficient. Once latch-up starts, local heating occurs due to inhomogeneities, and a steadily rising current goes through that point. Researchers have already tried to design the bipolar structure for a homogenous turn-on [8]. This could provide a sufficient avalanche capability as well, but devices are usually designed to shift the latch-up of the npn-transistor to current densities beyond the thermal destruction point. Precise control of the npn latch-up is difficult due to the complex dependencies of the transistor gain. Furthermore, as already explained, latch-up is self-amplifying while in case of avalanche, a uniform current distribution is supported by the positive temperature coefficient of the breakdown voltage. Destruction due to bipolar latch-up therefore usually results in a large statistical spread of the measured destruction current density, while thermal destruction shows a narrow distribution of the destruction current density of a given device. As an example, Fig. 5

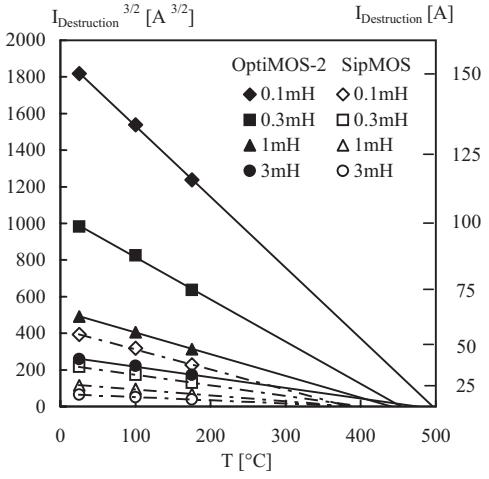


Fig. 6. Avalanche capability vs. junction temperature of two 100 V devices

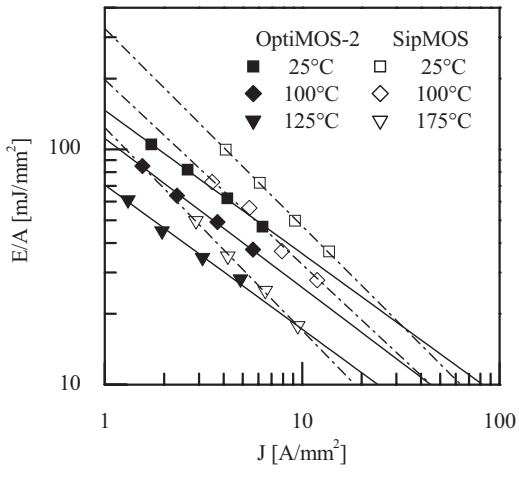


Fig. 8. Avalanche energy density vs. current density

shows probability plots of measured avalanche currents of two different devices rated for 100 V. Here, the increase of the groove contact depth gained a clear increase in the current capability of our devices due to a more efficient hole removal. By this measure, the current density leading to a latch-up of the bipolar transistor was shifted well above the thermal destruction limit.

Rugged devices show characteristic curves as shown in Fig. 6 for our new OptiMOS$^{\mathrm{TM}}$2 100 V trench device in comparison with our planar predecessor technology. Here, extrapolation lines are fitted to the average failure current points determined at various temperatures. The intersection point with the zero-current line is found at the intrinsic temperature of the device. The intrinsic temperature is the temperature at which the intrinsic carrier density $\mathrm{n_i}$ becomes equal to the background doping $\mathrm{N_D}$. From this point, the doping does not have any effect towards breakdown capability anymore, the silicon behaves intrinsically and fails due to thermal destruction. During an avalanche event, the present electric field generates more electrons by smashing electrons into the lattice atoms and thereby releasing new free electrons. The lattice temperature increases due to the rising current flow which again causes more thermally generated carriers, compensating the decrease of the avalanche generation rate due to the temperature rise. After a certain time, destruction of the device occurs.

The intrinsic carrier density and therefore the intrinsic temperature for a given background doping can be calculated by eq. 1 (Fig. 7), which is based on empirical data [7]:

$$n_i = 3.88\,10^{16}\,\frac{T}{K}^{\frac{3}{2}}\,\exp\left(-\frac{7000K}{T}\right)\,cm^{-3} \quad (1)$$

By using eq. 1 it is possible to estimate the avalanche capability of a device via the intrinsic temperature for a given background doping. The improved blocking capability of our new device allows for a larger drift-region doping (cp. Sect. II) and therefore a higher intrinsic temperature as validated by the measurement results in Fig. 6. This is extremely important since trench devices, especially those with very low $\mathrm{R_{ON}} \cdot \mathrm{A}$, allow much larger current densities even although the effective area is noteworthy limited by the trench area. Furthermore the heat flow is blocked by the silicon oxide, thus the total available silicon volume for heat-up is again reduced. Consequently, the temperature rise at a given power density becomes larger and therefore an avalanche event is more difficult to withstand. Fig. 8 shows the comparison of the relation between current density and maximum avalanche energy density for the new OptiMOS$^{\mathrm{TM}}$2 and the forerunner SipMOS$^{\mathrm{TM}}$ technology. It can be concluded that the new trench technology shows an avalanche ruggedness comparable to the planar predecessor technology, thus being suited for a wide range of fast and reliable switching applications.

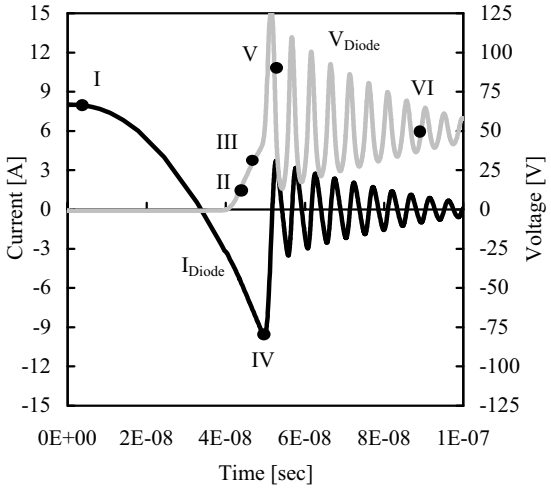


Fig. 9. Simulated reverse-recovery waveforms for the standard MOSFET body diode ($\mathrm{V_R} = 50\,\mathrm{V},\ \mathrm{J_F} = 8\,\mathrm{A/mm^2},\ \mathrm{di/dt} = 500\,\mathrm{A}/\mu\mathrm{sec}$)

## IV. Properties of the Body Diode

In many applications such as DC-DC converters or motor drives, the properties of the body diode play a significant role in the total system performance. In order to achieve a faster transient response and higher power efficiency for DC-DC converters, the reduction of reverse-recovery losses is crucial. Additionally, minimizing electromagnetic interference at high operating frequencies requires fast and soft switching. Especially for motor drive applications, soft reverse-recovery behavior is essential in order to minimize voltage overshoots due to stray inductances.

In contrast to discrete freewheeling diodes for high-voltage applications, various options for improvement of the body diode cannot be accomplished because the electrical characteristics of the body diode are predetermined by the MOSFET structure. For instance, the emitter injection efficiency on the anode side of the body diode

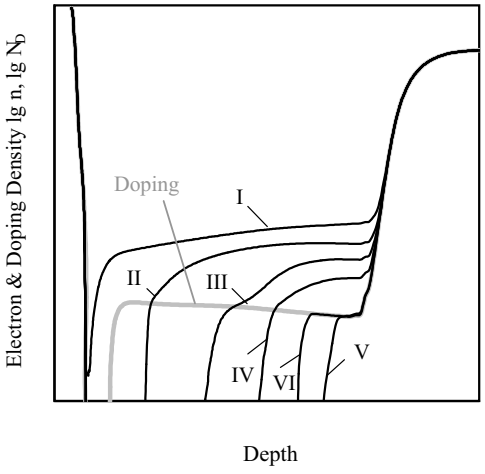


Fig. 10. Electron concentration and doping profile for the standard body diode at six different times (I - VI) as indicated in Fig. 9

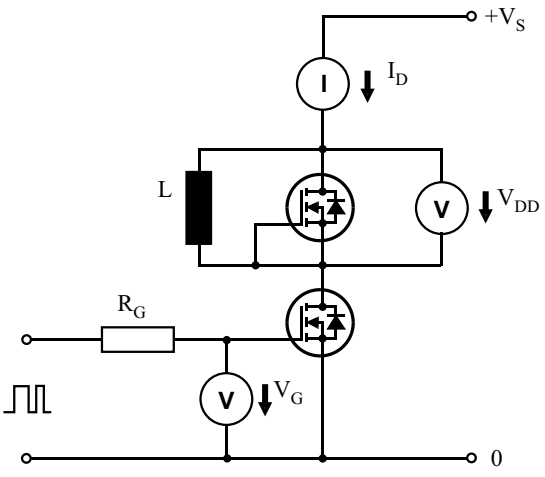


Fig. 11. Reverse-recovery measurement circuit used for characterization of the MOSFET body diode

is given by the doping profile of the MOSFET p-body. Thus, commonly known techniques for carrier injection control by altering the anode properties [9] cannot be used. Another widely used technique for the optimization of freewheeling diode properties is the tailoring of the carrier lifetime profile by irradiation with electrons or light ions [10]. This method has also been suggested for the improvement of the body diode of power MOSFETs [11]; however, it requires additional processing steps that can have an adverse effect on the MOSFET parameters. Other ideas include using a Schottky contact in parallel to the MOSFET in separate [12] and monolithic solutions [13].

The reverse-recovery of the 100 V MOSFET body diode was analyzed via two-dimensional device simulation, including the external circuit (mixed-mode simulation) [14]. The voltage and current waveforms (Fig. 9) showed undesired oscillations with large amplitudes. For several points in time as depicted in Fig. 9, the electron concentration inside the device was calculated (Fig. 10). The stored charge inside the device, feeding the reverse-recovery current, had already vanished at the time of the reverse-recovery current peak (IV). Consequently, the reverse current showed a snap-off, causing a large di/dt and therefore large voltage overshoots. To overcome this problem, it is necessary to provide stored charge carriers during the entire recovery process. In addition, the built-in npn BJT (Bipolar Junction Transistor) influences the reverse-recovery process [15]. Therefore its properties have to be taken into account when optimizing the body diode. Naturally, the measures taken to increase the avalanche capability will also influence the body diode properties. Therefore there are several possibilities to improve the performance of the body diode, e.g. variations of doping profiles, BJT properties, or contact groove depth.

Based on device simulation results, a variety of different power MOSFETs was manufactured and their reverse-recovery characterized with a standard circuit as shown in Fig. 11. Special care was taken to create a setup with low stray inductances in order to minimize any additional influences. Control of the rate of current change di/dt was done by varying the resistor $\mathrm{R_G}$.

Fig. 12 shows the reverse-recovery waveforms of a 100 V device with a deep contact groove and high avalanche ruggedness (cp. Fig. 5). The reverse recovery of the body diode was satisfactory for a rate of current change di/dt = 750 A/$\mu$s. The overvoltage spikes, approximately 30 V at most, did not cause any damage to neighboring devices since the stationary breakdown voltage of 100 V was not exceeded. Nevertheless, amplitude and duration

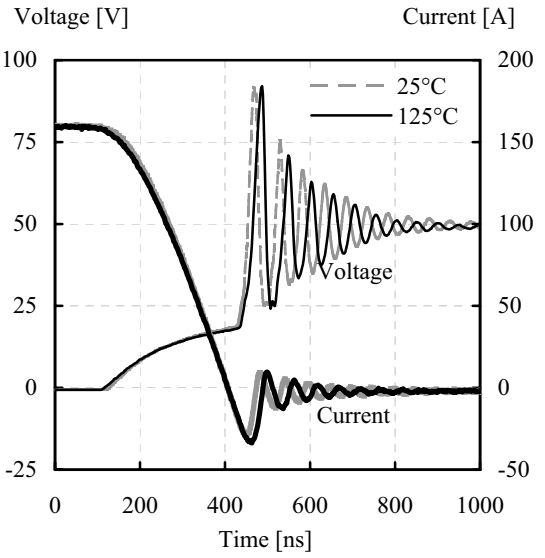


Fig. 12. Reverse-recovery waveform at nominal current for an avalanche-rugged device with deep groove contact ($\mathrm{V_R} = 50\,\mathrm{V}$, $\mathrm{I_F} = 160\,\mathrm{A}$, $\mathrm{di/dt} = 750\,\mathrm{A}/\mu\mathrm{sec}$)

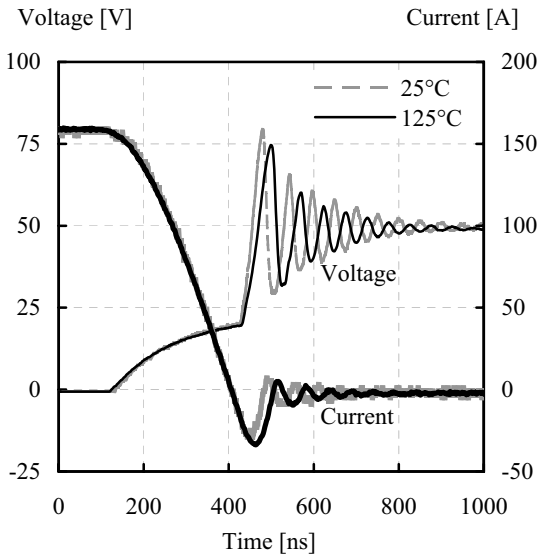


Fig. 13. Reverse-recovery waveform at nominal current for an avalanche-rugged device optimized for reduced voltage overshoot ($\mathrm{V_R} = 50\,\mathrm{V}$, $\mathrm{I_F} = 160\,\mathrm{A}$, $\mathrm{di/dt} = 750\,\mathrm{A}/\mu\mathrm{sec}$)

of the oscillations should be minimized for reduced EMC (electromagnetic compatibility) related problems.

Further experimental enhancements of the power MOSFET structure resulted in a device with good avalanche ruggedness and improved reverse-recovery behavior. The measurements shown in Fig. 13 indicate a smaller voltage overshoot and reduced oscillations at only slightly increased reverse-recovery charge $\mathrm{Q_{RR}}$. Even in case of a forward current density as small as 10 % of the nominal current density, the device showed only small overvoltages. A low current density is the more critical case for the body diode, since the number of stored charge-carriers, that feed the reverse current, is much smaller. The device performed well enough to suit even the most challenging applications, and indicated the potential for further developments.

## V. General Device Performance

A comparison of different MOSFET technologies is possible by using the so-called "Figure of Merit" $\mathrm{FOM} = \mathrm{R_{ONmax}} \cdot \mathrm{Q_G}$ in which the dependence of the parameters on the chip area is cancelled. Additionally, an adequate indicator for the switching losses is given by $\mathrm{FOM_{GD}} = \mathrm{R_{ONmax}} \cdot \mathrm{Q_{GD}}$. Fig. 14 gives a comparison of the device performance of currently available power MOSFET technologies in the 100 V class. Here, also values for the HS (High Speed) device optimized towards fast-switching applications are included. These devices have a drastically-reduced gate-charge $\mathrm{Q_G}$ while the on-state resistance $\mathrm{R_{ON}}$ is increased only slightly. The technology-specific parameters for our new 100 V MOSFET family are as follows:

$\mathrm{FOM} = 560\,\mathrm{m\Omega\,nC}, \mathrm{FOM_{GD}} = 140\,\mathrm{m\Omega\,nC}$ (standard)
$\mathrm{FOM} = 395\,\mathrm{m\Omega\,nC}, \mathrm{FOM_{GD}} = 108\,\mathrm{m\Omega\,nC}$ (highspeed)

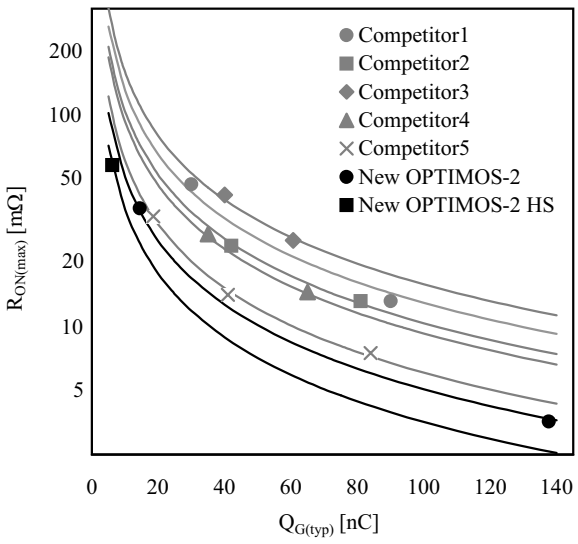


Fig. 14. Device performance comparison chart for available technologies at the time of writing, and the new OptiMOS$^{\mathrm{TM}}$2 technology in the 100 V class (package-related on-resistance eliminated)

## VI. Conclusion

The new OptiMOS$^{\mathrm{TM}}$2 100 V MOSFET family offers benchmark performance in its voltage class. It is therefore suitable for a variety of applications, including highly efficient power supplies for telecommunication and servers (DC-DC), adapters (AC-DC) for notebooks and plasma screens, battery chargers, Class-D amplifiers, or even motor drives. In addition, the superior reverse-recovery behavior due to the body diode with low $\mathrm{Q_{RR}}$ and sufficiently soft I-V characteristics makes the OptiMOS$^{\mathrm{TM}}$2 100 V MOSFET family an excellent choice for applications that require freewheeling of the device e.g. all motor-control applications with a full bridge converter topology. New horizons are opened with especially-optimized high-speed devices with strongly reduced gate-charge $\mathrm{Q_G}$.

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