COMPARISON OF PT AND NPT CELL CONCEPT FOR 600V IGBTs

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Abstract. This paper presents a comparison study of PT- and NPT-IGBTs with a blocking voltage of 600V using two dimensional device simulation. The devices are simulated within a realistic external circuit in order to study the trade-off between total power losses and switching frequency at various temperatures. The results are compared with published data from available PT-IGBTs. It is concluded that the 600V NPT structure is able to compete with the PT structure, but it needs an advanced manufacturing technology for thin wafer handling.

Keywords. PT/NPT 600V IGBT, blocking capability, device characteristics, simulation, comparison with data sheets

NPT-IGBTs (Non Punch Through IGBTs) are well established in the high voltage range (1200V and above). Due to the improvements in the last few years [1,2], the device will be able to compete with the PT-IGBT (Punch Through IGBT) in the range below 1000V as well. In this lower voltage range, the PT-IGBT is still the most important device. In this work, the possibilities for the use of the NPT cell concept for a 600V IGBT shall be discussed.

THE PT AND NPT CELL CONCEPT

NPT-IGBTs as shown in Figure 1 are presently fabricated with a thickness up to 200µm due to safe wafer handling. The thickness of 200µm also realizes the required blocking voltage of 1200V. Recent improvements in wafer handling reduce the required wafer thickness to 170µm [3]. This is sufficient for achieving the required blocking voltage, as well as a further decrease in the forward voltage drop. An additional improvement in wafer handling will allow a further reduction of wafer thickness, the NPT-IGBT may be usable for blocking voltages of 600V too. 600V NPT-IGBTs need a wafer thickness of approximately 100µm.

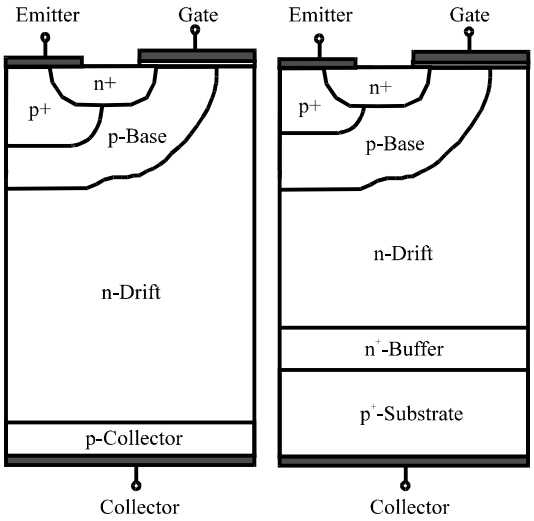

Figure 1: Structure of the NPT-IGBT(left) and the PT-IGBT(right)

NPT-IGBTs consist of a low-doped n-type substrate (Figure 1). The required p-collector at the device backside is formed by shallow implantation (of boron for instance) and acts as the physical emitter of the pnp-transistor. This is why it shall be refered to as backside emitter from now on. Substrate thickness and doping ensure a high blocking voltage, but increase forward voltage drop and turn-off losses. The efficiency of the emitter is affected by the p-doping, so that this parameter influences most of the device characteristics, like forward voltage drop and switching behaviour
PT-IGBTs consist of two epitaxial layers on top of a highly doped p-type substrate (Figure 1). The low doped drift layer strongly influences the forward voltage drop and the switching losses in relation to the stored charge. The drift layer also influences the blocking capability of the device and requires a minimum thickness of 45-65µm for a 600V device (depending on the buffer layer doping) [4,5]. The n-type buffer layer stops the expansion of the space charge region in the blocking state. The p-collector at the backside of the device is formed by the p^+-substrate. The emitter efficiency is affected by the doping relation between the buffer layer and the p^+-substrate as well as the carrier lifetimes. Thus the dynamic properties of the PT-IGBT depend on the parameters of the buffer layer and carrier lifetime control.

SIMULATION CONDITIONS

The structures investigated in this paper were simulated using the device simulator ToSCA [6]. ToSCA is able to solve the van Roosbroeck equations for two dimensional and cylindrically symmetrical devices. The device simulator uses finite elements on a triangular mesh. It also allows a kind of simple mixed mode simulation including several semiconductor devices.

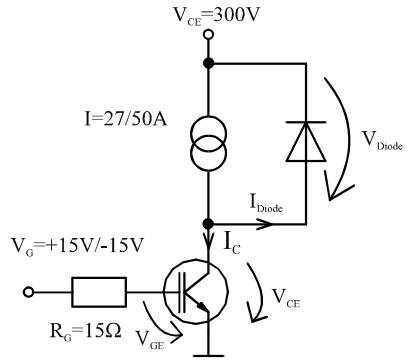

Figure 2: Schematic of the simulated circuit

Figure 2 shows the schematic for the evaluation of the turn-on and turn-off energies, while Figure 3 summarizes the definitions for the device characterization and comparison. The times t_{Won} and t_{Woff} are needed for the estimation of the turn-on and turn-off energy, respectively.

The simulations consider NPT-IGBTs with a common planar gate structure, varied backside doping and wafer thicknesses. The lifetimes for holes and electrons are both 50µs. Table 1 summarizes the simulated NPT device types.
The simulated PT-IGBT (PT_Sim) is a previously optimized structure with a 5µm, $2*10^{17}cm^{-3}$ n-doped buffer layer and a 65µm, $1*10^{14}cm^{-3}$ n-doped drift region. The lifetimes for electrons and holes are 0.6µs. The published data sheets of two fabricated 600V/50A PT-IGBT modules are used for comparison purposes (PT_1, PT_2) [7],[8]. Table 2 summarizes the PT devices.

TABLE 1 - Simulated structures of the NPT-IGBTs

	NPT 100a	NPT 100b	NPT 80
Doping of Drift Region [cm^{-3}]	$1.4*10^{14}$	$1.4*10^{14}$	$1.8*10^{14}$
Wafer Thickness [µm]	100	100	80
Backside Doping Peak [cm^{-3}]	$1*10^{17}$	$5*10^{17}$	$1*10^{17}$
Gate Resistor R_G [Ω]	15	15	15
Current density at 50A [A/cm^2]	150	150	150

TABLE 2 - Overview about the PT-IGBTs

	PT_Sim	PT_1	PT_2
Gate Resistor R_G [Ω]	15	22	51
Doping of Drift Region [cm^{-3}]	$1*10^{14}$	-	-
Thickness of Drift Region [µm]	65	-	-
Doping of Buffer Layer [cm^{-3}]	$2*10^{17}$	-	-
Thickness of Buffer Layer [µm]	5	-	-
Substrate Doping [cm^{-3}]	$5*10^{18}$	-	-
Current density at 50A [A/cm^2]	150	app. 150	-

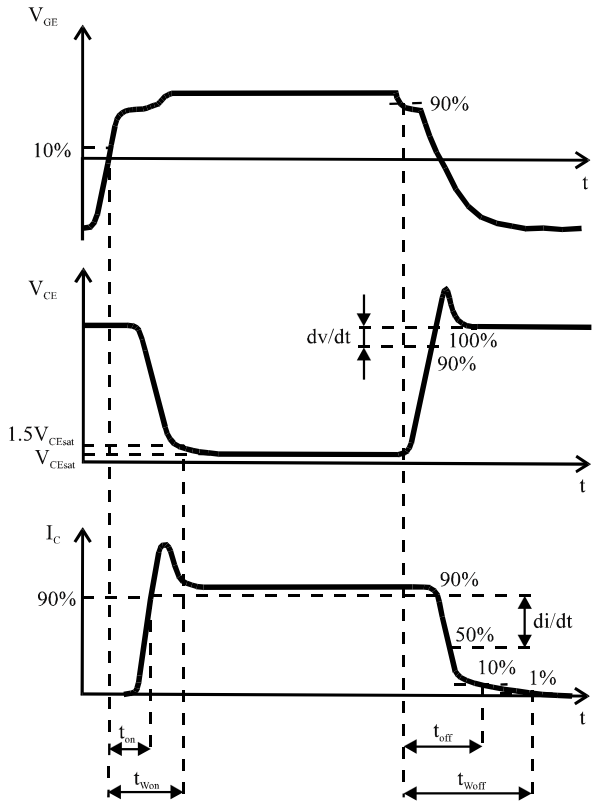

Figure 3: Definitions for device characterization

FORWARD BLOCKING CAPABILITY

First the drift region doping of the NPT-IGBT is examined to achieve a low forward voltage drop while avoiding the breakdown in the forward blocking state of the device. Figure 4 shows the dependence of the breakdown voltage on the device structure. Substrate thickness and doping are varied to find the optimum.

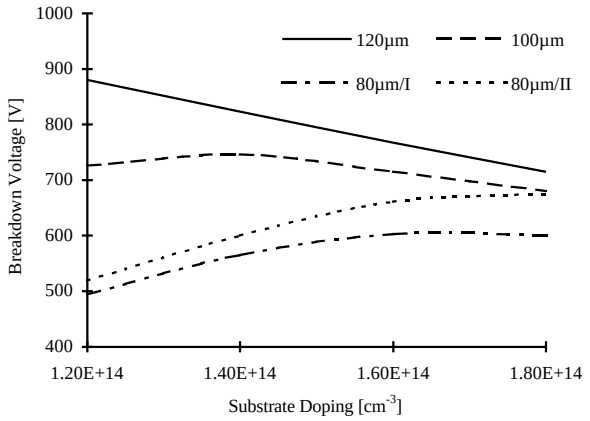

Figure 4: Breakdown voltage versus substrate doping (NPT-IGBT)

Two different dopings of the backside emitter are used in case of the 80µm device: $5*10^{17}cm^{-3}$ for type I, $1*10^{17}cm^{-3}$ for type II.

While the 120µm device has a sufficient blocking ability over the entire doping range, the 100µm and 80µm devices have lower breakdown voltages. The 100µm device shows its maximum breakdown voltage at a doping density of $1.4*10^{14}cm^{-3}$.

In case of the 80µm device with the higher backside doping (type I), the breakdown voltage is too low (app. 600V). A blocking capability of 675V is achieved using a lower backside doping (type II). The main reason for this higher blocking capability is the lower emitter efficiency of the pnp-transistor. The properties of the backside emitter are mainly controlled by the parameters of the backside implantation process (dose, energy). The lower emitter efficiency leads to a decrease in the leakage current and a later initiation of impact ionization compared to the 80µm NPT device type I.

In addition, it is necessary for the device type II to use a higher substrate doping of $1.8*10^{14}$ cm^{-3} (Figure 4) in order to achieve a sufficient breakdown voltage.

The breakdown voltage of the simulated PT-IGBT is about 700V.

CONDUCTION LOSSES

Figure 5 and Figure 6 show the on-state voltage drops of the IGBTs as a function of the collector current for a temperature of 300K and 400K.

The positive temperature coefficient of the on-state voltage is typical for NPT-IGBTs. This property of NPT-IGBTs is the result of a reduced carrier mobility in the drift region.

PT-IGBTs are known to have either positive or negative temperature coefficients depending on the operating point of the device. It is possible, and frequently noted, that a change of the temperature coefficient takes place in one curve. The main reason for this behaviour is the different and varying influence of components with a positive or negative temperature coefficient, such as the backside emitter diode characteristics, the channel resistance or the drift region resistance. All of the investigated PT-IGBTs show a slightly negative temperature coefficient in the examined current range.

The fact of a positive temperature coefficient is a clear advantage of the NPT-IGBTs, enabling an easy paralleling of chips in one module.

Both of the available PT-IGBTs have approximately the same on-state voltage drop, while the NPT-IGBTs show a greater difference. The NPT 100b shows the lowest forward voltage drop due to the highest emitter efficiency, followed by the 80µm device. The NPT 100a has the highest voltage drop due to the 100µm drift layer compared to the 80µm device (both devices have the same backside emitter with a lower emitter efficiency).

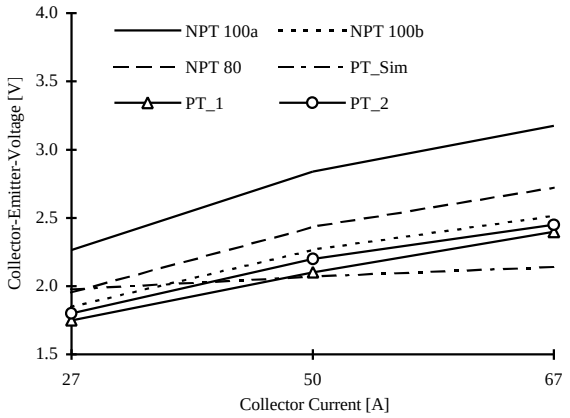

Figure 5: IGBT on-state characteristics at T=300K

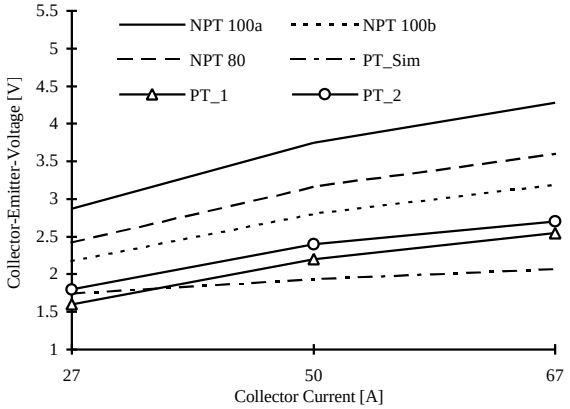

Figure 6: IGBT on-state characteristics at T=400K

SWITCHING LOSSES

Turn-on behaviour

Figures 7-8 show the turn-on losses of the IGBTs. For the PT_1 device data are available for a temperature of 400K only .The increase of the turn-on losses with increasing temperature is caused not only by the IGBT, but also by the changing reverse recovery of the free-wheeling diode.
In general, the simulated devices show much higher turn-on losses than the commercial available devices. This is probably related to the properties of the free-wheeling diode. The correct simulation of free-wheeling diodes for fast switching systems is still a widespread problem in two dimensional device simulators. The reason for this is that lifetime killing processes are introduced during the diode fabricating. An exact simulation needs more extensive models for a correct description of the recombination processes.

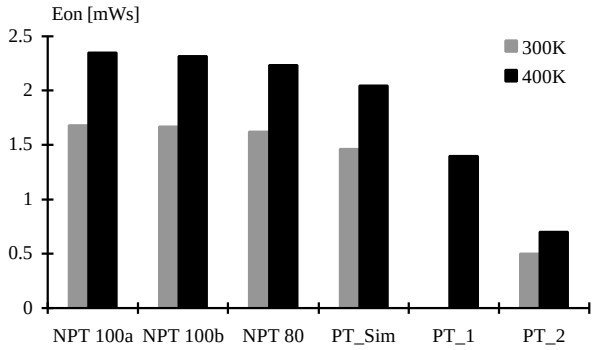

Figure 7: Comparison of IGBT turn-on losses at I_C=27A

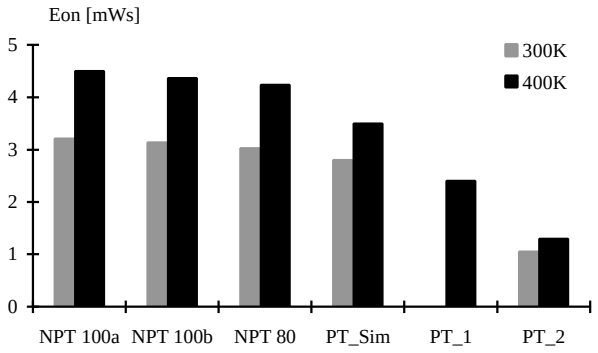

Figure 8: Comparison of IGBT turn-on losses at I_C=50A

While the NPT-IGBTs have similar turn-on losses, the PT-IGBTs show greater differences. The reason for this are variations in the device structures, the different reverse recovery of the free-wheeling diodes and, in case of the commercial available devices, of the differences in technologies.

Turn-off behaviour

The turn-off behaviour of IGBTs is characterized mainly by the tail current flow and its temperature dependence. The tail current is caused by the large minority carrier charge in the n-base region of the IGBT after turning-off the device. This charge is subsequently removed by recombination of the carriers only.

The turn-off losses of the IGBTs are shown in the Figures 9-10. For the PT_1 device data are available for a temperature of 400K only. They obviously vary more than the turn-on losses.

NPT-IGBTs have a comparatively low but long tail current (up to some microseconds). An advantage of this structure is the good temperature stability of the tail current value which only increases slowly with temperature. That is why the turn-off losses at a temperature of 400K are not significant higher than at 300K and below the values of the PT-IGBTs.

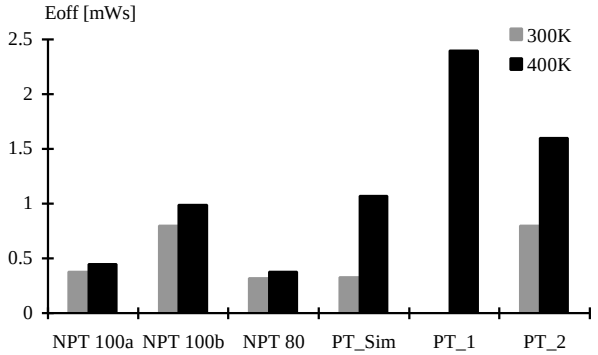

Figure 9: Comparison of IGBT turn-off losses at I_C=27A

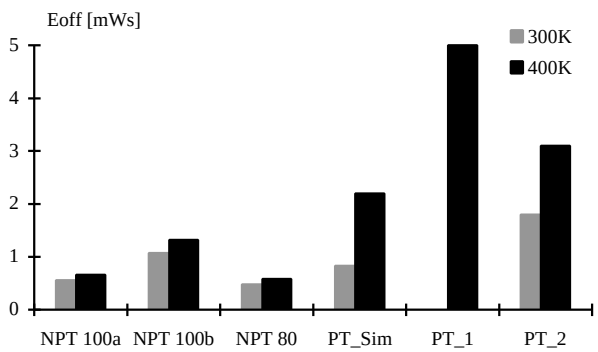

Figure 10: Comparison of IGBT turn-off losses at I_C=50A

At low temperatures all of the IGBTs have similar turn-off losses because of comparable starting values of the tail current. The high increase of the turn-off losses with temperature for the PT-IGBTs is caused by the longer carrier lifetimes at higher temperatures. NPT devices in general have very long carrier lifetimes. It is obvious that the influence of carrier lifetime will be much higher in devices with short lifetimes such as PT-IGBTs, than in devices with a long carrier lifetime.

TOTAL POWER LOSSES

As can be seen in Figures 11-14, the total power losses of the IGBTs are calculated as a function of the switching frequency for a middle duty cycle (0.5) and a load current of 27A (Figure 11,12) and 50A (Figure13,14).

Based on the total power losses, it is possible to estimate the maximum switching frequency of the devices.

In general, the total power losses increase for higher temperatures and higher switching frequencies due to the rising sum of turn-on and turn-off energies. The PT_2 commercial available device shows the lowest total power losses of all investigated devices at a collector current of 27A (Figures 11,12). In the higher frequency range the 80µm NPT IGBT shows comparable total power losses in relation to the simulated PT structure and the PT_1 device.

The result of the comparison at a collector current of 50A is very similar (Figures 13 and 14). The best properties are shown by the fabricated PT_2 device and by the simulated PT-IGBT. The NPT-IGBT with a wafer thickness of 80µm shows good results for higher switching frequencies, while the NPT100b device shows a better behaviour at lower switching frequencies.

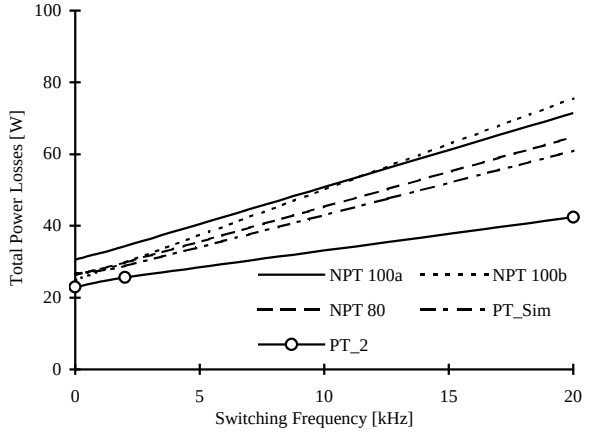

Figure 11: Trade-off at I_C=27A and 300K

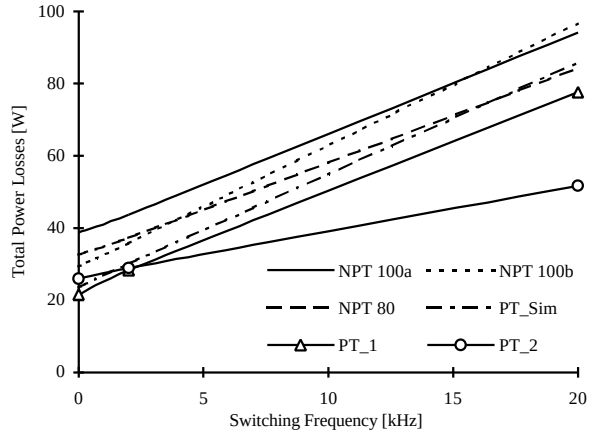

Figure 12: Trade-off at I_C=27A and 400K

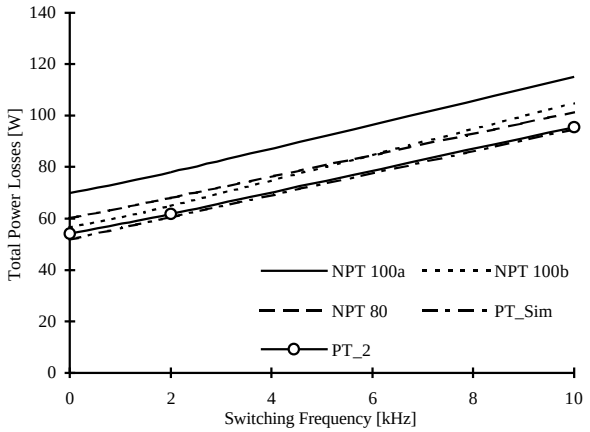

Figure 13: Trade-off at I_C=50A and 300K

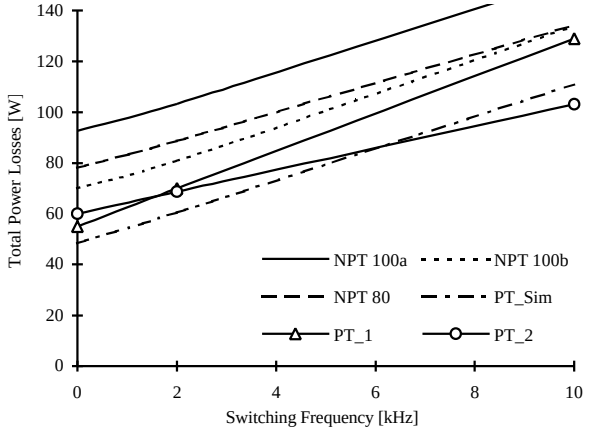

Figure 14: Trade off at I_C=50A and 400K

A further increase of the switching frequency as shown in the Figures 13 and 14 leads to thermal problems due to overriding the maximum junction temperature.

RATES OF VOLTAGE INCREASE AND CURRENT DROP

The rates of voltage increase and current drop during turn-off are increasingly important parameters for the characterization of a power switching device.
These parameters must be known in order to ensure the reliability of the device itself as well as for the designer of power electronic appliances due to the requirements of electromagnetic compatibility.

Rates of voltage increase

TABLE 3 - Rates of voltage increase du/dt [kV/µs]

		NPT 100a	NPT 100b	NPT 80	PT_Sim
I=27A	T=300K	16.2	11.1	9.3	6.48
	T=400K	10.3	4.86	15.4	4.91
I=50A	T=300K	17.4	12.1	15.3	6.67
	T=400K	15	11.8	14.9	2.82

Table 3 lists the results of the simulations at a collector current of 27A and 50A. The NPT-IGBTs show a higher rate of voltage increase than

the PT-IGBT. In case of the high load current of 50A and a temperature of 400K, the rates of the NPT devices are about 4 times higher than those of the PT device.

These high rates cause disturbance spectrums with high frequency components in the power supply grid. This means that the requirements on the net filter quality are greater.

Rates of current drop

The calculated rates of current drop are shown in Table 4. In comparison with the PT-IGBT, the NPT-IGBTs show very high rates of current drop during turn-off which may cause various other problems.

First, a high rate of current drop generates voltage peaks at stray inductances. These peaks may lead to the destruction of the IGBT under critical operating conditions (short circuit, over current range) by exceeding the safe operating area (SOA). In that cases the destruction of the device may occur by impact ionization.

Second, a high rate of current drop does not only generate a disturbance spectrum in the power supply grid, but also radiates a higher magnetic noise.

The application of the NPT-IGBTs obviously results in the necessity of a very low inductive design to prevent problems in electromagnetic compatibility.

TABLE 4 - Rates of current drop di/dt [kA/µs]

		NPT 100a	NPT 100b	NPT 80	PT_Sim
I=27A	T=300K	4.47	2.3	4.15	1.62
	T=400K	3.93	1.9	3.17	0.5
I=50A	T=300K	16.7	6.34	22.3	3.52
	T=400K	12.4	6.13	12.3	0.97

CONCLUSION

Simulated NPT-IGBTs with a blocking voltage of 600V are investigated and compared to simulated and fabricated PT-IGBTs. Based on wafers with a thickness of about 100µm, NPT devices are able to compete with the PT devices. Although the 600V NPT-IGBT does not match the properties of an optimized, sophisticated PT-IGBT, the device show some advantages.

The investigated NPT-IGBTs have similar conduction losses at a temperature of 300K. Because of the positive temperature coefficient, the conduction losses increase with rising temperature. This leads to higher conduction losses as in the case of the PT-IGBTs.

In this work, the NPT device clearly shows higher turn-on losses. A reduction of the turn-on losses is possible by the development of specially optimized diodes. Thus, an improvement in the commutation of the current from the diode to the IGBT is expected. But, due to the basic device structure, the turn-on losses will remain higher than those of a PT-IGBT.

The NPT-IGBTs obviously have lower turn-off losses than PT-IGBTs, especially at higher temperatures. Another advantage of the NPT device is the good temperature stability of the tail current, which increases very slowly with rising temperature.

Thus, the trade-off between total power losses and switching frequency shows advantages for the PT-IGBT. Nevertheless, the NPT-IGBT is competetive. The main advantage of the NPT-IGBT is the lower price of the device due to the much simpler fabrication by offering good properties. Because of the thin wafer the device is expected to have a much better power dissipation than the PT-IGBT. For fabrication, further improvements in wafer handling are required.

The higher rates of voltage increase and current drop during turn-off are a problem. They result in a higher frequent disturbance spectrum. Thus, a very low inductive design of applications is necessary to fulfill the requirements of electromagnetic compatibility for 600V NPT-IGBTs.

Acknowledgements

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