600 V power device technologies for highly efficient power supplies

Ralf Siemieniec, Rene Mente, Wolfgang Jantscher, David Kammerlander, Ute Wenzel
INFINEON TECHNOLOGIES AUSTRIA AG
Siemensstrasse 2, A-9500 Villach, Austria
ralf.siemieniec@infineon.com
http://www.infineon.com

Acknowledgements

The authors would like to thank our colleagues from the Villach application engineering team for their support over the past years, especially Matteo Kutschak and David Herrera Meneses for the design of the 3.3 kW CCM Totem Pole PFC and many helpful discussions. Our thanks go also to Ying Pang, Michael Brambach, Martin Bernauer, Nurmarizah Umar, Izzaty Haziqah Mohd Nadzar and Richard Proch for their intense support in device characterization and application tests.
We also want to thank Adrian Finney for carefully editing this article.

Keywords

power semiconductor device, super junction devices, wide bandgap devices, power supply, efficiency

Abstract

Switched mode power supplies (SMPS) for target applications covering a wide range from telecom rectifiers through servers to solar inverters or electric vehicle chargers share the need for high efficiencies in order to minimize the overall energy consumption and the total cost of ownership. With the appearance of wide bandgap semiconductors, designers cannot only choose between different devices but also may benefit from using advanced topologies. This work compares the properties of the latest generations of a CoolMOS™ Superjunction (SJ) device with integrated fast body diode, of a CoolSiC™ Silicon-Carbide MOSFET and of a CoolGaN™ E-mode GaN power transistor in the 600 V class. The device behavior is discussed with a view to its use in the AC-DC conversion power factor correction (PFC) stage of a power supply. It is shown how the technology-specific parameters impact the different aspects of the application performance and the choice of topology. This understanding may also act as a guideline for an adequate selection of the best-suited device technology for a given application beyond the scope of AC-DC conversion in power supplies. However, this comparison does not discuss solutions which can address device limitations with the application of dedicated circuitries as, for example, the solution recently proposed for CoolMOS which enables efficiencies close to that of wide bandgap devices [1].

1. Introduction

The three device technologies with a voltage rating of 600 V to 650 V differ substantially in their device structure in order to benefit most from their respective semiconductor material. The fundamental device exemplary structures are shown in Fig. 1 in order to explain the basic device properties [2-4]. The SJ- and the SiC-MOSFET are both vertical structures. However, the purpose of the incorporated p-regions in the vertical structure is different. While the SJ p-columns provide charge compensation to optimize the trade-off between low on-resistance and high breakdown voltage, the buried p-region of the SiC-MOSFET limits the electric field at the gate oxide to gain the required oxide lifetime. Both devices have the drain on the backside and represent truly vertical device structures. The SiC device requires a roughly ten times smaller drift region length, enabling both a strongly reduced area-specific on-resistance $R_{DS(on)}$ and small reverse recovery charge Q_{RR}. In contrast, the GaN device consists of a lateral structure placed on a (not shown) Silicon substrate. The Silicon backside is electrically isolated but typically tied to the source potential. The GaN device is based on the heterojunction High Electron Mobility Transistor (HEMT) structure and does not contain physical

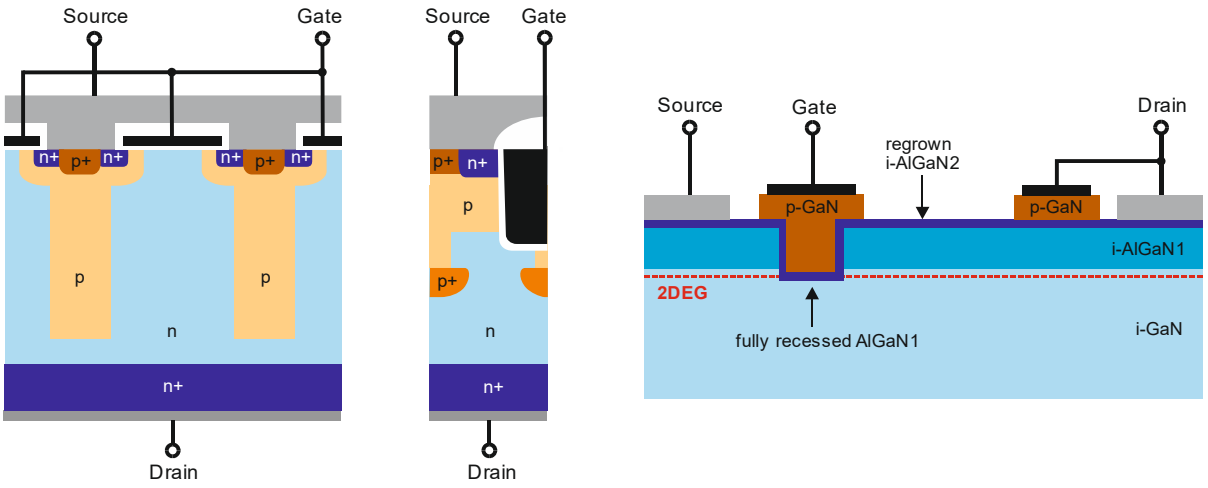

Fig. 1: Exemplary device structures: SJ-MOSFET [1], SiC-MOSFET [2], E-mode GaN Power Transistor [3]

pn-junctions between source and drain. Instead, the channel builds through a highly conductive two-dimensional electron gas (2DEG) at the AlGaN/GaN interface. To achieve a normally-off (or E-mode) device, a recessed p-GaN gate is provided to locally interrupt the 2DEG. This GaN transistor can be operated not only as a power switch, but also as a diode in the reverse direction with practically zero reverse recovery charge Q_{RR}. Note that the recessed Gate is non-isolated and acts like a diode, calling for a dedicated gate drive circuitry as discussed later.

2. Application requirements

Fig. 2 shows the main building blocks of a power supply designed for a universal input voltage range of 85 – 265 VAC. The compared devices are intended for use in the AC-DC conversion power factor correction (PFC) stage. The different device properties require the use of different topologies. Fig. 2 employs a common Boost PFC stage typically used with SJ devices. The typical operating frequency is limited to 70 kHz to keep the fundamental and 2nd harmonics below 150 kHz due to EMI reasons. A higher operating frequency also clearly increases the switching losses. The typical control mode is the Continuous Conduction Mode (CCM) as here the ripple current losses and switching losses are well balanced. The PFC stage may also be operated in Discontinuous Conduction Mode (DCM) or Critical Conduction Mode (CrCM) at the cost of a much higher ripple current while at the same time enabling quasi Zero Voltage Switching (ZVS) for reduced switching losses. However, the input bridge rectifier is in all cases the dominant source of losses, causing alone an efficiency loss of between 1 % and 2 %. The switching losses of the transistor P1 strongly depend on the energy stored in the output capacitance, consequently it is good to use devices with low E_{OSS} values in this topology. To achieve a higher efficiency, the use of a Dual Boost PFC stage is possible [5,6]. As shown in Fig. 3, the higher efficiency is paid for with a higher effort on the system side. Another alternative topology offering comparable efficiency is the H4 PFC [5].

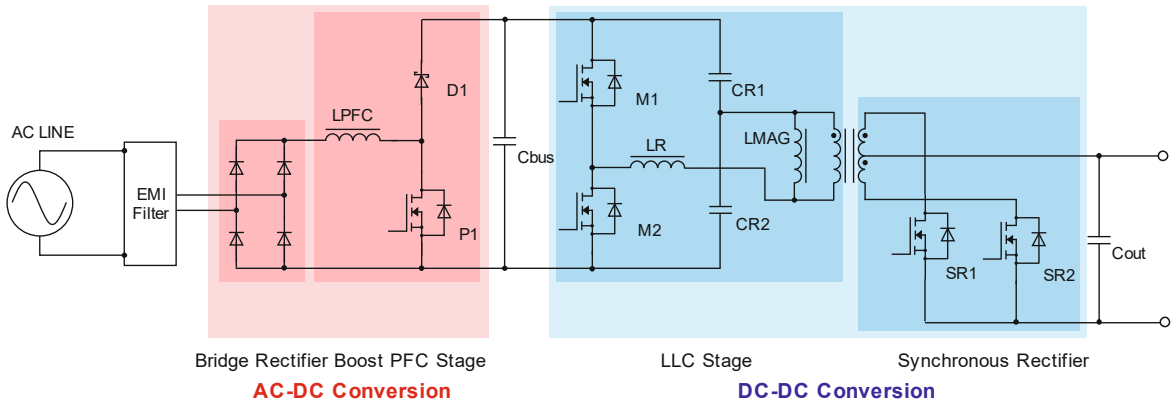

Fig. 2: Main building blocks of a power supply

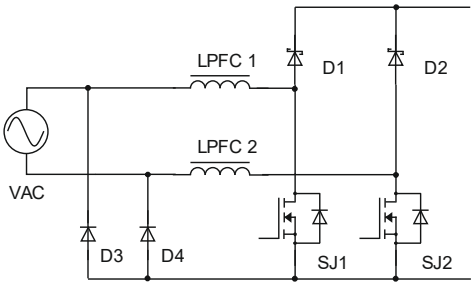

Fig. 3: Schematic of a Dual Boost PFC stage (use of two SJ devices and two SiC Schottky diodes)

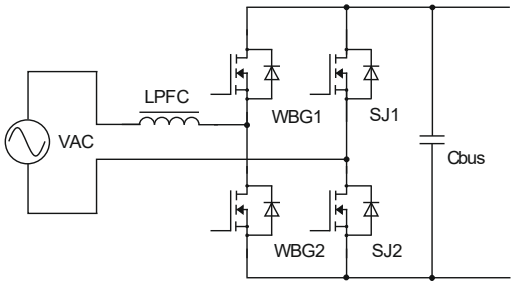

Fig. 4: Schematic of a Totem Pole PFC stage (use of two WBG devices and two SJ devices)

A better alternative topology is the totem-pole PFC as depicted in Fig. 4 [7]. This bridgeless topology eliminates the need for traditional bridge rectifiers that contribute substantially to the overall losses in the PFC stage. While being a rather simple topology, the totem-pole PFC is intrinsically capable of providing a bi-directional power flow and provides the highest practically achievable efficiency. However, the topology imposes serious challenges to the power semiconductors.

The switching frequency of the power semiconductors WBG1 and WBG2 is relatively high with values of up to 100 kHz, with one transistor working as a boost switch and the other as a synchronous rectifier. The totem-pole is usually operated in Continuous Conduction Mode (CCM), however other control modes including DCM or CrCM may be employed as well [8]. In any case, this topology requires devices with low values of reverse recovery charge Q_{RR} to enable the repetitive hard commutation operation of a conducting body diode. The output capacitance dependency on the drain voltage must avoid sharp drops, in addition a low output charge Q_{OSS} is needed to facilitate short dead times and to enable higher switching frequencies. Further, this low output charge together with a small value of E_{OSS} helps gaining high efficiencies. Wide bandgap devices provide all these properties and are a perfect match for this topology.

3. How device technology impacts the device parameters

3.1. Thermal Considerations

Being wide-bandgap semiconductor devices, the chip area for SiC and GaN devices of a given on-resistance is several times smaller than for a SJ device. A smaller area leads to an increase in the thermal resistance from junction to case R_{thJC}. SiC is advantageous in terms of its much higher thermal conductivity of 360 W/m K compared to 150 W/m K for the other two devices. This better thermal conductivity largely compensates the increased R_{thJC} value due to the reduced chip area. In contrast, the GaN device is limited here by the thermal conductivity of the Silicon substrate. As it is a lateral device, the chip area gets somewhat larger compared to a SiC MOSFET. However, this cannot fully compensate for the increased thermal resistance, and a good thermal design becomes crucial. Note that a higher thermal conductivity is also beneficial for the lateral heat spreading within the chip itself as illustrated in Fig. 5. This is important for two reasons: Firstly, the heat is generated only in the active area of the chip and not in the surrounding parts which are required for other tasks like providing a proper electrical edge termination etc. Secondly, the heat is not generated over the full thickness of the

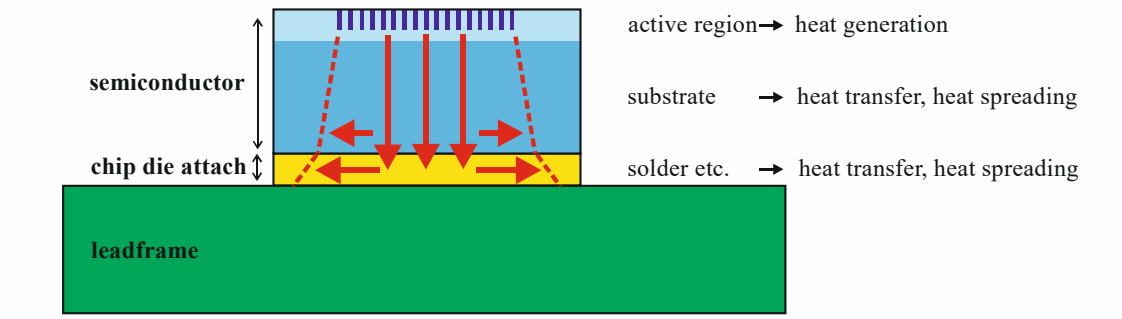

Fig. 5: Simplified illustration of heat flow (red arrows) and heat spreading (dashed lines) in the power device

semiconductor die. Instead, almost all of the power dissipation occurs within the active region of the device. Its thickness depends on the properties of the semiconductor material. Wide bandgap semiconductors require much less thickness here than Silicon and a higher thermal conductivity helps spread the heat across the full chip area. In addition the die attach from the chip to the lead frame plays a significant role. The use of a traditional soft solder process introduces a solder layer with a thickness of up to 120 µm. This increases the thermal resistance from junction to case and limits the thermal performance especially for smaller chips. Diffusion solder processes [9] enable much thinner layers for the die attach and, in addition, the use of thinner semiconductor substrates. Both supports the achievement of lower values of the thermal resistance R_{thJC}.

3.2. Temperature dependence of on-resistance

The temperature dependence of the on-resistance, shown in Fig. 6, indicates another important difference between the investigated device technologies. The $R_{DS(on)}$ of SiC-MOSFET shows the smallest increase with junction temperature T_J. From an application point of view, a small increase of on-resistance with temperature offers an additional benefit. It means that if all devices come with an identical $R_{DS(on)}$ at the datasheet condition of 25 °C, the on-state resistance for the typical operation junction temperature of 100 °C of the silicon SJ device is more than 45 % higher and for the GaN device it is 25 % higher than the value of the SiC MOSFET.
Considering the thermal behavior discussed before and the junction temperature dependence of the on-resistance, the SiC device shows the best overall performance. To give an example, a CoolMOS CFD7 57 mΩ device operated at a temperature of 100 °C could ideally be replaced by a 62 mΩ CoolGaN device or by a 84 mΩ CoolSiC part. An appropriate selection of the device on-resistance at the targeted operation temperature is key to enabling cost savings and, at the same time, achieving substantially lower dynamic losses.

3.3. Differences in the transfer characteristics

Another aspect that needs to be considered is the proper choice of the gate drive voltage. While the CoolSiC devices can generally be used with the same standard gate drivers as CoolMOS parts, this is not recommended due to differences in the transfer characteristics.
Fig. 7 compares the transfer characteristics for all three technologies at temperatures of 300 K and 450 K. Here, the CoolMOS device already reaches the full current capability with gate voltages of V_{GS} = 10 V. In contrast, the characteristics of the CoolSiC device shows a lower transconductance. Therefore, the use of higher gate voltages gives a benefit as the on-resistance reduces. Fig. 8 illustrates this behavior plotting the $R_{DS(on)}$ dependence on the applied gate voltage over temperature. From these considerations, it is recommended to use a gate drive voltage of V_{GS} = 18 V for the CoolSiC devices.
The further comparison of the different transfer characteristics depicted in Fig. 7 indicates that the impact of junction temperature is lowest for the CoolSiC part. In contrast, the CoolGaN devices reach the required current capability at much lower gate voltages due to the low typical achievable threshold

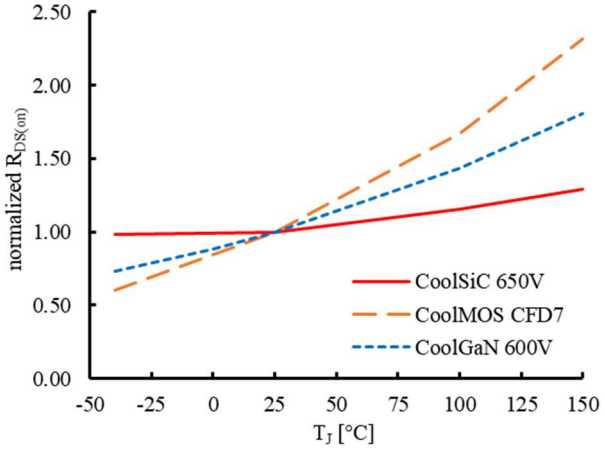

Fig. 6: Normalized temperature dependence of $R_{DS(on)}$ for the different device technologies

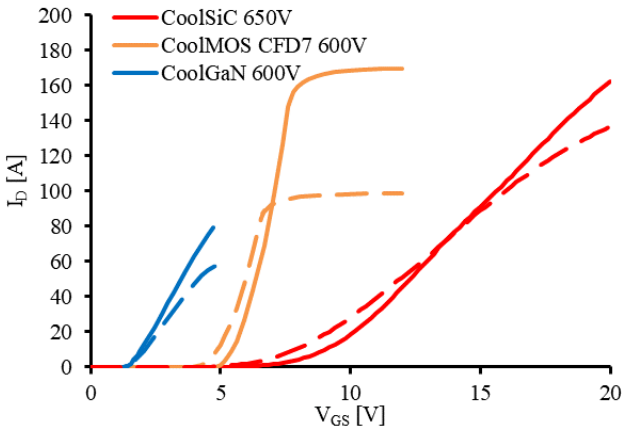

Fig. 7: Transfer characteristic comparison at two temperatures (solid lines – 25 °C, dashed lines – 150 °C)

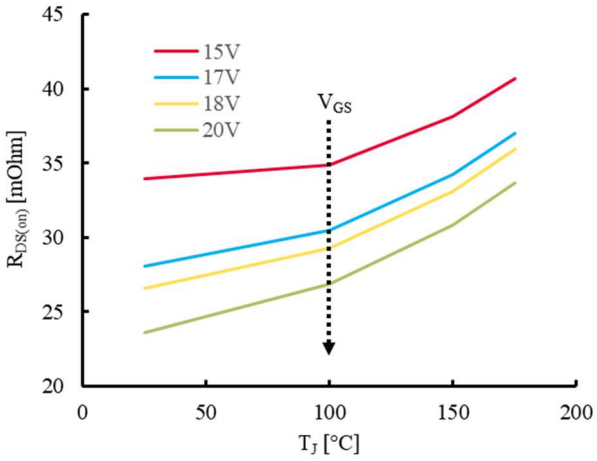

Fig. 8: $R_{DS(on)}$ vs. V_{GS} over temperature for a 27 mΩ 650V CoolSiC-MOSFET

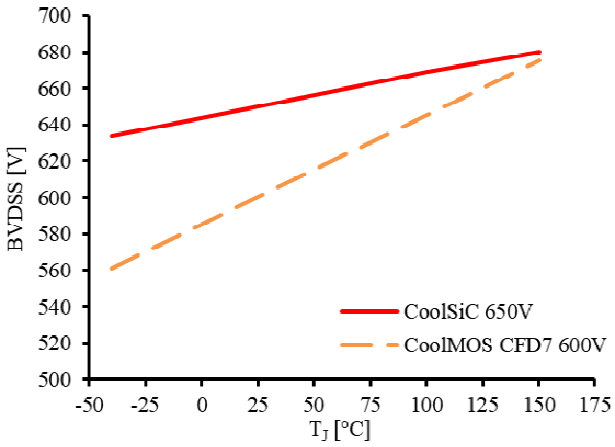

Fig. 9: Comparison of temperature dependence of breakdown voltage for CoolMOS and CoolSiC devices

voltage of 1.2 V. To gain immunity against unwanted parasitic turn-on, a negative gate voltage of down to V_{GS} = -5 V should be considered for use of these parts in hard-switching totem-pole configurations.

3.4. Device breakdown

Due to the differences in the properties of the semiconductor materials and the device structures, also the drain-source breakdown behavior differs between the device technologies.
In case of the two MOSFET devices, the breakdown mechanism is due to impact ionization at a pn-junction once the electric field in the device structure exceeds the critical electric field strength. The breakdown voltage is temperature dependent and governed by the impact ionization rates that reduce at elevated temperatures, therefore the breakdown voltage increases with temperature. Fig. 9 compares the temperature dependent breakdown voltages of the silicon and silicon-carbide devices, indicating a stronger dependence for the silicon part. From an application point of view, the higher breakdown voltage at low temperatures for the CoolSiC devices is beneficial for usage in outdoor applications or if devices need to start up at lower temperatures.
In case of the GaN device, the breakdown mechanism is different due to the lateral device structure [10]. Here, the breakdown is not limited by the critical electric field of the semiconductor but by the dielectric strength of the surface materials in the GaN HEMT structure. Therefore, the breakdown mechanism is a dielectric breakdown mechanism similar to the one found in ceramic capacitors. In turn, this behavior requires a destructive failure limit that must be at least 50 % larger than the maximum rated peak voltage of the device in order to safely avoid device degradation. This different breakdown behavior as well as the much higher breakdown voltage are clearly visible in the breakdown characteristics as depicted in Fig. 10. Different to the MOSFET devices, the CoolGaN device shows an exponential current increase.

3.5. Forward voltage of body diode

There are significant differences in the body diode conduction between the three device technologies. The CoolMOS and CoolSiC devices both incorporate an intrinsic pn-diode structure as is usual for a power MOSFET. Nevertheless, the forward voltage of the SiC device is around four times higher than that of the silicon MOSFET due to the wide bandgap of the silicon-carbide material. The forward voltage V_F shows a negative temperature coefficient for both materials. Due to the larger conduction losses of the CoolSiC body diode it is not efficient to use the intrinsic diode to conduct current over long periods of time. The impact on the light-load efficiency in an LLC converter can be as big as 0.5 %. Therefore, it is recommended to limit body diode conduction to dead-time operation and otherwise employ synchronous rectification to limit the body diode conduction losses. Applying synchronous rectification has the additional benefit that the positive temperature coefficient of $R_{DS(on)}$ supports current sharing.

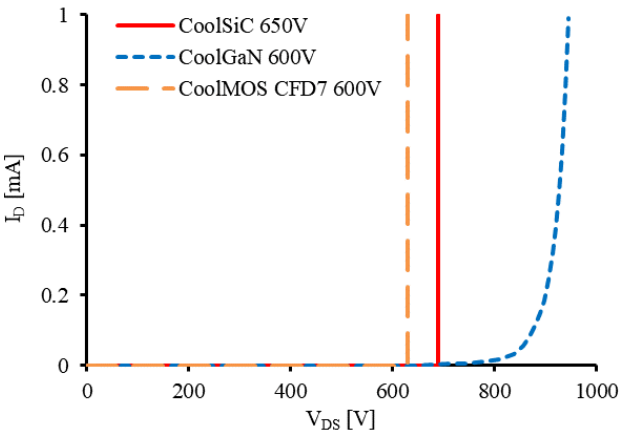

Fig. 10: Breakdown characteristics for the different device technologies at room temperature

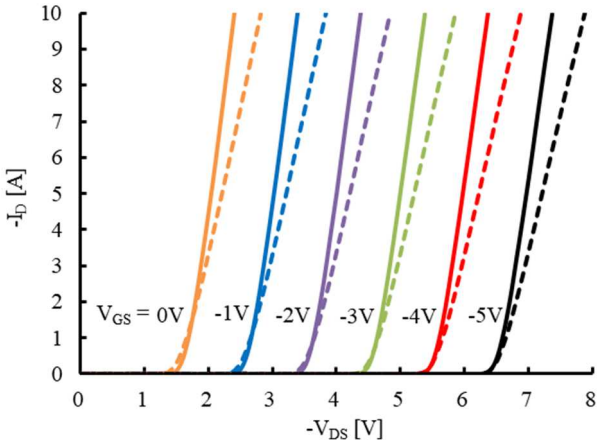

Fig. 11: CoolGaN 3rd quadrant characteristics at two temperatures (solid lines – 25°C, dashed lines – 125°C)

In the case of the CoolGaN device, the structure does not incorporate an intrinsic diode structure. However, with the gate driven to the on-state, the GaN HEMT will conduct current equally well in either direction, just like a MOSFET. If the gate is turned-off at $V_{GS} = 0$ V and the drain potential exceeds the gate threshold voltage, the HEMT structure turns-on and begins conducting in the reverse direction with a voltage drop of about 2 V. Applying a negative gate-source voltage will shift the onset of reverse conduction appropriately and the "diode-like" voltage drop increases as depicted in Fig. 11. Consequently one should also limit this "diode-like" conduction mode to a brief period during the dead-time between switching intervals as in the case of SiC devices.

3.6. Gate drive considerations

The gate drive requirements are identical for SJ- and SiC MOSFETs, however the SiC device benefits a lot from a higher $V_{GS} = 18$ V as indicated in Fig. 8. In contrast, the GaN device is a gate injection transistor (GIT) and the required gate driving scheme differs significantly in comparison to the other two devices. Different to the MOSFET devices, the CoolGaN device has a non-isolated gate with a pn-diode between gate and source. The forward voltage V_F of 3.0 … 3.5 V is defined by the GaN band structure. It is evident that the V_F must always be higher than the threshold voltage of the transistor, which is ensured by the comparably low achievable threshold voltage of GaN devices. However, it is this gate diode that requires a different driving scheme compared to conventional MOSFETs.
As for any MOSFET, the switching speed depends on the gate current available in the Miller plateau phase. In the case of a GaN device with a non-isolated gate, a permanent current I_{SS} will flow into the gate diode during on-state, see Fig. 12. As this current causes additional losses, it should be kept as small as possible. On the other hand, gaining low switching losses requires large peak currents I_{ON} and I_{OFF} in the transition phases. To achieve such a behavior, the classic gate resistor is substituted by an RC network that provides two parallel branches as depicted in Fig. 13. Here, a small resistor R_{ON} is coupled to the gate via the capacitor C_C while a large resistor R_{SS} provides the direct current path for the stationary on-state. This capacitor C_C now provides the required charge to drive the transient

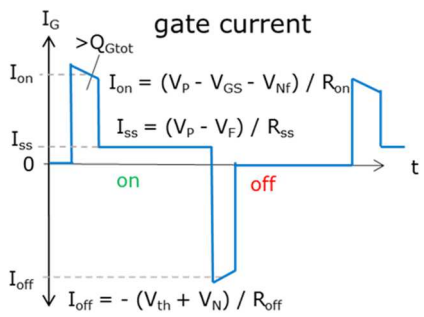

Fig. 12: Driving scheme of the CoolGaN™ E-mode GaN Power Transistor

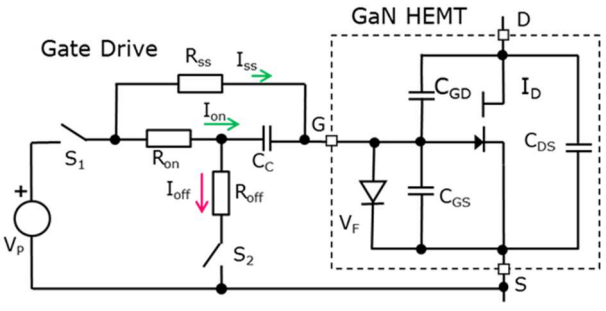

Fig. 13: Equivalent circuit to properly drive the gate of the GaN Device

current I_{ON} defined by the value of the resistor R_{ON}, assuming the values of the parts are properly dimensioned [11]. If the device is turned-off, the gate-drive voltage level shifts to negative values again due to the capacitor C_C. This guarantees a fast turn-off transient and the avoidance of a potential re-turn-on.

3.7. Capacitances and Charges

Fig. 14 - Fig. 17 compare the output capacitance, the output charge, the energy stored in the output capacitance, and the gate charge of the three different technologies using devices with a comparable on-resistance of 50 - 55 mΩ at nominal current and room temperature (e.g. for normal datasheet conditions). With respect to the output capacitances as shown in Fig. 14, the CoolMOS technology offers a smaller output capacitance than both wide bandgap devices at V_{DS} >20V. Therefore, the CoolMOS is capable of offering lower switching losses in a standard boost PFC application. However, the CoolMOS shows a more sensitive behavior to PCB and design related parasitic elements as well as larger V_{DS} overshoots during turn-off. At drain voltages larger than 20 V, the output capacitances of the SJ-MOSFET and the GaN device are almost identical. However, the lower output capacitance of the GaN and SiC MOSFET below V_{DS} = 20 V represents a clear benefit as it allows an overall faster transition of the drain voltage. GaN offers the lowest C_{OSS} values below V_{DS} = 20 V which translates into a lower output charge Q_{OSS} and a lower E_{OSS} of the GaN transistor as indicated in Figs. 15 & 16.
In terms of output charges, both wide bandgap devices offer a clear benefit over the SJ MOSFET. The lower Q_{OSS} value allows either the discharge of the output capacitance with a lower re-circulating current or to minimize the dead time. Short dead time settings are important in conjunction with wide bandgap devices in order to minimize body diode conduction losses related to the four times higher forward voltage drop compared to the CoolMOS device. As shown in Fig. 16, CoolSiC has a higher

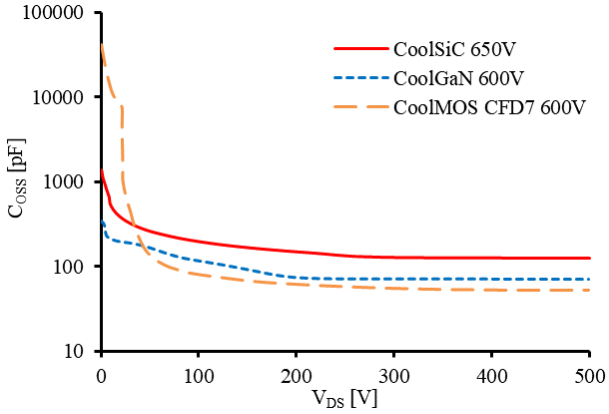

Fig. 14: Comparison of the output capacitances

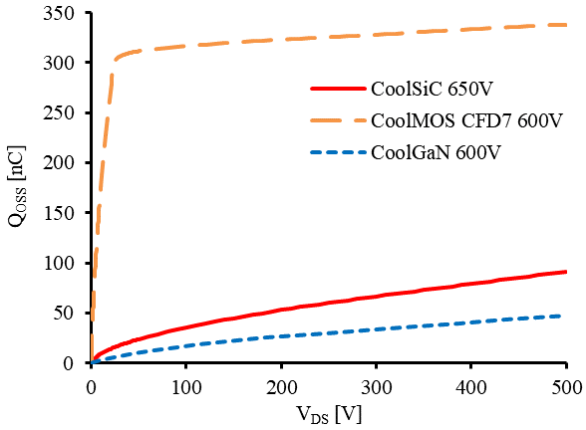

Fig. 15: Comparison of the output charges

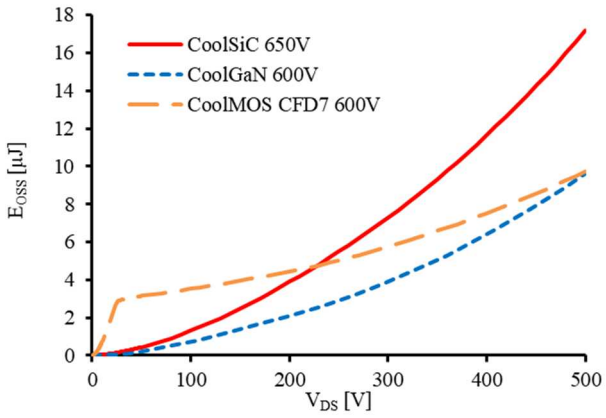

Fig. 16: Comparison of the energies stored in output capacitance

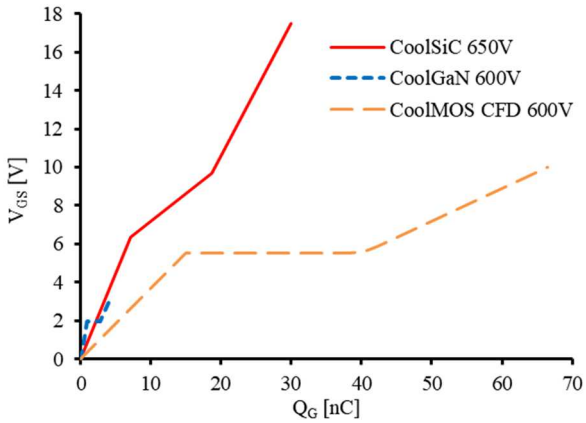

Fig. 17: Comparison of the gate charges

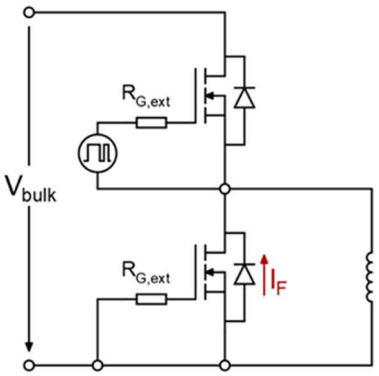

Fig. 18: Schematic circuitry of reverse-recovery test setup

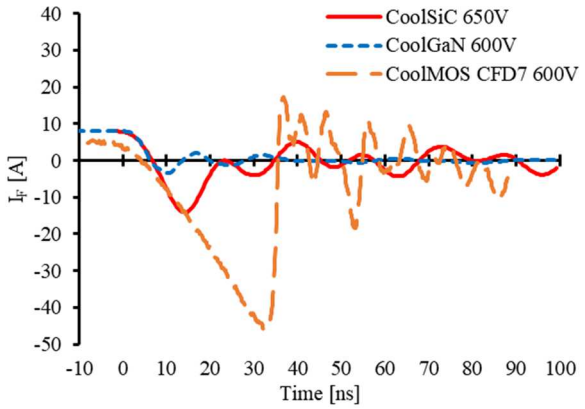

Fig. 19: Comparison of reverse-recovery current waveforms

E_{OSS} than CoolMOS and CoolGaN technology. The E_{OSS} represents the minimum energy that translates into switching losses in standard hard switching topologies. However, the large output charge together with the dramatically larger reverse recovery charge of SJ devices prevent these devices from being used in hard-switching bridge topologies such as in a Totem Pole.

Fig. 17 compares the gate charge characteristics at a drain current of ~9 A as typically used in the targeted application. Lower overall gate charge values result in lower driving losses at higher switching frequencies and enable higher efficiencies in light-load operation. Here the SiC-MOSFET shows a clearly smaller value than the CoolMOS device, nevertheless the difference gets smaller if the SiC device is driven with the recommended on-state gate voltage of V_{GS} = 18 V. In comparison, the gate charge of the CoolGaN device is substantially smaller, acting as an enabler for high-frequency applications. However the losses due to the stored energy in the output capacitance E_{OSS} remain at comparable levels to other device technologies. A high-frequency operation will be most efficient in soft-switching or resonant topologies.

3.8. Reverse Recovery Charge

The reverse-recovery charge Q_{RR} is a very important factor for any resonant switching topology such as the highly efficient hard-switching topologies like the CCM Totem Pole PFC discussed in this work. This charge is build-up during conduction of the intrinsic body diode of Si and SiC MOSFET devices and needs to be removed during hard commutation of the body diode. The generated amount of charge depends on internal device properties like doping profiles, thickness of the drift layer or carrier lifetimes as well as on external conditions controlled by the application like current density, temperature or the conducting time of the body diode. The part of this build-up charge that does not recombine in the device during the body diode commutation must be removed by the reverse-recovery current over time and represents the reverse-recovery charge. Fig. 18 depicts a typical test circuit to measure Q_{RR}.

In case of the CoolMOS CFD7 technology, the amount of stored-charge was significantly reduced by a factor of 10 over the standard CoolMOS technology. Still, the stored-charge Q_{RR} remains too large to allow the use of the device in the CCM Totem Pole PFC topology. This is very different for the SiC MOSFET. Being a wide bandgap device, the drift region thickness required for the targeted blocking voltage is much smaller. Also the active area is clearly reduced compared to even the best Superjunction MOSFET on the market. As a consequence of the dramatically reduced volume of the drift region, the amount of stored charge in the device becomes significantly smaller, which is further supported by the short carrier lifetimes in SiC. It is especially this property of a low reverse-recovery charge Q_{RR} that paves the way for the use of the CoolSiC device in the Totem Pole topology and to achieve peak efficiencies beyond 99 %. A low stored-charge also supports an improved robustness in hard commutation as the risk of a snap-off at high reverse-recovery currents is much lower.

Fig. 19 compares the reverse-recovery waveforms of all three technologies, clearly indicating the much higher amount of stored charge for the CoolMOS device, although a 50 % lower forward current was running through the device. For the CoolGaN part, one cannot identify any reverse-recovery charge as the device does not contain an intrinsic bipolar diode. As discussed before, the structure

conducts in the third quadrant due to an open channel. Consequently, the "reverse-recovery" current here is purely capacitive and driven solely by the output charge of the device, giving room for a further improvement in overall efficiency.

4. Comparison of efficiency in the target application

The performance of the different devices is evaluated in the AC-DC conversion stage (PFC stage) of 3.3 kW power supplies. For the purpose of this comparison, the SJ devices are used in a Dual Boost PFC stage while the wide bandgap devices are used in a totem-pole PFC:

- CoolSiC Trench MOSFET with $R_{DS(on),typ}$ = 48 mΩ in a Totem Pole PFC
- CoolGaN E-mode HEMT with $R_{DS(on),typ}$ = 55 mΩ in a Totem Pole PFC
- CoolMOS P7 (2x) with $R_{DS(on),typ}$ = 26 mΩ in a Dual Boost PFC

The need to use different topologies for SJ and wide bandgap devices in combination with the need for varying gate drive schemes for MOSFET and GaN devices reveals a real challenge for a true performance comparison. As the measurements were performed using different evaluation boards, some uncertainties arise due to the different parasitic elements introduced by the different layouts.
However, the comparison shown in Fig. 20 reveals a clear trend of what the different technologies can deliver. Both wide bandgap devices clearly enable efficiencies higher than 99 %. The CoolGaN enables the highest peak efficiency but requires a significantly more complex driving scheme and hence more effort in the system design compared to the CoolSiC devices. The CoolMOS SJ device used in a Dual Boost configuration is capable of delivering a peak efficiency of 98.8 %.

5. Conclusion

SJ devices will remain as the first choice for the PFC stage of a SMPS with an overall efficiency below 97 %. The devices are easy to drive, offer the most granular portfolio and offer a proven quality and reliability. Due to the higher output capacitance shape at V_{DS} > 20 V, wide bandgap devices will not offer clear advantages in this topology.
The SiC MOSFET offers the best solution for SMPS with standard form factor and an efficiency range of 97 % to 98 %. This better efficiency is linked to the move to the Totem Pole topology and eliminates the need for bridge rectifiers. Although C_{OSS}, Q_{OSS} and E_{OSS} are all higher than for the GaN transistor, the SiC device clearly benefits from a much lower increase of on-resistance over temperature. The SiC transistor is easy to drive, yet it is recommended to use a gate drive voltage of

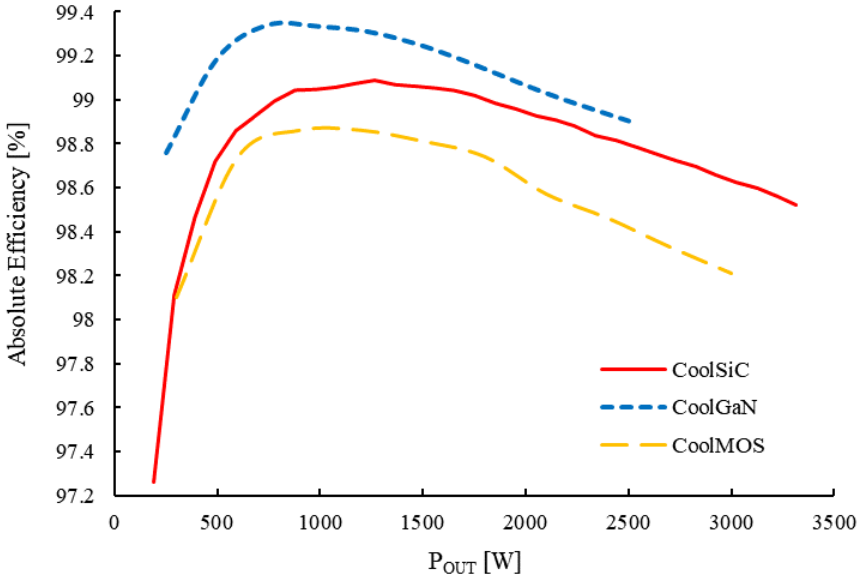

Fig. 20: Comparison of the absolute efficiency achievable in the respective 3.3 kW PFC stage (CoolSiC and CoolGaN measured in Totem Pole topology, CoolMOS measured in Dual Boost topology, V_{IN} = 230 VAC, V_{OUT} = 400 VDC, f_{sw} = 45 – 65 kHz (Dual Boost), f_{sw} = 65 kHz (Totem Pole))

18 V to benefit from the further lowered $R_{DS(on)}$. SiC MOSFET are especially beneficial for high power applications.
Solutions using GaN devices are currently capable of delivering the highest efficiencies, exceeding 98 % in standard form factor. They are the first choice for high frequency applications where the form factor is the key requirement. However, GaN solutions use a dedicated gate drive concept that requires additional effort for its implementation.
Alternatively, the application of dedicated circuitries offer an alternative path to address device limitations. For example, the efficient use of SJ devices in half-bridge configurations with hard commutation is usually prevented by the presence of high reverse-recovery and high output charges. However, this limitation is addressable by adding relatively simple circuitry using bootstrapped low-voltage supplies which provide low voltage current injection to pre-charge the output capacitance of the device [1]. Such measures enable repetitive hard commutation of the body diode at commonly used switching frequencies and offer customers further alternatives.

6. References

[1] R.A.G.Mora, M.A.Kutschak, D.Meneses, M.Escudero.: Lossless Hard-Commutated Operation of SJ MOSFETs and Application to CCM Totem-Pole Bridgeless PFC, Proc. PCIM Europe, Nueremberg, Germany, 2021

[2] G.Deboy et al.: A new generation of high voltage MOSFETS breaks the limit line of silicon, Proc. IEDM, San Francisco, USA, 1998

[3] R.Siemieniec, R.Mente, W.Jantscher, D.Kammerlander, U.Wenzel, and T.Aichinger.: 650 V SiC Trench MOSFET for high-efficiency power supplies, Proc. EPE, Genova, Italy, 2019

[4] H.Amano et al.: The 2018 GaN power electronics roadmap, J. Phys. D: Appl. Phys., Vol. 51, No. 16

[5] Y.Jang and M.M.Jovanivić.: A Bridgeless PFC Boost Rectifier With Optimized Magnetic Utilization, IEEE Transactions on Power Electronics, Vol. 24, No. 1, pp. 85-93, 2009

[6] L.Huber, Y.Jang and M.M.Jovanivić.: Performance Evaluation of Bridgeless PFC Boost Rectifiers, IEEE Transactions on Power Electronics, Vol. 23, No. 3, pp.1381-1390, 2008

[7] B.Zhou.: CCM Totem-Pole Bridgeless PFC with Ultra-Fast IGBT, Master Thesis, Virginia Polytechnic Institute and State University, Blacksburg, USA, 2014

[8] N.Mohan, T.M.Undeland and W.P.Robbins.: Power Electronics – Converters, Applications, and Design – 2nd Edition, John Wiley & Sons, USA, 1995

[9] M.Pürschel and K.Röschlau.: Diffusion soldering for automotive power MOSFETs offers the first 100% lead free die attach, Proc. EPE, Birmingham, UK, 2011

[10] E.Persson.: CoolGaN™ application note. Infineon Technologies AG, Application Note AN_201702_PL52_010. Available at: https://www.infineon.com/dgdl/Infineon-ApplicationNote_CoolGaN_600V_emode_HEMTs-AN-v01_00-EN.pdf?fileId=5546d46262b31d2e016368e4cab10701

[11] B.Zojer.: Driving CoolGaN™ 600 V high electron mobility transistors. Infineon Technologies AG, Application Note AN_201702_PL52_012. Available at: https://www.infineon.com/dgdl/Infineon-ApplicationNote_CoolGaN_600V_emode_HEMTs_Driving_CoolGaN_high_electron_mobility_transistors_with_EiceDRIVER_1EDI_Compact-ApplicationNotes-v02_00-EN.pdf?fileId=5546d46262b31d2e016368e4d7a90708