AN IMPROVED AND LOW-RESISTIVE PACKAGE FOR HIGH-CURRENT MOSFET

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Keywords

MOSFET, power semiconductor device, packaging, device application, reliability

Abstract

Over the years improved silicon technologies for low-voltage power MOSFETs have led to a very low on-resistance of the die which is now comparable or even lower than that of the device package. Modern SMD packages offer a significant reduction of the package-related resistive contribution to the overall on-resistance but are limited in the maximum useable chip size due to their small form factor. Larger dies are usually mounted into through-hole-packages or their derivatives resulting in certain limitations of their performance. In this work a new package solution especially suited for high current applications linked to high reliability requirements such as industrial motor drives or servers is discussed from the user's perspective.

The need for a new power package

Low-voltage power MOSFETs based on charge-compensation using a field-plate offer a significant reduction of the area-specific on-resistance. The first commercially available devices of this type were introduced in 2001, and since that time such power MOSFETs have become more and more dominant in the market. With silicon technology moving forward so rapidly the package becomes an increasingly important part of low-voltage MOSFETs [1]. The on-resistance of the latest device technologies has become remarkably low and the package proportion of the overall on-resistance has changed from a negligible 1:10 to a 1:1 ratio or even worse. This is especially true for devices intended for motor drive applications, as here the lowest possible on-resistance is needed, while maintaining a good thermal performance. This demand for low-resistive packages to avoid limitations of the device performance by the package characteristics has driven the development of new solutions.

Classic package solutions are represented by through-hole-packages such as the well-known TO-220 and TO-247. Such packages allow a relatively simple assembly linked to a simple thermal management. As assembly technologies moved away from through-hole to surface-mounted technologies, these packages were adapted in order to meet the changed assembly requirements. A good example is the widely used D^2PAK (or TO-263) or the smaller DPAK (or TO-252). However, these packages are derivatives of existing solutions rather than intentionally optimized packages.

To better meet recent system requirements, a number of new surface-mounted-device (SMD) packages were developed and introduced during the past years such as SuperSO8, CanPAK™ or

BLADE™. Compared to the traditional through-hole-packages, these solutions contribute significantly less to the overall device on-resistance, cause a much lower parasitic inductance and offer the capability for topside cooling. As an example, Fig. 1 visualizes the limitation of the device on-resistance for new device technologies in different packages. Here, the reduction of the typical on-resistance of a best-in-class 100 V device for the last three technology generations is compared for the pure die and best-in-class dies mounted in a TO-220, D²PAK and SuperSO8 package, respectively. Starting with 100 % as the reference for each device for the first generation, the on-resistance of the chip was reduced down to only 41 % for the third technology generation. In case of a SuperSO8 device, a reduction to 44 % is realized. This means that only an increase of 3 % is contributed by the package resistance. In case of a TO-220 device, the on-resistance of the product is reduced only to 57 % due to the large contribution of the package itself.

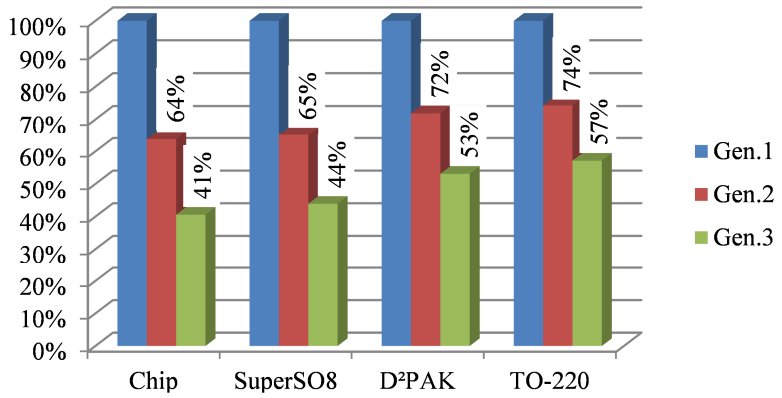

Fig. 1: Typical on-resistance reduction comparison of three technology generations on chip and package level

Despite the clearly better performance of the available SMD packages, no dedicated SMD packages for large chip sizes have so far been developed. However, drive applications in particular call for devices with the lowest possible on-resistance and a high current capability. Additionally a low parasitic inductance is advantageous to enable fast switching, while a low thermal resistance is needed to enable a good heat flow from the die to the heat sink. Further requirements with respect to drive applications are related to the need for a high reliability even under rough environmental conditions and a good solderability.

Fig. 2 analyzes for the example of a classic TO-220 how the package resistance of a best-in-class device is composed, accounting for up to 50 % of the overall product on-resistance depending on the voltage class. Obviously, the highest contribution is caused by the leads of the package, followed by the bond wires, already pointing to potential improvements. The leads are almost eliminated in a true SMD package. The resistance of the bond wires could be reduced by a larger diameter and/or a larger number of wires; however this is limited by mechanical reasons and the available space. A much better option is to reduce the length of the bond wires as much as possible.

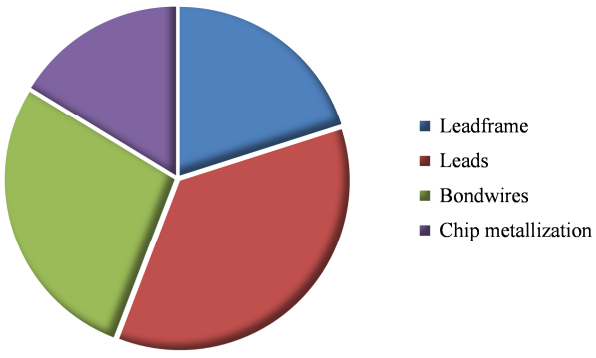

Fig. 2: Package resistance contributors for a best-in-class TO-220

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Properties of the TO-Leadless package

Electrical properties of the proposed package

The newly developed TO-Leadless package [2] addresses the aforementioned issues and all reasonable improvements were consequently implemented. What is gained is an SMD power package without external leads and up to five bond wires having a minimal length. The overall electrical resistance of the package is reduced to typically less than 0.25 mΩ. Especially at lower MOSFET breakdown voltages this reduced package resistance significantly influences the overall $R_{DS(on)}$. In a 60 V device this 0.25 mΩ package resistance already contributes one third of the overall on-resistance of 0.75 mΩ (maximum). In today´s lowest ohmic device of 0.4 mΩ at a breakdown voltage of 30 V the package resistance is already higher than the resistance of the silicon itself: 0.25 mΩ (package) vs. 0.15 mΩ (silicon, max.). Fig. 3 gives an overview of the package contribution to the on-resistance for best-in-class devices of the latest device technology in different TO packages in the medium-voltage range. It is obvious that the TO-Leadless package offers a clear benefit in all voltage classes.

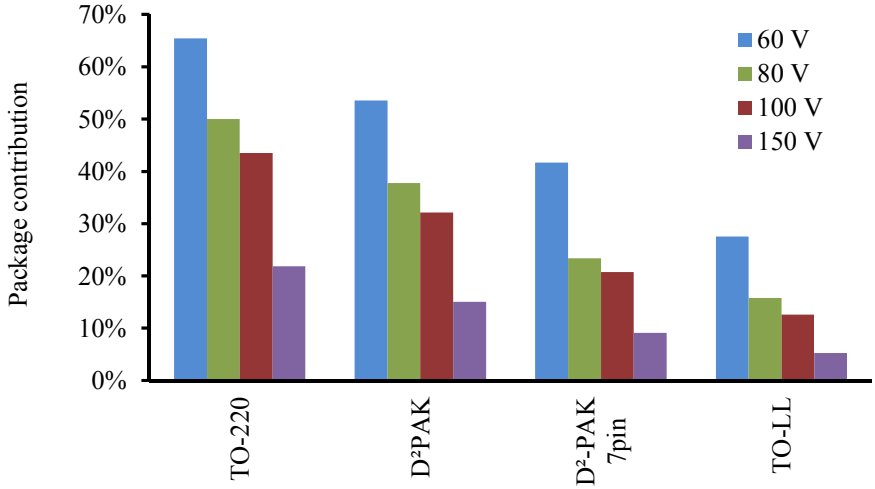

Fig. 3: Contribution of the package resistance to the overall on-resistance of best-in-class devices for different voltage classes

While the footprint of the TO-Leadless package is reduced to only 70 % of that of a D^2PAK, the solder area of the lead frame itself is unchanged. Compared to a D^2PAK 7pin, the source solder area is increased by one third. This reduces the current density at the solder connections and consequently the risk of electromigration. Fig. 4 shows the package soldered to a PCB, giving a good indication of the eliminated leads and the footprint. Fig. 5 gives an inside view and shows the large-area connection of the bond wires with the metallization layer of the die.

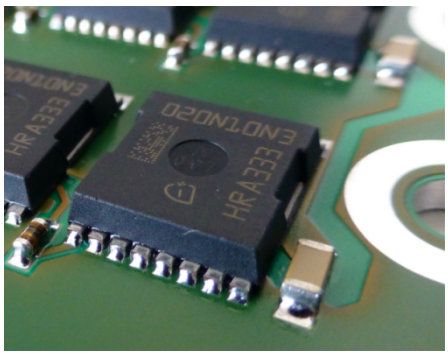

Fig. 4: TO-Leadless soldered on a PCB

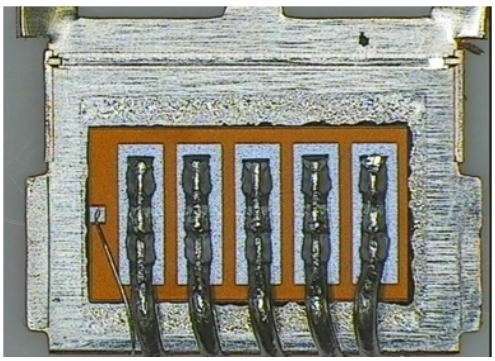

Fig. 5: View of an open TO-Leadless package

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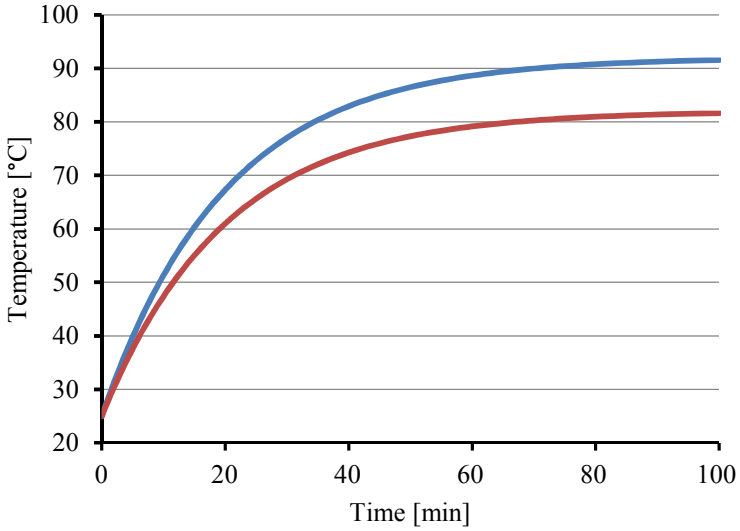

Fig. 6: Evolution of device temperature over time in a 3-phase drive application (f_{sw} = 10 kHz, V_{DC} = 24 V, I = 100 A) using TO-Leadless package (red) or D²PAK 7pin package (blue)

To prove the significance of the realized improvements, the devices were tested in a typical 3-phase motor drive application. Here 60 V OptiMOS™ 5 devices [3] with an overall area of 30 mm² were mounted in either a TO-Leadless or a D²PAK 7pin package, resulting in maximum specified on-resistances of 0.75 mΩ and 1.0 mΩ, respectively. Fig. 6 shows the evolution of the device temperature over time in this application. Looking at the device temperatures over time, a clear difference is found after only a few minutes. After 100 min the temperature difference is already 10 K. This is a clear indication that choosing the right package type can significantly increase the efficiency. The lower losses linked to reduced chip temperatures ease the thermal management and help to increase the device lifetime.

Reduction of parasitic inductance

Packages include unwanted parasitic elements which cannot be avoided. In low frequency applications the most severe parasitic is given by the ohmic package resistance. The higher the switching speed and frequency become, the more important the influence of the parasitic inductance of the package will be. The source inductance plays a particularly significant role. Packages like the well-known TO-220 have a parasitic source inductance of more than 10 nH. SMD packages like the D²PAK already show a reduction down to ca. 5 nH. For a D²PAK 7pin this unwanted inductance is further reduced due to two reasons: four bond wires are used instead of three and the number of source legs is increased from one to five. The result is a reduced parasitic source inductance of less than 3 nH.

The TO-Leadless package shows a much better performance in high frequency applications as the number of bond wires is increased from three in a D²PAK or four in a D²PAK 7pin to five. Additionally the length of these bond wires is reduced and there are no leads contributing to the overall inductance outside the package. In total this results in a parasitic source inductance of less than 2 nH, which also makes the TO-Leadless package a promising candidate for high speed/high frequency applications.

Thermal impedance

Compared to the well-established D²PAK either in the standard or the 7pin version, the main difference from a thermal point of view is the lead frame volume. In a D²PAK the lead frame has a bigger area and the thickness is 1.27 mm while the lead frame used in a TO-Leadless has a smaller thickness of 0.5 mm. The higher amount of thermally effective material (copper) in the D²PAK increases the thermal capacitance. The thermal simulation using ANSYS [4] confirms the higher energy storage capability of the D²PAK for a time frame up to 3 ms. This is indicated by the

crossing point of the two curves in Fig. 7. The better behavior is only caused by the bigger volume and resulting higher thermal capacitance of the lead frame.

At longer pulse times the TO-Leadless shows a clearly improved thermal behavior. The reason is the reduced thickness of the lead frame. Assuming a thermally effective area of 30 mm², the smaller thickness of the lead frame of the TO-Leadless and the specific thermal conductivity of copper yields an easily calculated difference of around 0.1 K/W.

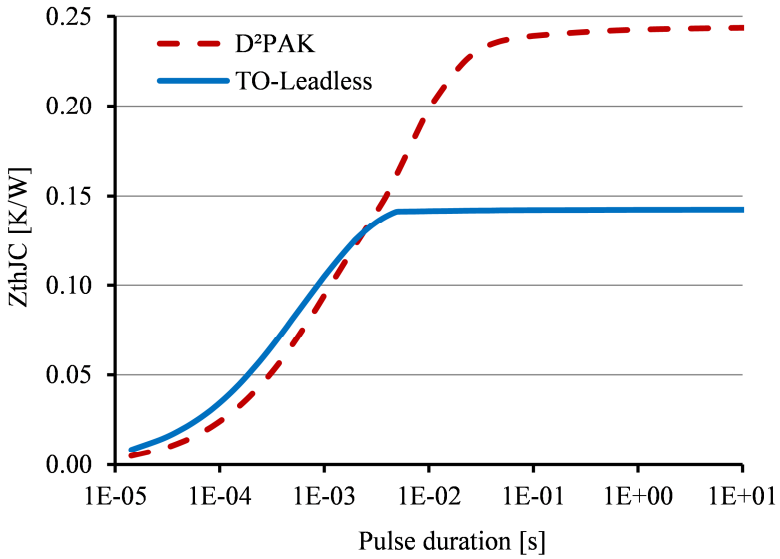

Fig. 7: Comparison of the calculated thermal impedance of D²PAK 7pin vs. TO-Leadless package (total chip area 25 mm²)

It depends on the application whether the better thermal capacitance C_{th} of the D²PAK or the better thermal resistance R_{thJC} is more important. Especially in high power motor drive applications like forklifts where SMD MOSFETs are assembled on an IMS (insulated metal substrate) PCB, the TO-Leadless with the much better R_{thJC} promises a better performance. This is due firstly to the fact that the overall thermal resistance per MOSFET position is well below 1 K/W. Secondly the critical load conditions are not short power pulses where the higher C_{th} of the D²PAK would be beneficial. Instead typical high load conditions, with up to five times the continuous load current, last from tenths of milliseconds up to 1 s in this kind of applications.

Reliability aspects

Reliability and device lifetime are of high importance especially for motor drive applications. A number of appropriate reliability tests need to be passed during the development of each new device in order to fulfill all requirements. Naturally, temperature tests play an important role. However, with respect to packages it is not the absolute value of the temperature but temperature swings which are most critical. This is easily understandable when considering the many different materials used in a power semiconductor, each having a different coefficient of thermal expansion. Additionally the solder connection to the PCB and the PCB itself must be considered.

Intermittent Operating Lifetime Test

Using Intermittent Operating Lifetime tests (IOL), also called „Power Cycling“, the reliability of the devices in the new TO- Leadless package was proven. In this test, the device is heated up by a high current flow in each cycle until the defined temperature difference is reached. The relevant standard AEC Q101 requires the device to survive a minimum of 15,000 cycles at a temperature difference of 100 K [5]. Although one only gets one measured point as shown in Fig. 8 (ΔT = 100 K at 15,000 cycles), the minimum number of cycles at different temperature differences can be calculated.

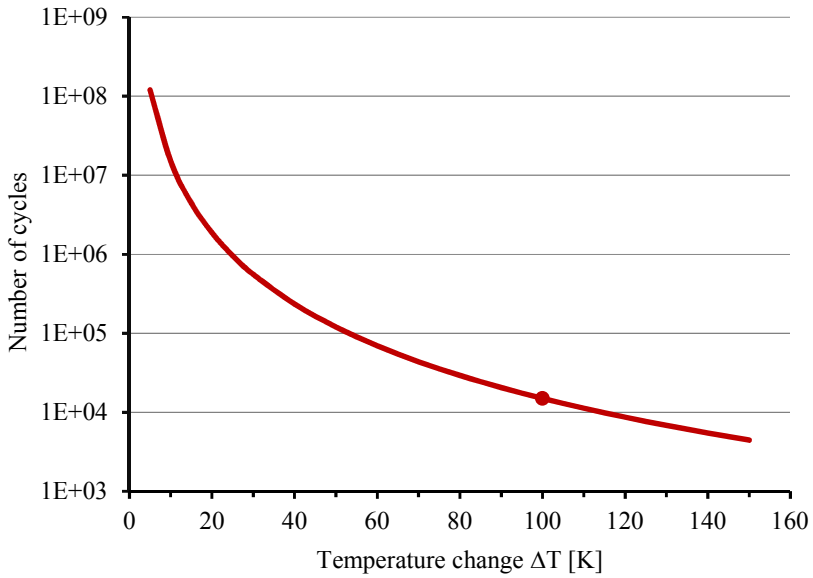

Fig. 8: IOL test of TO-Leadless and calculated number of cycles over temperature rise according to AEC Q101 standard [5]

As motor drives are subject to many alternating load conditions, 15,000 cycles might already be reached within less than two years. Packages intended for such applications should therefore be tested using a larger number of cycles. Considering that the cool-down phase of one cycle needs roughly three minutes, translating into one month for 15,000 cycles, there is a need to reduce the test time to enable such extended reliability tests. As a rule of thumb, each additional 10K temperature increase leads to a reduction of the expected lifetime by 50 % (=half the number of possible power cycles). Therefore the temperature difference was increased from 100 K to 150 K, applying a much higher stress to the MOSFET. 60,000 applied cycles using this dramatically higher stress condition did not result in any device failure or any measurable parameter drift. This corresponds to 200,000 cycles at a temperature difference of 100 K or 13 times the requirement according to the AEC Q101 standard. Fig. 9 shows the diagram including the calculated curves for different temperature rises.

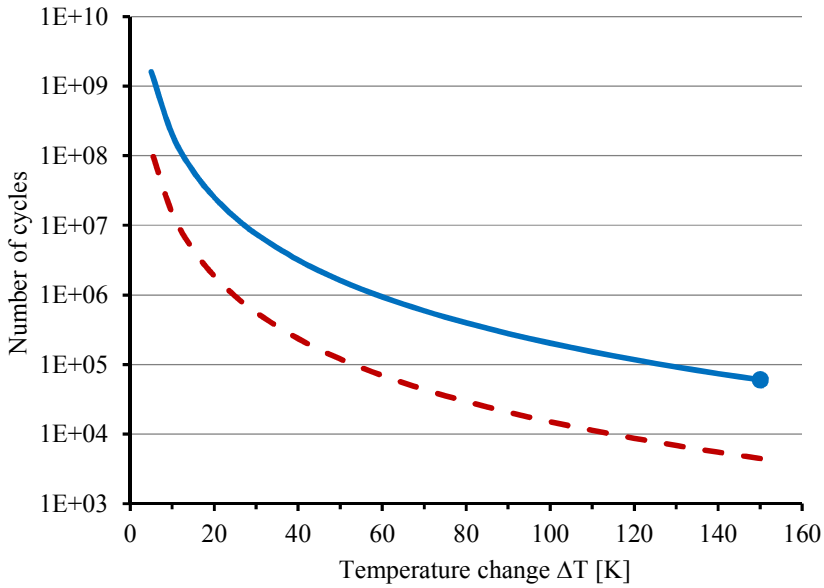

Fig. 9: IOL test of the TO-Leadless using ΔT = 150 K and a calculated number of cycles over temperature rise (blue line) vs. the requirements according to AEC Q101 standard (dotted red line)

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Inspection of solder joints

The reliability of a power electronic device is not only linked to the properties of the power semiconductor itself but also depends on the solder connection to the PCB. The quality of this joint is affected by many parameters and might result in an unreliable connection. Such an imperfect connection is often not electrically detectable at the beginning, but can lead to failure of the assembly within a relatively short time of operation. As such the judgment of the solder joint quality is very important. This check is quite simple in the case of power devices using a D^2PAK or similar - here the normal Automatic Optical Inspection (AOI) as available in almost all SMD assembly companies is sufficient. This is a very cost efficient way to do the required inspection. In the case of SMD devices having no external leads one needs to go for significantly more expensive inspection methods based on X-Rays, as the solder joints are covered by the semiconductor device itself.

Fig. 10: Schematic view of the tinned grooves on the short leads

Although the TO-Leadless package is an SMD device, the quality of the solder joint can still be evaluated by the normal AOI. This is enabled by small grooves being punched into the lead frame before the plating and tinning is applied as shown in Fig. 10. A clean, effective solder has taken place if a solder meniscus is also present in these small grooves as seen in Fig. 11. Fig. 12 shows a magnified cross section through a source connection with the solder meniscus visible on the left side (light color – solder, dark color – device pin).

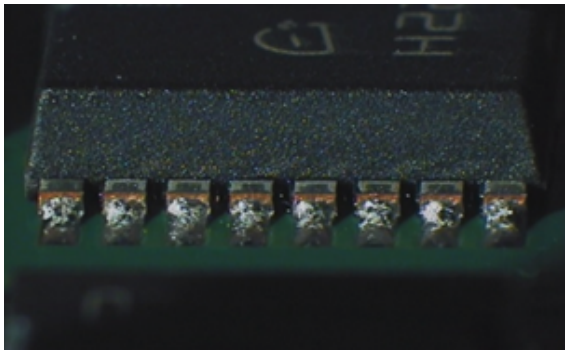

Fig. 11: Image of the leads of a TO-Leadless device soldered to a PCB

Fig. 12: Cross section through the soldered TO-Leadless device

Discussion of further improvements

The chip-to-lead frame connection ("die attach") in most packages is made by a standard soft soldering process. This method has many advantages but also a few drawbacks compared to so-called diffusion soldering [7]. Soft soldering is broadly similar to the method used when soldering SMD parts to a PCB. Solder, today mostly lead free, is applied and the chip is assembled, followed by a heating process to melt the solder material. The result is a thin layer of solder, connecting the chip and the lead frame. This process is cheap and currently the standard method. In contrast no solder layer is applied in the diffusion solder process. Instead, the chip is connected directly to the copper lead frame. This process needs special equipment and is unfortunately still much more expensive than a standard soft solder process. However there are some reasons to change from standard soft soldering towards diffusion soldering. The biggest difference between these two methods is the elimination of the solder layer. At first sight this thin layer of nominally 50 … 80 µm does not seem to have a big influence to the performance of a power transistor. Nevertheless a closer look at this solder layer reveals further details. Most prominently, this layer also contains small gas bubbles, the so-called voids. Such voids are the result of the solder process and cannot be avoided in the standard soft soldering method without additional effort. These voids not only reduce the effective solder area but also weaken the thermal connection from the chip to the lead frame. In particular if a void becomes too big cooling of the affected chip area is reduced which leads to a local hotspot. This hotspot may cause two issues. Firstly, the higher the local temperature the bigger the induced stress to the material. A reduced lifetime is the result, causing failures of the electronic equipment. The second effect which might also lead to a device failure is linked to the temperature dependence of important electrical properties. Two electrical parameters are especially affected in the case of the power MOSFET - the transconductance of the transfer characteristics, linked with the on-resistance $R_{DS(on)}$, and the threshold voltage V_{GSTH}.

It is well-known that the on-resistance $R_{DS(on)}$ of a MOSFET usually shows a negative coefficient over temperature. This means that the on-resistance increases with temperature, resulting in less current at the same voltage and as such leading to better device stability. Physically, this effect is caused by a reduced bulk mobility of the carriers. It also leads to a reduced transconductance of the device as can be seen from the transfer characteristics shown in Fig. 13. In contrast, the threshold voltage shows an unwanted behavior, as it is reduced over temperature as shown in Fig. 14. This does not trigger problems as long as the MOSFET remains fully turned-on or fully turned-off, but it might lead to difficulties during the transition process between these two conditions. Hence the switching process is a critical situation. A problem may also occur if the device is used in linear mode operation at a current condition below the crossing point of the characteristics shown in Fig. 13.

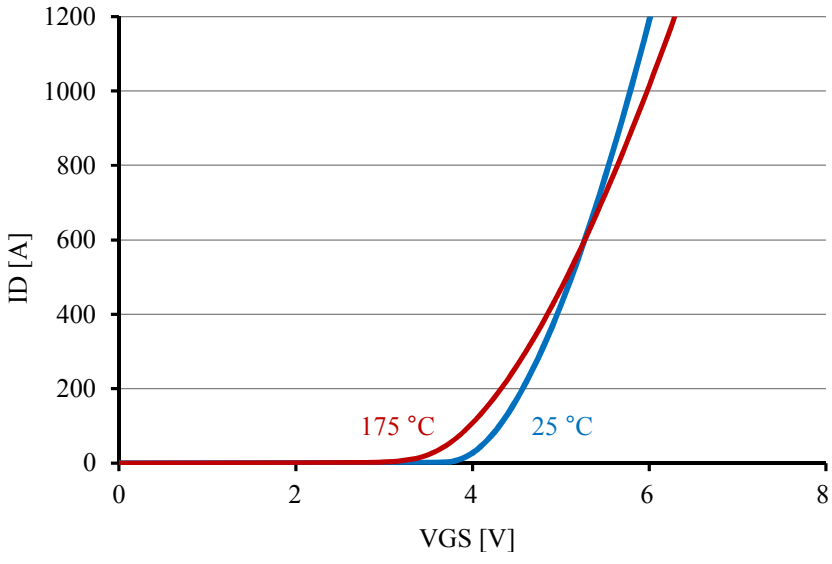

Fig. 13: Transfer characteristics for a 60 V / 7 mΩ device in TO-Leadless package (IPT007N06N)

Due to the reduced threshold voltage the MOSFET cell with a higher local temperature starts to conduct first and such handles a higher current density than the colder cells at the same case temperature [6]. This leads to locally higher losses linked to a local heat generation during the turn-on phase.

A similar effect also happens to the affected area of the MOSFET when it is turned-off, as the cells with increased temperature conduct a higher current and switch-off later than the cooler ones. Consequently the affected part of the device will further increase its temperature. Due to this unwanted positive feedback, depending on the length of the transition (with the linear operation as the worst condition), a thermal runaway can be triggered which usually leads to the destruction of the part. As voids in the solder layer directly lead to such hotspots it is easy to understand why only chips without voids or with a limited void ratio (for example less than 10% of the chip area) are allowed. As mentioned before it is hard to gain a zero void rate using standard soft solder processes, but this method can be optimized using a vacuum chamber. The result will be a nearly void-free solder layer, however manufacturing costs will be higher.

Using a diffusion solder method avoids any issue linked to voids. Additionally, as the thermal resistance of the solder layer is also eliminated, a smaller overall thermal resistance from junction to case R_{thJC} is gained. For example, in case of a TO-Leadless with a 30 mm^2 chip using a soft-solder die attach, the datasheet specifies a maximum value R_{thJC} of 0.4 K/W while the typical value is below 0.2 K/W. If the solder layer is eliminated by the introduction of a diffusion solder process, the thermal resistance is reduced by ca. 50 µK/W. Fig. 15 illustrates the improvement in a comparison of the calculated thermal impedance.

At first sight this improvement does not seem to be of any significance as the solder layer in a standard arrangement with the MOSFET assembled to a PCB is just a small contributor to the overall thermal resistance, and in most cases not the critical one. Here, the main reason is found in the poor thermal conductivity of the PCB material used, usually FR4 or similar [8]. However, this picture changes completely in true high power arrangements where a special PCB is used. Such IMS (insulated metal substrate) PCBs are formed by laminating a very thin and thermally optimized PCB material to a metal carrier. Such insulation materials show a much better specific thermal conductivity of only 2 - 5 W/(m K) compared to ca. 0.3 W/(m K) using FR4. Together with the reduced thickness of less than 80 µm of the thermal insulator, the thermal resistance of an IMS PCB is very low and reaches values of typically less than 0.4 K/W per positioned power transistor. Thus the aforementioned reduction of the thermal resistance by using diffusion soldering offers an additional benefit. This benefit helps to either increase the power handling capability of the MOSFET or to reduce the chip temperature, the latter resulting in a longer lifetime.

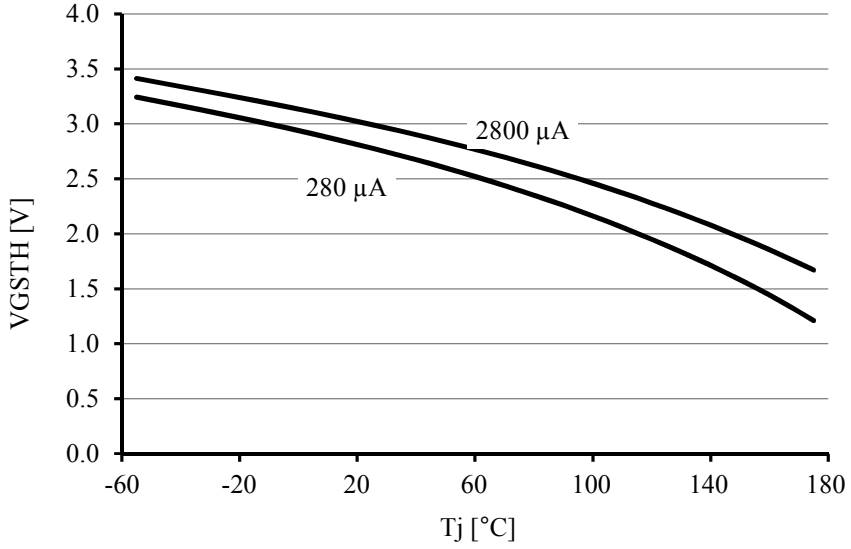

Fig. 14: Threshold voltage dependence on temperature for a 60 V / 7 mΩ device in TO-Leadless package (IPT007N06N)

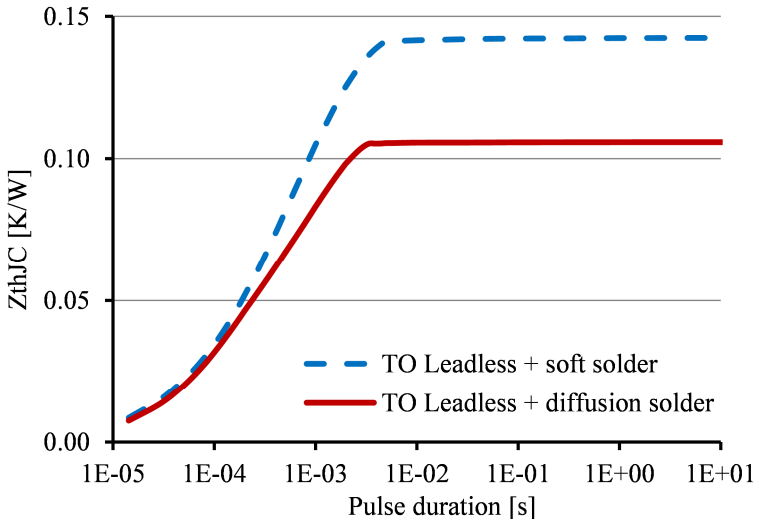

Fig. 15: Comparison of the calculated thermal impedance of a TO-Leadless package using different die attach methods (total chip area 25 mm²)

While the much higher costs of the diffusion solder process are the biggest disadvantage and currently prevent the technology from being used in most of today's applications, it still offers advantages to applications where the highest efficiencies and power densities are most important.

Conclusion

Thanks to improved silicon technologies for low-voltage power MOSFETs the on-resistance of the die has started to be comparable or even lower than that of the package itself, which is especially valid for state-of-the-art through-hole packages. Modern SMD packages offer a significant reduction of the package-related resistive contribution, but they are not able to address high-current applications due to the limited chip size and due to limitation of the current density by the available contact area. Furthermore there is also a need to reduce the parasitic inductance introduced by the package. The recently introduced TO-Leadless package addresses these issues and offers much smaller resistive and inductive parasitics, good thermal behavior and a high reliability. This work considers the properties and reliability of this package from an application point of view. Further improvements to the package using advanced solder technologies and the use of advanced materials such as IMS PCB are discussed. Despite the higher costs such measures might be beneficial for high-end applications. However, further work on these topics is needed to study and verify both the expected performance improvements and reliability of such arrangements.

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