Design of Avalanche Capability of Power MOSFETs by Device Simulation

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Keywords

Power semiconductor device, Simulation, Measurement, MOSFET, Robustness

Abstract

The avalanche behavior of new 150 V Trench Power MOSFETs was designed with the help of two-dimensional device simulation techniques. The devices employ the compensation principle for low on-state losses. A new edge-termination structure ensures that avalanche breakdown always occurs in the cell region of the device. For the transistor cells, two different destruction regimes were identified: energy-related destruction and current-related destruction. Possible simulation approaches to account for the different effects were proposed. The found dependence on design parameters based on device simulation was qualitatively confirmed by experimental results. Furthermore, strong dependence between on-resistance and avalanche current was shown.

Introduction

There is an ongoing demand for devices with lower on-state resistance and good switching behavior. Low-voltage devices are used for example in DC-DC power supplies, AC-DC adapters, Class-D amplifiers and motor drives. In all these applications, atypical switching conditions can occur, particularly

during high voltage peaks, driving devices into the avalanche mode. The aim of this work is to predict, by means of numerical simulations, the maximum avalanche current I_{as} that the transistor is able to sustain. It is well known that this current strongly depends on the load inductance L_{load} and decreases with increasing inductance. The on-state resistance and I_{as} are inversely proportional to each other; thus a trade-off exists. To simulate this trade-off for different cell design parameter variations and process variations significantly accelerates the development process and the finding of a desired optimum.

Measurement Setup

EBIC Investigations

Electron Beam Induced Current (EBIC) microscopy is a reliable tool for imaging of space charge regions, detection of electric field enhancements inside of power devices and investigation of termination structure functionality under static [1, 2] and dynamic [3] bias conditions. It has also been shown [4] that EBIC is suitable for defect characterization in MOS Field-Effect Transistors (MOSFETs) with trench gates. EBIC investigations were undertaken with a scanning electron microscope using a chopped electron beam with primary electron energy of 25 keV targeting the surface of the MOSFET. The beam generated electron hole pairs inside of the MOSFET. The free charge carriers were separated due to internally or externally applied fields, which led to a current flow. The current was measured at the source contact of the transistor using a current amplifier. The EBIC-Signal was conditioned by a Lock-In amplifier with the same reference frequency as the chopper. The Lock-In amplifier gained the measured phase and frequency sensitively thus improving the signal-to-noise ratio. By scanning the electron beam over the device, an area of approximately 130 μm x 130 μm was imaged, which was a good compromise to resolve the structure details while maintaining an overview. The spatial EBIC resolution for these measurements was determined to be 1.2 μm. The gate of the MOSFET under investigation was statically biased with $V_{GS} = -10V$ in order to ensure the blocking state of the device. The drain-source voltage was increased stepwise from 0 V to the voltage at which field enhancement occured, while the EBIC micrographs were recorded.

Figure 1 shows the measurement configuration described above. As a result of electron irradiation, electron hole pairs were also generated in insulation layers of the transistor. Due to much higher mobility of the electrons in silicon dioxide, they flowed out of the insulator and the density of holes increased with time. This led to a charge imbalance in SiO_2 [5, 6]. Therefore, the electrical properties of the device, especially the electric field distribution, changed. In addition, some positive charge carriers were trapped near an interface of the insulator [7]. The positive charging of the insulator led to an accumulation of electrons in silicon, and the drain-source channel became conductive. To counter the charging effect and

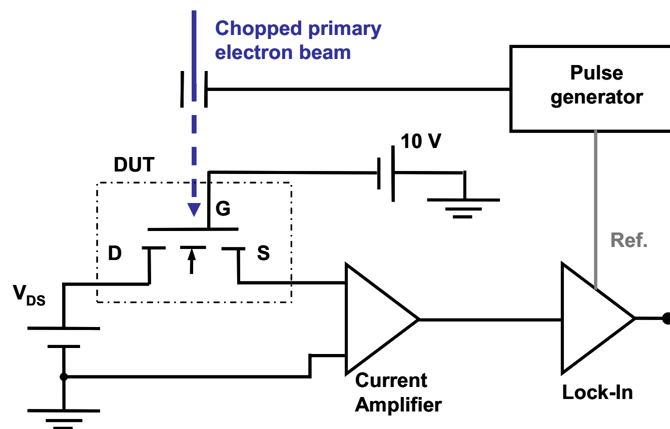

Fig. 1: Setup for EBIC measurements

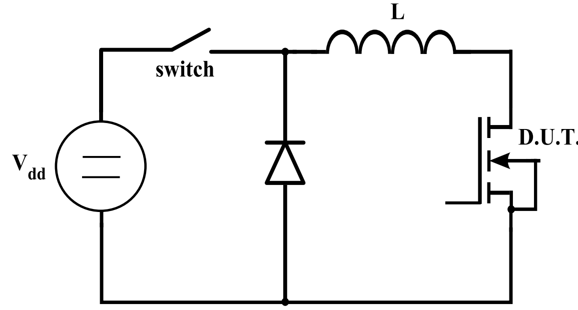

Fig. 2: Setup for UIS measurements

to be able to apply blocking voltage between drain and source, a negative voltage had to be applied to the gate. Nevertheless, the maximal blocking voltage was reduced from 150 V to approximately 50 V with increasing measurement time. This effect limited our measurement time, so the investigation needed to focus on critical areas.

Unclamped Inductive Switching Measurements

In certain applications, a failure mode called Unclamped Inductive Switching (UIS) can occur. The aim of the UIS test is to determine the maximum avalanche current the device could sustain under certain conditions.

Figure 2 shows the structure of the circuit used for the measurements. It consists of a voltage source V_{dd}, an external switch, a freewheeling diode, a load inductance L_{load} and the Device Under Test (DUT). While the transistor is turned on ($V_{GS} = 20V$) and the external switch is closed, the current ramps up in proportion to the inductance and the applied voltage. After turning off the DUT, the energy stored in the inductance

$$E = \frac{1}{2} \cdot L \cdot I^2 \tag{1}$$

must be dissipated in the transistor. A special control circuit makes sure that at the same time V_{dd} is disconnected by opening the external switch. Since the current continues to flow through the inductance and cannot change instantaneously, the transistor is forced to maintain the current. Thus it is driven into avalanche mode. The ramping process is repeated for higher currents until the device fails. Failure is detected by a rapid decay of breakdown voltage. By repeating this process with different inductances, the UIS behavior can be characterized, in particular the dependence of maximum avalanche current I_{as} on load inductance in the circuit.

Device Concept

Compensation Principle

The compensation principle for power MOSFETs was introduced in commercially available products in 1998 with the 600 V CoolMOS^{TM} Technology [8]. The basic principle behind the drastic $R_{ON} \cdot A$ reduction compared to conventional power MOSFETs is the compensation of n-drift region donors by acceptors located in p-columns, shown schematically in Fig. 3a.

The compensating acceptors are located in lateral proximity to the drift region donors, in contrast to a large vertical distance when the acceptors are positioned in the body region. In addition, the acceptors are distributed over the total drift region length, in contrast to a strong localization in the body region, which leads to a very homogeneous electric field distribution over the entire voltage-sustaining region.

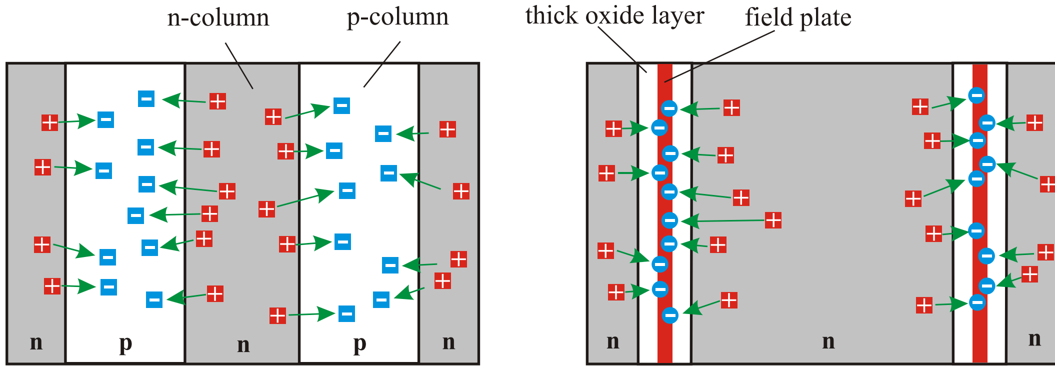

Fig. 3: a) Compensation by p- and n-columns (left) b) Compensation using a field-plate structure (right)

The requirement for precise lateral n and p dose compensation limits the n-drift region doping. This type of compensation power MOSFET is typically used for breakdown voltages of several hundred Volts. For breakdown voltages below 200 V, field-plate trench MOSFETs are an excellent alternative [9]. These devices haven a deep trench penetrating the n-drift region. An isolated field-plate provides mobile charges required to compensate the drift region donors under blocking conditions, as shown in Fig. 3b. Precise lateral drift region compensation is ensured under all operating conditions. The field-plate isolation has to withstand the full source drain blocking voltage of the device at the trench bottom; therefore oxide thicknesses in the micron range have to be regulated carefully with a special focus on avoiding thinning at the bottom trench corners and preventing generation of stress-induced defects. The drift region doping can be increased using both concepts, resulting in reduced on-state resistance. In fact, $R_{ON} \cdot A$ is even reduced below the so-called "silicon limit," which is the on resistance of an ideal abrupt p^+n junction at a given breakdown voltage not limited by any termination structures.

Edge Termination

Compensation structures make higher drift region doping possible. Consequently, conventional edge termination structures are not useable due to the high doping density, and specially formed termination structures are needed. In structures employing field-plates, a field-plate enclosing the cell array is usually sufficient to ensure the necessary breakdown strength in the edge region. However, if larger breakdown voltages appear, this simple termination structure may experience problems due to incomplete compensation. Furthermore, it is advantageous to create a termination structure whose blocking capability is equal to or higher than that of the cell array. One proposed termination structure consists of trenches that run from the cell array towards the edge region, forming several rings [10]. Field-plates inside of the trenches compensate the electric field as described before. Since the dielectric layer around each

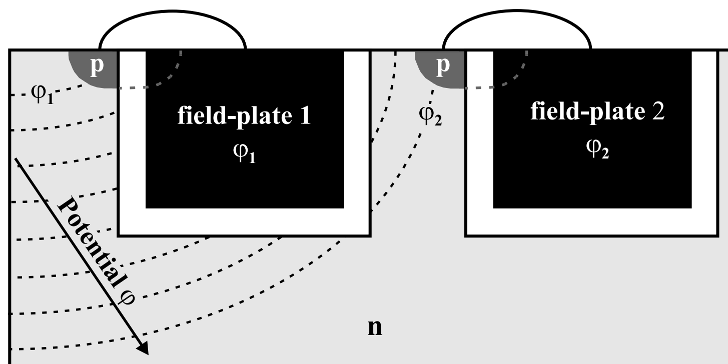

Fig. 4: Edge termination structure formed by field-plates in trenches

field-plate controls the maximum blocking voltage, the field-plate potential needs to increase from ring to ring. Therefore, each field-plate is connected to a p-well region which is reached by the electric field. The potential of the field-plate is now set to the potential prevailing in the p-well region as illustrated in Fig. 4.

For design verification purposes, EBIC measurements were used to identify and to overcome weak points in the design. For example, an inner and an outer corner of the termination structure, which are located between source and gate, are shown in the lower and upper rows, respectively, of Fig. 5.

Backscattered electron images indicate the topography of the device surface, and EBIC amplitude maps display the strength of measured signals. Since the passivation over the U-shaped gate fingers is thinner than on top of the termination structure, more generated electron hole pairs could be collected. Therefore the EBIC amplitude on the gate finger region had to be considered lower compared to the EBIC signal on termination structure. With rising drain-source voltage the space-charge region was distributed across the field-plate rings. The space-charge region extended only to the first ring and no field was applied to the following rings, except on the corner. At an applied voltage of 45 V, the EBIC amplitude on indicated locations (Fig. 5) increased rapidly. Strong electrical fields in those areas accelerated free excess charge carriers to velocities, at which charge multiplication due to avalanche effect could occur. The depth of the maximum field enhancements was determined by varying the primary electron energy, making it possible to examine different depth locations in the device. EBIC phase maps in Fig. 5c, present the phase shift between the reference signal of the Lock-In amplifier and induced currents. U-shaped gate fingers and the inner field plate were in phase with the reference signal. Since no field was applied to the other rings, the excess charge carriers diffused and recombined. Only a small fraction of the free charge carriers reached the space charge region by diffusion and were collected; therefore the EBIC amplitude was small. Diffusion processes are much slower than drift processes; the delay resulted in a phase shift.

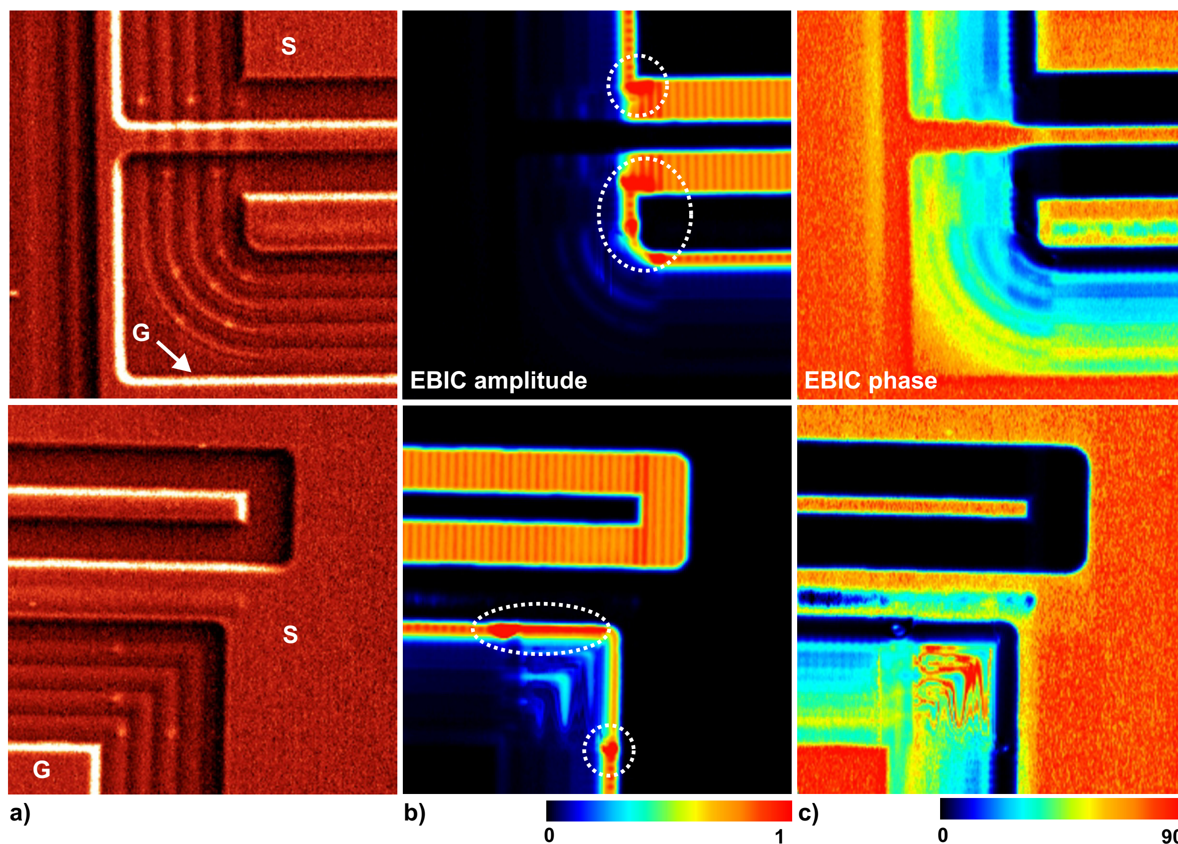

Fig. 5: a) Backscattered electron image of termination structure detail (bright color: high signal; dark color: low signal); b) EBIC amplitude map from the same region shown in (a) (normalized scale); c) EBIC phase map from the same region shown in (a) (scale in degree). Circles indicate premature breakdown locations.

Device Simulation Setup

The simulation setup for energy-related destruction has already been investigated [11, 12]. In this paper we deal especially with the behavior at higher currents, i.e. at smaller load inductances. Therefore two approaches are developed and compared. They both incorporate integration of two or more cells into the device simulation environment, and use the same external circuitry. This circuitry consists of a voltage source and the load inductance. The models are shown in Fig. 6.

The dashed rectangle symbolically represents the device on chip, separating it from the external circuitry. In both cases, the transistor cells are quasi-statically ramped up to a defined current under on-state conditions. In a steady state, $di/dt = 0$, and no voltage drop across the inductance occurs. In order to connect the transistor cells to the external circuit necessary for mixed-mode simulations, the voltage source is set exactly to the on-state voltage drop of the transistor cells: $V_{stat} = V_{DS,on}$. With these conditions the transient simulation starts and maintains the steady-state conditions for 10 ns. Then the gate voltage is ramped down at a specific rate (default 133 V/μs). If the channel ceases to exist, the drain voltage increases rapidly and the device enters the avalanche mode, when high impact ionization sets in to maintain the current through the inductance. The current then decreases with:

$$\frac{di}{dt} = -\frac{V_{br} - V_{stat}}{L} \approx -\frac{V_{br}}{L} \tag{2}$$

Both models incorporate two cells and external circuitry with V_{br} approximately 1.3 times the static breakdown voltage.
All simulations including the effects of self-heating were performed using the 2D device simulator MEDICI [13]. Thermal electrodes were placed at the bottom of the device. No thermal electrodes at the top of the device imposed worst-case conditions since no heat flow across this surface was possible. In order to increase simulation speed, heat transfer into the electrode's polysilicon was neglected. Reflecting boundary conditions were used in all simulations. The influence of top metal (Source) was discussed elsewhere [12].

Model 1: Monolithic Integration of Cells

Several cells are connected monolithically and comprise a single transistor cell (see Fig. 6a). In other words, they share the same drain contact but different source contacts. Heat transfer between cells is possible. All cells are the same size. The destruction criterion is defined as the current that leads to a maximum cell temperature during switching that is higher than a certain destruction temperature $T_{destruct}$. This value is basically determined by the doping concentration of the epitaxial layer, and in our case is set to 700 K.

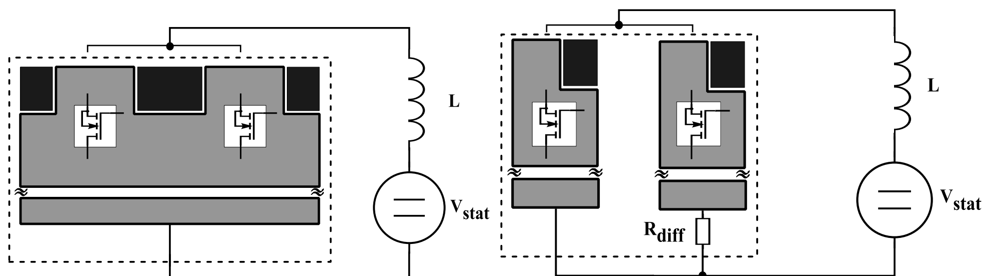

Fig. 6: Simulation approaches: a) Monolithic Integration (left) b) Mixed Mode Integration (right). Both models incorporate 2 cells and the same external circuitry. The dotted rectangle symbolically indicates the device boundaries.

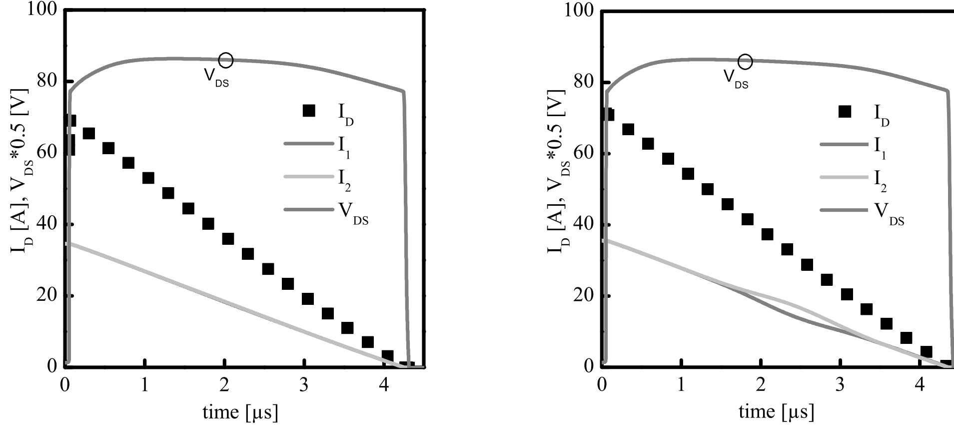

Fig. 7: Model 1 (Monolithic Integration) - a) $I_{total} = 69.3A$ (left) b) $I_{total} = 71.3A$ (right). Squares represent drain current, and grey lines indicate source currents in the two cells. V_{DS} is indicated by a small circle. In the left figure, cells carry exactly the same current, while in the right figure, one cell carries more than 50% of total current.

Model 2: Mixed-mode Integration of Cells

The second model consists of two half cells that are combined in Mixed-mode simulation and thus can be treated independently. In particular, the current density and the size of the cells can be varied. The two cells may be processed identically or not, making it possible to investigate the influences of process variations, especially over the chip area. In addition to the external load inductance, three parameters remain: The current inhomogeneity factor X, the area ratio parameter Y, and an external gate resistance R_{ext}. Thus a parameter vector $\vec{P}$ may be defined:

$$\vec{P} = \begin{pmatrix} X & Y & R_{ext} \end{pmatrix} \tag{3}$$

Assume cell 1 has to carry a current density $(1+X)$ higher than cell 2:

$$J_1 = (1+X) \cdot J_2 \tag{4}$$

with

$$A_{chip} = A_1 + A_2 = Y \cdot A_{chip} + (1-Y) \cdot A_{chip} \tag{5}$$

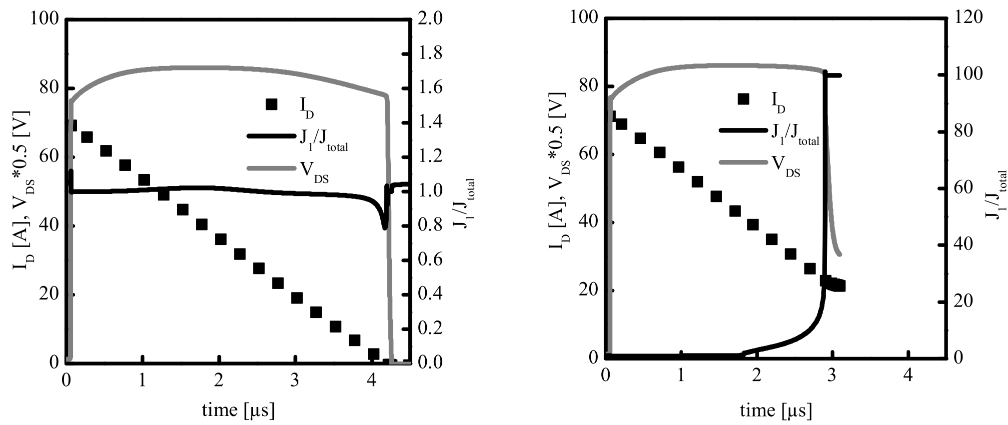

Fig. 8: Model 2 (Mixed-mode Integration) - a) $I_{total} = 69.3A$ (left) b) $I_{total} = 71.3A$ (right). Squares depict drain current, grey line drain source voltage, and black line the ratio of current density in cell 1 to total current density of device. In b) simulation swiftly reaches destructive temperatures and the simulation is then terminated.

the total current in the chip I_{total} calculates to:

$$I_{total} = (1 + X \cdot Y) \cdot J_2 \cdot A_{chip} \tag{6}$$

Due to the different current densities, the on-state voltage drop of cell 1 is higher than cell 2, i.e.:

$$V_{DS1,on} > V_{DS2,on} \tag{7}$$

In order to maintain voltage equilibrium in steady-state conditions, resistor R_{diff} has to be introduced. Its value is determined by:

$$R_{diff} = \frac{\Delta V}{(1 - Y) \cdot J_2 \cdot A_{chip}} \tag{8}$$

with

$$V_{DS1,on} = V_{DS2,on} + \Delta V = V_{stat} \tag{9}$$

The destruction criterion is identical to the one for Model 1. Model 1 is suitable for determining the effect of heat transfer between adjacent cells, whereas Model 2 predicts the influence of inhomogeneities in the cell structure on the avalanche ruggedness. Both simulation approaches were compared using the same basic transistor cell. The load inductance was set to $10\mu H$ and start temperature set to 300 K. Two different currents were investigated. The results are shown in Fig. 7 and Fig. 8, respectively. In both models, at the lower current all cells carried the same current and thus could be considered stable (see Fig. 7a, 8b). If the current increased slightly, instability effects became apparent. After a certain time (in both models $\sim 2\mu s$) currents in the cells started to differ from each other. As for Monolithic Integration, it was only a small effect and it eventually stabilized. No significant voltage drop could be observed. On the other hand, in Mixed-mode Integration, cell 1 eventually had to carry all the current, and a significant voltage drop occurs. The high current density and voltage in a minute part of the chip led to fast self-heating, even going above 1200 K in this particular region of the device. Furthermore, the impact ionization generation center relocated to the nn^+ junction when the current density exceeded a critical limit.

Simulation and Experimental Results

Model Comparison

The device's behavior under UIS conditions is of great importance for certain applications. Two different destruction regimes were detected experimentally. They depend on the value of the load inductance. One is the well-known energy-related destruction that occurs at relatively large inductances. This mechanism has already been investigated [11]. At smaller inductances, the device is destroyed well before the critical energy level is reached, i.e. at smaller currents. It has already been shown that different simulation approaches are necessary to account for these effects [12]. Our new simulation approaches were designed to examine the second effect discussed above. First we shall consider simulations by means of Model 1.

The results are shown in Fig. 9a. The transition from one destruction mechanism to the other is indicated by the kink in the curve. Simulation and measurement match quite well. Furthermore, we investigated the influence of design variations on the avalanche behavior. This is shown for six variations in Fig. 9b. The simulations agree sufficiently with measurements. The deviations can partly be related to a rather broad distribution of measured I_{as} not depicted in the figure. For Variations 4, 5 and 6 we also performed simulations using Model 2. Although the results of the simulation do not agree quantitatively with the corresponding experimental results, at least the correct qualitative behavior can be predicted. I_{as} increases monotonically both in simulation and measurement.

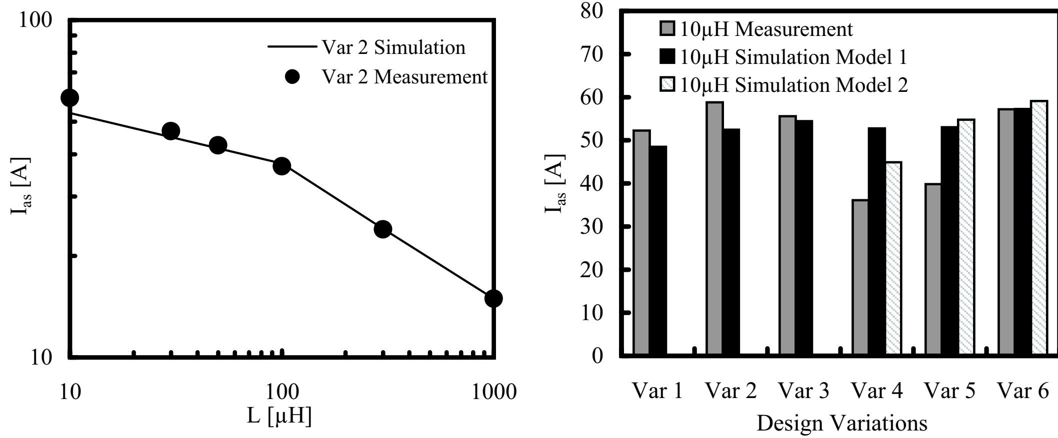

Fig. 9: a) Measurement and simulation (Model 1) of I_{as} vs. load inductance. Kink in curves indicates different destruction regimes (left)
b) Influence of design variations on I_{as}. Model 2 more accurately predicts the measured behavior than Model 1 does (right)

Dependence on Process Variations

We used Model 2 to simulate these effects. The parameters according to Eqn. 3 were set to:

$$\vec{P} = \begin{pmatrix} 0.05 & 0.01 & 1\,m\Omega \end{pmatrix} \tag{10}$$

Several devices processed with different technologies and different on-state resistances were manufactured. Experimental results and simulation results obtained by means of Model 2 are depicted in Fig. 10.

Both processes qualitatively showed the same behavior. Nevertheless, Process 2 performed significantly better in terms of avalanche robustness and on-state resistance. Yet for small Ron, experimental results were significantly worse than predicted by simulation. This effect is currently under investigation but it seems to be related to asymmetrical turn-off of different cells.

The influence of masking of p^+ implantation into the body contact groove to further suppress the turn-on of the parasitic bipolar junction transistor also showed great influence on avalanche current. If 1% of the chip area was masked, meaning that there is no additional implantation in this area, the total sustained I_{as} at $L = 10\mu H$ decreased by 25%.

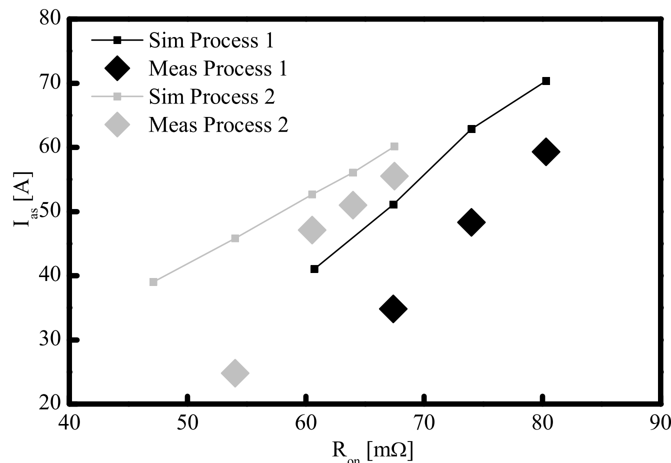

Fig. 10: Avalanche current vs. on-state resistance for two different manufacturing processes

Conclusion

The effectiveness of edge termination was investigated by means of EBIC measurements. Our tests showed at least equal breakdown behavior for edge termination than for the cell. We evaluated different simulation approaches for current-related destruction at small inductances. One approach featured monolithic integration of two or more cells, allowing investigation of heat transfer effects between cells. The other approach featured mixed-mode integration of two or more cells, allowing investigation of different switching behavior, process variations, current asymmetries and other effects not possible to simulate with a monolithic approach. Due to better scalability and enhanced possibilities to investigate process variations, the mixed-mode approach has become the standard model. We could realistically simulate the strong dependence of avalanche current on on-state resistance. The remaining deviations contributing to switching effects on the chip are currently under investigation. It is worth noting that all modeling results were quantitatively in the range of the experimental results, despite the relative simplicity of the chosen models.

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