More than an Evolution: a New Power MOSFET Technology for Higher Efficiency of Power Supplies

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Abstract

This work introduces our latest trench MOSFET technology released to the market. Based on the advantages of a revolutionary new cell design combined with the benefits of an advanced manufacturing technology, the new device technology family combines the benefits of low conduction losses and superior switching performances with an extended SOA and high ruggedness [1]. These balanced features make the devices an ideal fit especially for high switching frequency applications, supporting the trend towards significantly higher efficiency while enabling designs for higher power densities and cost effectiveness. The efficiency is studied in different applications.

1 Introduction

Since their introduction, MOSFET technologies have been noted as excellent candidates to be used as switches in power management circuits. Vertical diffused MOSFET (VDMOS) structures, commercially available since the late seventies, first addressed the needs of a power switch (Fig. 1a) [2]. The superior switching performance together with a high input impedance placed the MOSFET as an attractive alternative to the bipolar technologies that dominated the power semiconductor arena at the time.

Nevertheless, the high on-state resistance limited the current-handling capabilities of the VDMOS and hence its use in power electronics applications. For medium-voltage devices, the total on-state resistance between drain and source was set by the intrinsic channel resistance, and by the JFET region between the body regions that limits the channel current flow into the drift region (Fig. 1a). It took more than a decade of development in device design and process engineering to overcome these limitations in the late 1980s with the commercialization of the first trench gate power MOSFETs, which set a milestone for the broad adoption of field-effect transistors in the power electronics industry [2,3]. By aligning the channel along the vertical direction, the JFET region was virtually eliminated and the cell pitch dramatically reduced (Fig. 1b). The ultralow specific

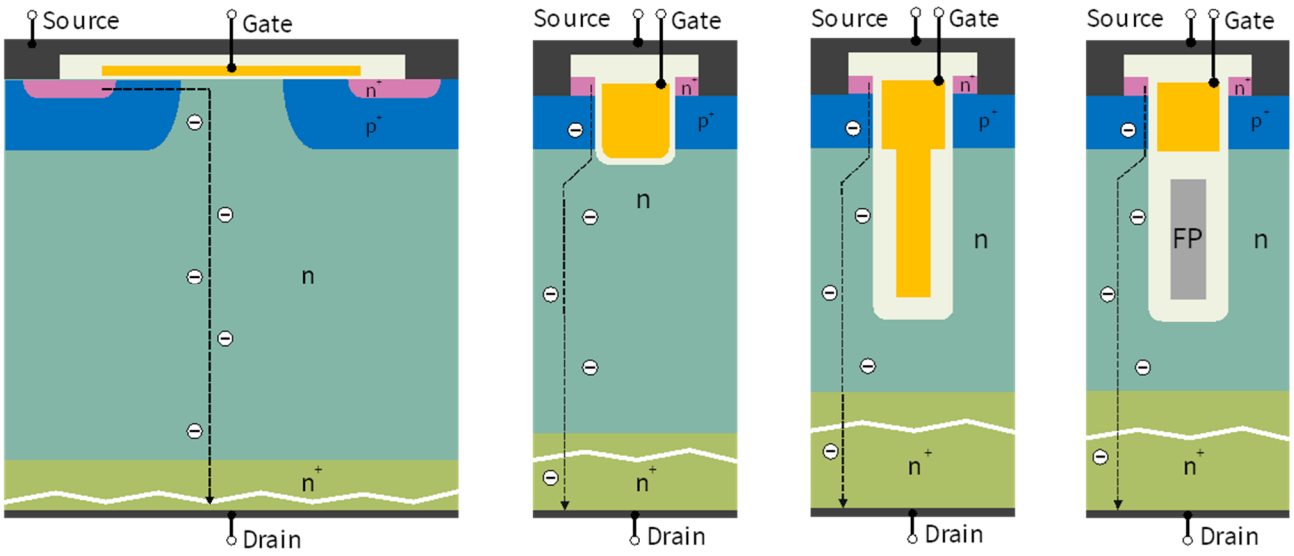

Fig. 1. Exemplary device structures depicting the evolution of power MOSFET:
a) VDMOS structure with lateral channel and planar gate
b) Trench MOSFET structure with vertical channel
c) Trench MOSFET with lateral charge-compensation by a gate-connected field plate
d) Trench MOSFET with lateral charge-compensation by an insulated field plate connected to source

channel resistance achieved no longer prevented low on-state resistances, although as a result the substrate and package resistances became more significant contributors.

However, the remarkable increase in cell density has also brought to light significant disadvantages. The gate-drain capacitance and gate-source capacitance both increase linearly with the number of trenches, i.e. with the cell density. Together with a sublinear scaling in the on-resistance $R_{DS(on)}$, this significantly impacts the technology figure-of-merit $FOM_G = R_{DS(on)} \times Q_G$.

Since the MOSFET is uniquely controlled through its gate terminal, the gate driver circuitry has to provide the total gate charge Q_G required to turn on the transistor. In the case of high switching frequency applications, as found for switched-mode power supplies (SMPS), the lowest gate charge is desirable since it proportionally reduces the driving losses. A part of the total gate charge is associated with the gate-to-drain charge Q_{GD}, which governs the drain voltage transient. Larger values of the Q_{GD} impact the transient speed, result in an increase of the switching losses, and additionally force the use of longer dead-times. Additionally, another constraint is imposed by the Miller charge ratio: Q_{GD}/Q_{TH} must be lower than one. This is needed in order to ensure an intrinsic robustness against parasitic turn-on of the MOSFET under fast drain voltage transients [4].

The introduction of charge-compensated structures, exploiting the same principle as super junction devices, marked the beginning of a new era. The introduction of devices employing an insulated deep field plate as an extension of the gate electrode enabled the lateral depletion of the drift region in the off state (Fig. 1c) [5]. The lateral depletion alters the electric field distribution throughout the structure, and it is possible to block the same voltage within a shorter length. In turn, the electric field can now be supported by a thinner and more heavily doped drift region, which leads to a substantial reduction in the on-state resistance.

Unfortunately the field plate as an extension of the gate electrode leads to a significant increase of the gate-drain capacitance C_{GD} (hence also Q_{GD} and Q_G) and a nonlinear dependence on the drain voltage. This causes a sharp drop in the transfer capacitance as soon as the mesa region completely depletes.

These disadvantages were soon overcome by the use of a separated field plate, which was isolated from the gate electrode and instead electrically connected to the source potential (Fig. 1d). While the charge compensation principle operates as before, the buried field plate does not introduce any additional contributions to the gate-drain capacitance. Instead, the field plate shields the gate electrode from the drain potential, which reduces the gate-drain capacitance C_{GD} and related charges.

These devices, at the time of their introduction to the market, showed best-in-class performance with low gate charge and gate-drain charge characteristics, high switching speeds and good avalanche ruggedness [6]. While the presence of the field plate comes with the disadvantage of an increased output capacitance C_{OSS} and output charge Q_{OSS} (a consequence of the lateral charge-compensation), a careful device optimization enabled field plate-based power technologies with $FOM_{OSS} = R_{DS(on)} \times Q_{OSS}$ comparable to those of the standard trench MOSFET [7,8].

2 Novel Cell Concept

2.1 Device Structure

New MOSFET devices are required to provide improvements across all figures of merit, as this is needed to enable high-frequency SMPS operation where losses are associated both with charges (switching) and on-state resistance (conduction). To meet these requirements, a novel cell-design was developed, which explores a true three-dimensional charge compensation.

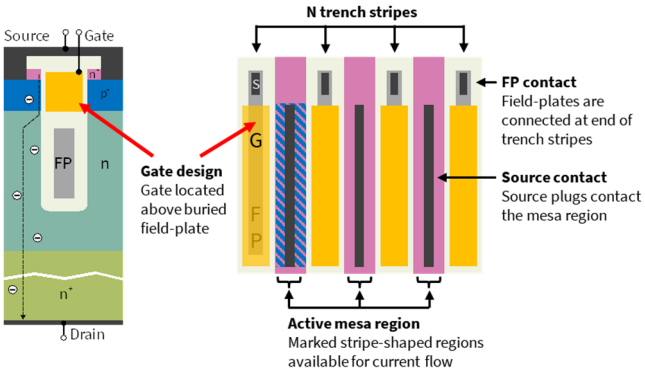

Fig. 2. Typical Trench MOSFET structure with lateral charge-compensation by an insulated field-plate connected to source (left) and top view of commonly employed stripe layout approach in the chip design (right)

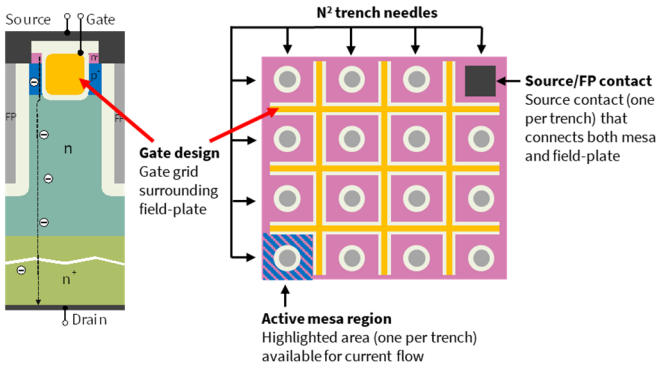

Fig. 3. Trench MOSFET structure with lateral charge-compensation by an insulated field-plate and separated gate trench (left) and top view of the new grid-like layout approach in the improved chip design (right)

State-of-the-art power MOSFET technologies commonly use an insulated deep field-plate separated from the gate electrode above combined with a stripe layout as depicted in Fig. 2 [6]. The new approach separates the field-plate trench (now forming a needle-like structure) from the gate (now forming a grid surrounding the needles), as illustrated in Fig. 3 [1]. This increases the silicon area available for current conduction, allowing a further reduction in the overall on-resistance. In order to further reduce the $FOM_G = R_{DS(on)} \times Q_G$ and $FOM_{GD} = R_{DS(on)} \times Q_{GD}$ values, the gate trench underwent a complete redesign to minimize its lateral extension.

2.2 Distributed Gate Resistance

The substantially shrunk dimensions of the gate impose a challenge, as the use of polysilicon as the gate material would result in unacceptably large internal gate resistances. This issue is usually solved by the introduction of gate fingers, however at the cost of the active area available for current conduction. To avoid this waste of area, a metal gate system has been introduced that not only reduces the internal gate resistance but also significantly improves the gate resistance uniformity over the chip.

Fig. 4 illustrates the improved homogeneity of the new approach with a comparison of the distributed gate resistance for BiC PQFN 5x6 mm² devices. In the case of the stripe design, the local gate resistance rises along the length of the stripe, with the lowest values at the gate runners and the gate pad. The use of a combination of a metal gate and a gate grid results in a much more even distribution of the gate resistance across the chip.

2.3 Distributed Field Plate Resistance

Fig. 5 compares the distribution of the field plate resistance across the chip, which is actually completely flat for the new device generation as the trench electrodes acting as field plates connect directly to the source metal. As can be seen for the previous generation device, the stripe layout again results in an increase of the local resistance with increasing distance from the source runner in the center of the chip. Thanks to the perfectly homogeneous and low-ohmic connection of the field plates for the new device setup, the chip is expected to switch extremely homogeneously, supporting fast transitions between the on- and off-state and vice versa. In addition, the direct connection between the

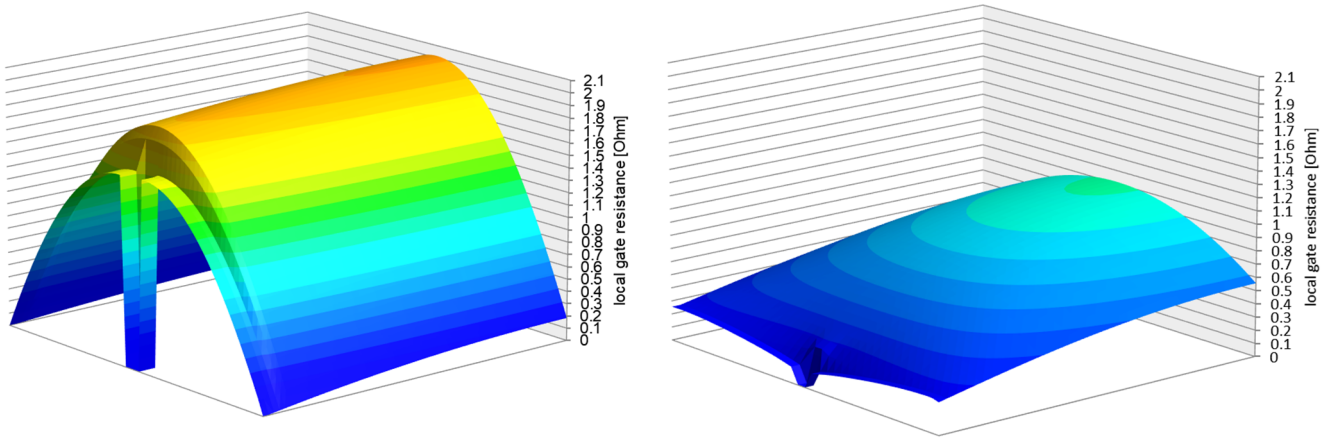

Fig. 4. Distributed gate resistance for a common stripe design (left) and the new grid-like design (right)

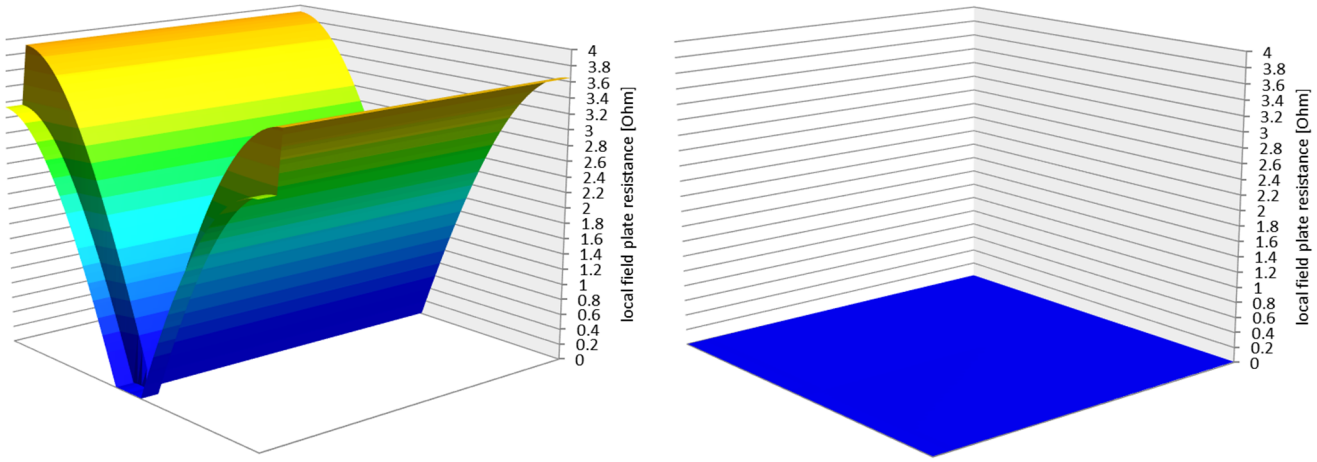

Fig. 5. Distributed field plate resistance for a common stripe design (left) and the new grid-like design (right)

source and the field-plate practically eliminates any resistance in series with the output capacitance, which minimizes ohmic losses during charging and discharging of the output capacitance.

2.4 Improved Device Parameters

Fig. 6 summarizes the achieved device parameter improvements for the 80 V and 100 V technologies, indicating impressive improvements in all of the relevant parameters. The innovative gate trench engineering of the new device technology results in a remarkable reduction of both gate-source and gate-drain specific capacitances, which is reflected in the respective figures-of-merit FOM_G and FOM_{GD}.

The FOM_G reduction helps to achieve better efficiencies, especially at light load conditions, due to the much reduced driving losses $P_{AUX} = Q_G \times V_{GS} \times f_{sw}$. This is of even higher importance for an SMPS operated at high switching frequencies, as well as in applications where a large number of MOSFETs are paralleled. In this case, the low gate charge also relaxes the requirements on the gate driver's current capability. On the other hand, the low Q_{GD} enables fast switching transients, lowering the switching losses.

Overall, the use of a gate grid and a metal gate electrode and the direct connection of the field plates to the source metal realizes a device set-up that not only ensures a very fast and homogeneous transition at turn-on and turn-off to minimize switching losses, but also reduces the risk of an unwanted, dv/dt induced parasitic turn-on of the MOSFET.

3 Application Test Results

3.1 600 W Intermediate Bus Converter for Telecom

The efficiency of operating the 100 V devices is studied in an isolated DC/DC Intermediate Bus Converter (IBC),

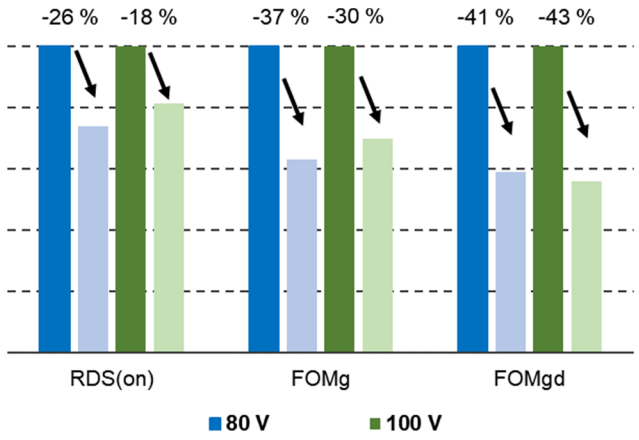

Fig. 6. Improvement of device parameters for best-in-class devices in the PQFN 5x6 package

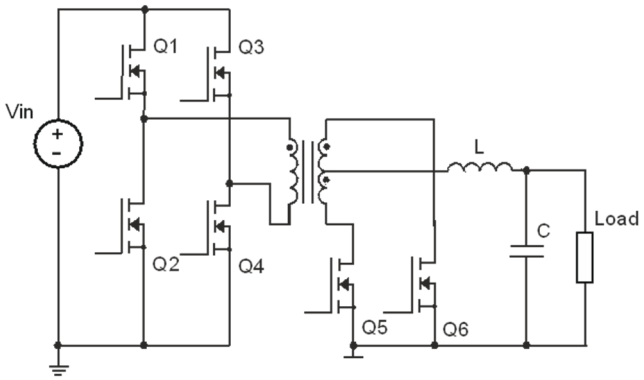

Fig. 7. Basic schematic of the 600 W DC/DC IBC

as typically used in telecom and datacom power systems [9,10]. The unit operates with a switching frequency of 250 kHz, a nominal 48 V input and a 12 V regulated bus output voltage. The operating input voltage is allowed to vary between 36 V and 75 V; the turns ratio of the transformer is 3:1. The board delivers 600 W in a standard quarter-brick form-factor. For the measurement of the efficiency, the test board employs a full-bridge topology on the primary side and a center-tapped synchronous rectifier topology on the secondary side. Fig. 7 illustrates the basic schematic of this converter. Fig. 8 shows the top and bottom view of the realized converter, with the primary side devices marked in yellow and the secondary side devices marked in blue.

The study first investigates the primary side efficiency for 100 V devices of the previous technology generation OptiMOS™ 5 BSC050N10NS5 with that of the new technology generation OptiMOS™ 6 ISC060N10NM6, all in PQFN 5x6 mm² packages. The on-resistance of the selected devices was matched as closely as possible, with 6 mΩ devices of the new and 5 mΩ devices of the predecessor technology.

Fig. 9 compares the achieved efficiencies on the primary side, which improves by a remarkable 0.7 % at

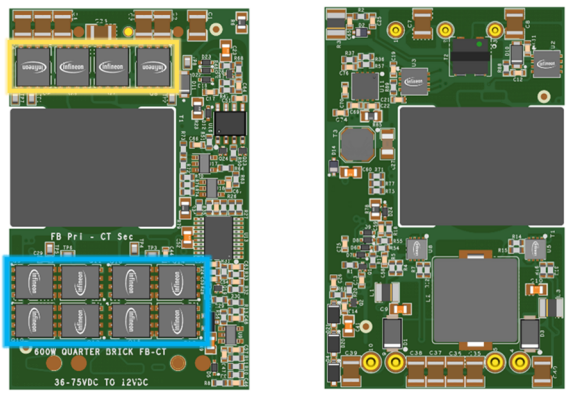

Fig. 8. Top and bottom view of the 600 W IBC board with the primary side MOSFETs marked in yellow and the secondary side MOSFETs marked in blue

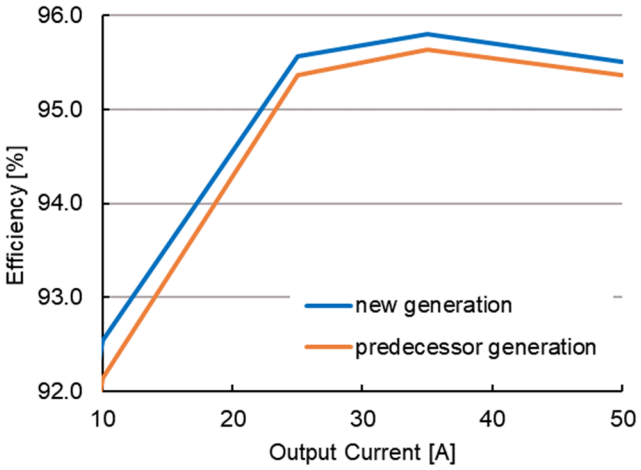

Fig. 9. Comparison of measured efficiency on the primary side of the 600 W IBC

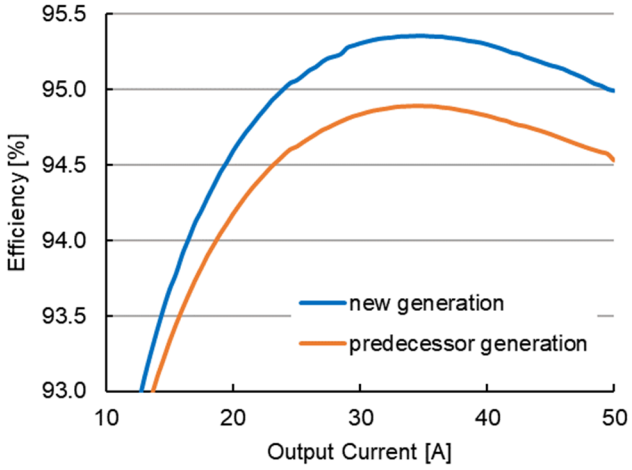

Fig. 10. Comparison of measured efficiency on the secondary side of the 600 W IBC

light load and still 0.14 % at full load. The reduction in the charges of the new devices enables the improvements in efficiency even with the higher on-resistance. In the low load range, the reduction of the drain-to-source charge has more impact on the efficiency, whereas from half to full load the reduction of the gate-to-drain capacitance has a higher impact.

To investigate the secondary side efficiency, 100 V devices of the previous technology generation OptiMOS™ 5 BSC027N10NS5 compare with devices of the new technology generation OptiMOS™ 6 ISC027N10NM6, all in PQFN 5x6 mm² packages. The on-resistance of the selected devices is 2.7 mΩ for both generations, with two devices in parallel per leg. The efficiencies measured on the secondary side are depicted in Fig. 10 and yield an improvement of 0.46 % over the entire range from half to full load. This improvement is mainly attributed to the lower reverse-recovery charge of the new OptiMOS™ 6 devices, and to the lower gate charge with impact on the light-load range.

3.2 1 kW LLC Intermediate Bus Converter for Datacenters

The performance of the 80 V device is investigated in another IBC: this time the topology employs a closed-loop LLC design [11-13]. In this converter, the resonant frequency of the LLC converter is 300 kHz, and varies from 220 kHz to 800 kHz to regulate the output voltage. The turns ratio of the transformer is 4:1 and the board can deliver an output power of up to 1 kW. Both primary and secondary side employ a full-bridge configuration. The basic schematic is shown in Fig. 11. The LLC board can achieve ZVS turn-on across the full input voltage and load range (except at high input voltage at light load).

As devices under test, two 80 V MOSFETs in a PQFN 5x6 mm² are paralleled in each leg of the primary-side full-bridge. The secondary-side uses four source-down 25 V MOSFETs in a PG-TSON-8-4 3.3x3.3 mm² per leg in parallel. Views of the realized test board, which spans over a standard quarter-brick form factor, are given in Fig. 12.

The investigation compares 80 V devices of the predecessor technology device generation OptiMOS™ 5 BSC026N08NS5 with the new technology generation OptiMOS™ 6 ISC031N08NM6. Also here, the on-resistance of the selected devices was matched as closely as possible, with 3.1 mΩ devices of the new and 2.6 mΩ devices of the predecessor technology.

Fig. 13 depicts the comparison of the gained efficiencies for two input voltages. As the previous generation devices available for this comparison had a ~16 % lower on-resistance, the high-load efficiency is comparable with the new devices. At low-load, the efficiency improves by up to 0.7 %, whereas at half-load the efficiency gain is 0.13 %.

The LLC topology targets to achieve soft-switching (either at zero-voltage or at zero-current) for all MOSFETs, meaning that the switching losses are assumed to be negligible. The relevant losses that need

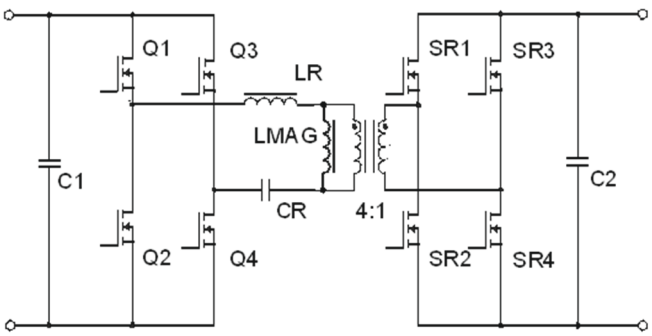

Fig. 11. Basic schematic of the 1 kW full-bridge LLC IBC

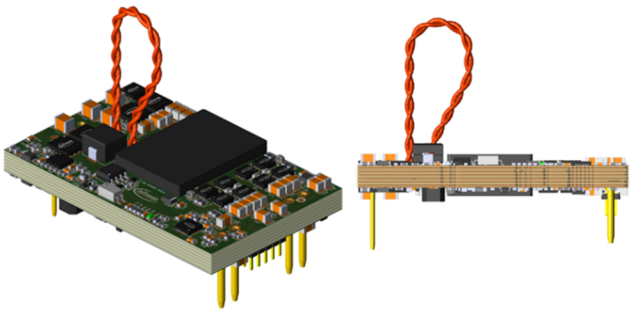

Fig. 12. Views of the realized full-bridge LLC converter board.

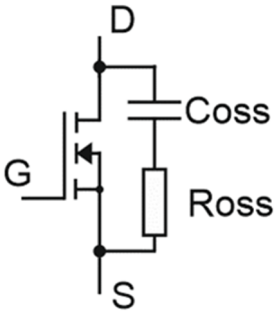

Fig. 14. MOSFET with internal field-plate capacitance C_{OSS} and field-plate resistance R_{OSS}

to be considered are the conduction and the gate-drive losses. The impressive efficiency improvement found with the new device generation therefore largely results from the dramatically lowered gate and gate-drain charge, together with the strongly improved switching homogeneity across the chip area.

However, in addition to these there is another loss mechanism contributed by the power device itself. This mechanism is often neglected and relates to the so-called R_{OSS}, the field-plate resistance that is in series with the field-plate capacitance C_{OSS}. Fig. 14 shows a simplified representation of the MOSFET. Every time C_{OSS} is either charged or discharged, a large portion of the magnetizing current must pass through R_{OSS}, causing conduction losses, which may become significant depending on the device setup. It is evident that the R_{OSS} can become significant for a MOSFET with a common stripe layout as shown in Fig. 2, as the field-plates can only be connected with the source at the end of the trench stripes. This is completely different for the new MOSFET technology which has a much lower R_{OSS} value, as each field-plate is directly connected to the source metal as can be seen in Fig. 3.

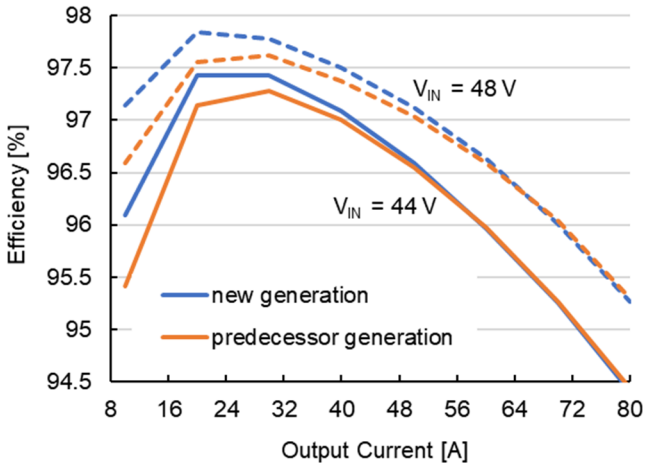

Fig. 13. Comparison of the gained efficiency for the use of 80 V devices in the investigated closed-loop LLC IBC (f_{RES} = 300 kHz)

4 Conclusion

This work introduces the 80 V and 100 V voltage class of our latest power MOSFET technology family. The new technology generation delivers improvements in all important device parameters and combines the benefits of low on-state resistance with a superior switching performance. The new technology is specifically optimized for high switching frequency applications such as telecom SMPS and solar.

The remarkable jump in the overall device performance is enabled by substantial improvements at the device technology level. This has culminated in a unique device structure, which is the first to employ a three-dimensional charge compensation combined with the first ever use of a metal gate in a trench power MOSFET.

The reduction achieved in the on-resistance, the dramatically-lowered gate charge and gate-drain charge, together with a low output charge and improved switching homogeneity across the device area, enhance the system efficiency in the tested applications across all load conditions. The new device structure is also beneficial for the internal body diode of the MOSFET. Because the silicon area conducting current is increased, the body diode current density is decreased, which for the same current level means a decreased reverse recovery charge. Efficiency measurements in several SMPS applications under hard and soft switching conditions confirm the findings at the semiconductor device level.

Resonant applications like the LLC converter especially benefit from the improved device characteristics. Here the losses due to the stored charge in the output capacitance of the power semiconductors are largely avoided, as this charge swings from one MOSFET to the other. However, this swing current is linked to conduction losses due to the PCB tracks, the transformer windings and the internal series resistance R_{OSS} connected to the output capacitance C_{OSS} of the device structure, but this series resistance R_{OSS} is effectively eliminated with the new technology.

The significantly improved device performance also enables a reduction of up to half in the number of devices required, or alternatively the use of smaller footprints, without having a negative impact on the temperature of the devices. This not only provides an advantage in terms of bill-of-materials (BOM) costs, but also the chance to save real space on the PCB. This opens the door for a further optimization at the system design level, which is expected to further boost efficiency, reduce the converter size and increase the power density.

5 Acknowledgements

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