POWER ELECTRONICS NEWS

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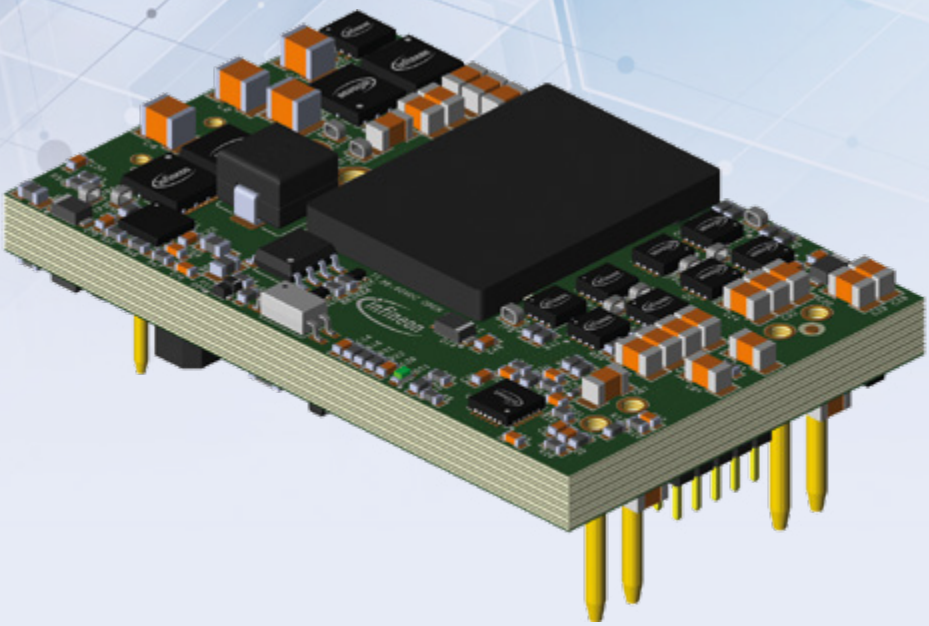
Rethinking Power MOSFET Design for Greater Efficiency and Performance

Infineon

COVER STORY – DESIGN



Accelerating the Drive for Higher Efficiencies Through Power MOSFET Technology Innovation

Introducing Infineon's latest OptiMOS™ 6 device technology—a novel cell-design approach for higher power densities and cost-effectiveness

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MOSFET technology has been widely recognized as an excellent option for switches in power management circuits since its inception. Commercially available since the late 1970s, vertical diffused MOSFET (VDMOS) structures were the first to fulfill the need for a power switch.[1] Due to its superior switching performance and high input impedance, the MOSFET quickly emerged as an attractive alternative to bipolar technologies. However, its application in the power electronics industry was limited by the high on-state resistance

that restricted the current-handling capabilities of the VDMOS. In medium-voltage VDMOS, the intrinsic channel resistance and the JFET region—which restrict the channel current flow into the epitaxially-grown drift region—were the primary contributors to the total on-state resistance ($R_{DS(on)}$) between the drain and source (Figure 1a).

It took more than a decade of device design and process engineering progress to overcome this limitation, which finally led to the commercialization of the first trench-gate MOSFETs in the late 1980s. By moving the channel in the vertical direction, this device concept enabled a reduction in cell pitch without negatively affecting current spreading. The virtual elimination of the JFET region dramatically decreased the on-state resistance (Figure 1b). Nevertheless, the significant increase in cell density not only established the trench MOSFET as a competitive alternative to planar technology but also brought substantial drawbacks to light.

The gate-drain capacitance (related to trench-gate penetration in the epi drift region) and gate-source capacitance (overall capacitance between trench gate and body/source diffusion) increase linearly with the number of trenches, i.e., with the cell density. Together with a sublinear scaling in the on-resistance, this significantly impacts the technology figure of merit (FOM) $FOM_g = R_{DS(on)} \times Q_g$. Because the MOSFET is uniquely controlled through its gate terminal, the gate-driver circuitry has to provide the total gate charge (Q_g) required to turn on the transistor. In the case of high-switching–frequency applications, the lowest gate charge is desirable, as it proportionally reduces the driving losses. A part of the total gate charge is associated with the gate-to-drain charge (Q_{gd}), which governs the drain-voltage transient. A higher Q_{gd} impacts the transient speed, increases the switching losses and forces the use of longer deadtimes. It became evident that specific measures were needed to reduce the overall gate and gate-drain charge.

A new era started with the introduction of charge-compensated structures, exploiting the same principle as superjunction devices. Introducing devices that use an insulated deep field plate as an extension of the gate electrode enabled the lateral depletion of the drift region in the off state (Figure 1c).[2] The lateral depletion alters the electric field distribution throughout the structure, allowing the same voltage to be blocked within a shorter length. Because the electric field can now be supported by a thinner and more heavily doped drift region, a substantial reduction in the on-state resistance can be achieved. It is worth noticing that the field plate (as an extension of the gate electrode) leads to both a significant increase of the reverse-transfer capacitance C_{gd} (hence also Q_{gd} and Q_g) and a nonlinear dependence on the drain voltage.

In fact, the transfer capacitance drops abruptly as soon as the mesa region completely depletes. These disadvantages were soon overcome by using a field

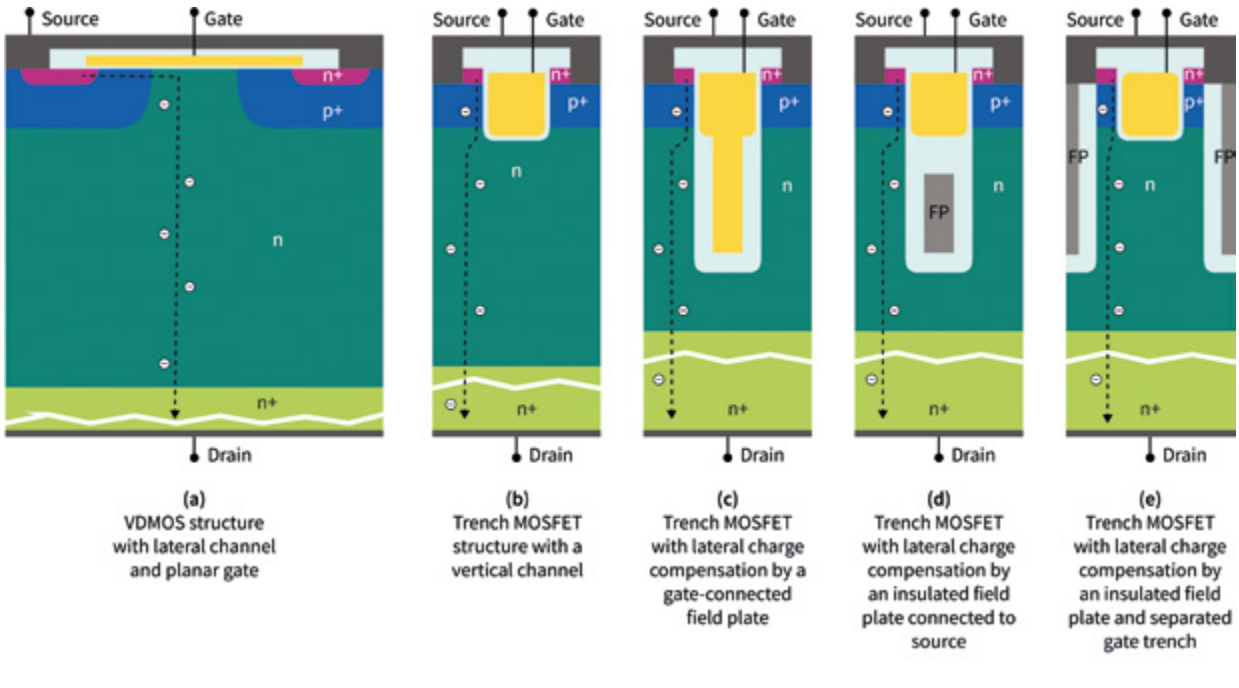

Figure 1: Exemplary device structures depicting the evolution of a power MOSFET

plate, which was isolated from the gate electrode and instead electrically connected to the source potential (Figure 1d). While the charge compensation principle operates as before, the buried field plate does not introduce any additional contributions to the gate-drain capacitance. Instead, the field plate shields the gate electrode from the drain potential, which reduces the gate-drain capacitance C_{gd} and related charges. These devices, at the time of their introduction to the market, showed best-in-class performance with low gate charge and gate-drain charge characteristics, high switching speeds and good avalanche ruggedness.[3]

INFINEON'S INNOVATIVE APPROACH TO RAISING POWER MOSFET DESIGN TO THE NEXT LEVEL

To reach the next level in power MOSFET evolution, new MOSFET devices are required to provide improvements across all FOMs. This is needed to enable high-frequency switched-mode power supply (SMPS) operation, whereby losses are associated with charges (switching) and on-state resistance (conduction). To meet these more demanding requirements, a novel cell-design approach has been developed and implemented, which explores for the first time a true 3D charge compensation.

First, a direct connection of the field-plate electrodes to the top-side source metal is required, as illustrated in Figure 1e. Second, the device layout must move away from the common stripe layout to a grid-like layout structure, as depicted in Figure 2. This increases the silicon area for current conduction compared with a structure with stripes, allowing a further reduction of the overall on-resistance in the new ***OptiMOS™ 6 low- and medium-voltage power MOSFETs***. In order to also further reduce the $FOM_g = R_{DS(on)} \times Q_g$ and $FOM_{gd} = R_{DS(on)} \times Q_{gd}$ values, the gate trench underwent a complete redesign to minimize its lateral extension. However, the substantially smaller dimensions of the gate impose a new challenge, as the use of polysilicon as gate material would result in unacceptably large internal gate resistances. The introduction of gate fingers usually solves this issue, but these reduce the active area available for current conduction.

Instead, a new metal gate system has been introduced to avoid any loss of active area, which otherwise would be rather significant. This system not only reduces the internal gate resistance but also enhances the gate resistance uniformity across the chip.[4] Furthermore, the field plates are directly connected to the source metal, ensuring a rapid and homogeneous transition at turn-on and turn-off. This minimizes switching losses and mitigates the risk of an undesired dv/dt-induced parasitic turn-on of the MOSFET.

BOOSTING END-TO-END CONVERSION EFFICIENCY IN TELECOM AND DATA CENTER SYSTEMS

Intermediate bus converters (IBCs) are considered a demanding application for power MOSFETs. As part of the intermediate bus architecture (IBA), the IBC is a ***DC/DC converter*** that performs an intermediate conversion to supply the downstream ***point-of-load (PoL) step-down converters***, as shown in Figure 3.

This architecture is prevalent in ***telecom*** and ***data centers*** and aims to achieve the best conversion efficiency from the AC/DC power supply unit to the

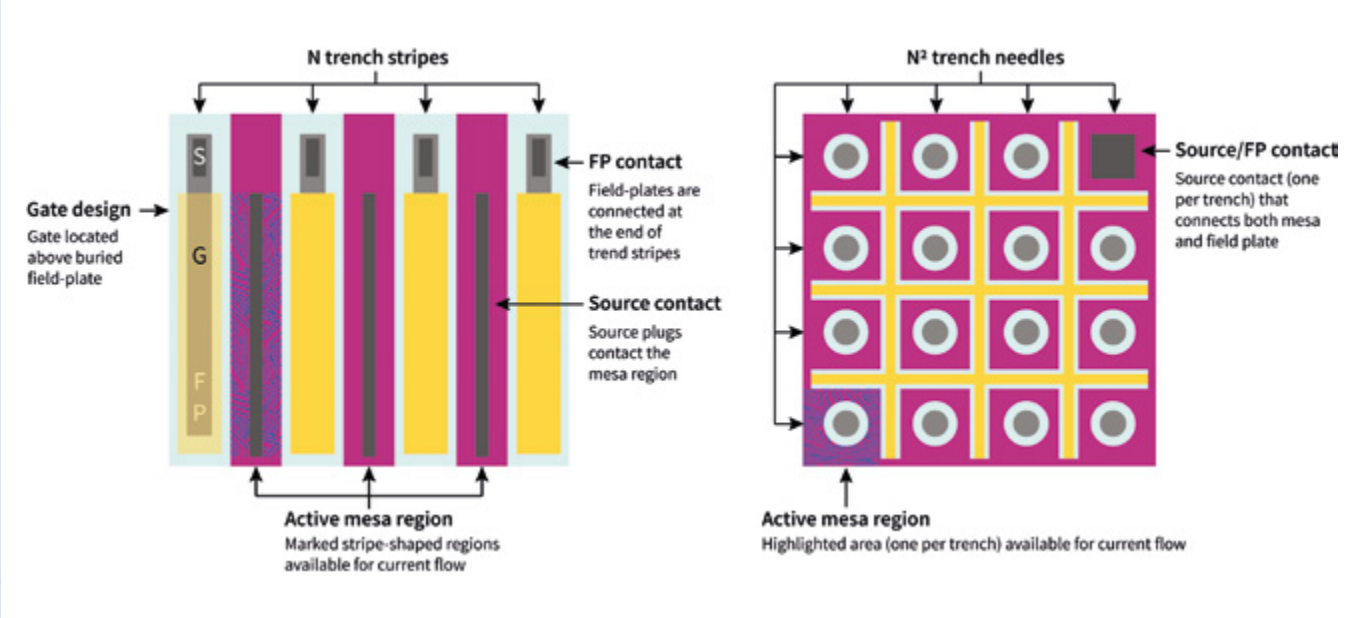

Figure 2: Comparison of the commonly used stripe layout with the new grid-like layout approach

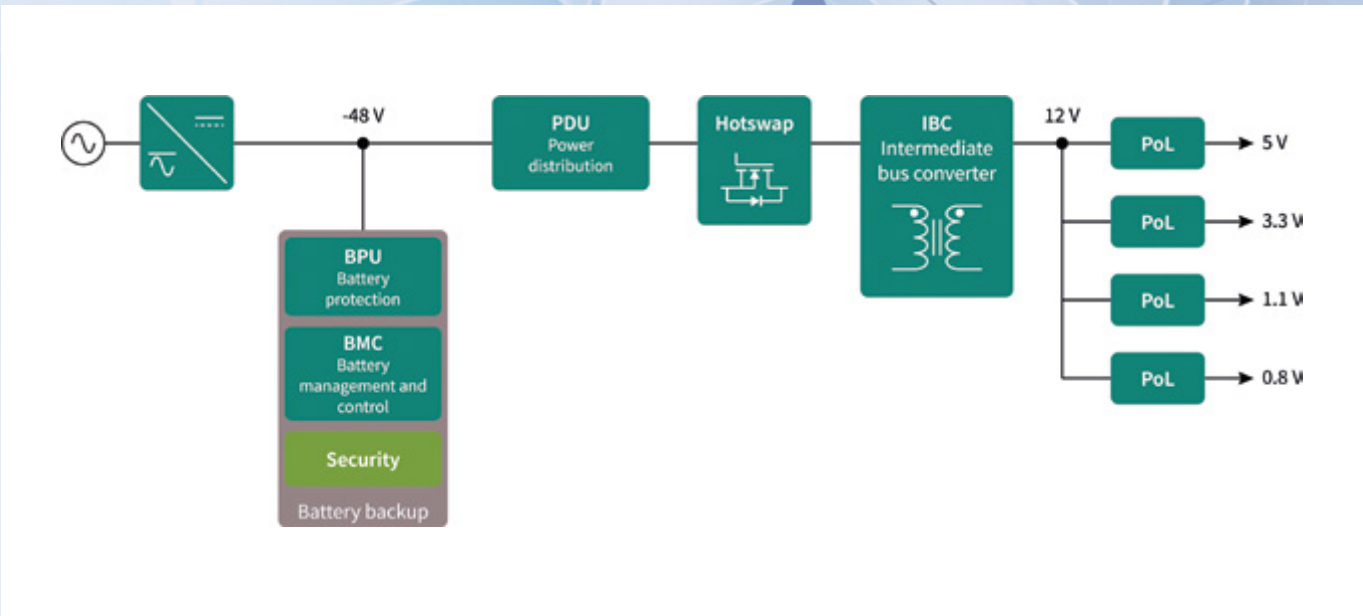

Figure 3: System diagram of the IBA

digital loads (xPUs and ASICs).[5] Depending on the end application, PoL converters can be optimized to operate either with a narrow or wide input voltage range.
In telecom systems, where the –48-V bus shows wide tolerance, it has been common for the PoL regulators to operate with a narrow input voltage range (e.g., 12 V), thus requiring a regulated IBC. Taking the burden of the regulation from a wide input range (–36 V to –75 V), the IBC tends to be rather inefficient and plays an important role in defining the end-to-end conversion efficiency. Improving the IBC efficiency is thus paramount to boosting the overall conversion efficiency.

In ***modern data center systems*** or ***advanced AI hardware accelerators***, extremely high currents have to be supplied to sub-1-V digital loads. The efficiency of the two stages can be maximized by playing with the down-conversion ratio of the IBC and with the burden of regulation being transferred to the multiphase PoL/voltage regulator module. Indeed, unregulated IBCs in the form of DC transformers (DCX) are employed in these applications, showing typical peak efficiencies that exceed 98%, much higher than their regulated counterparts.

DEVICE BEHAVIOR AND EFFICIENCY MEASUREMENTS UNDER HARD-SWITCHING CONDITIONS: TESTING A 600-W IBC FOR TELECOM APPLICATIONS

The IBC in this application operates as an isolated DC/DC IBC with a nominal –48-V input (overall range from –36 V to –75 V) and a 12-V output voltage bus. The fully regulated converter in the industry's standard quarter-brick form factor operates at a switching frequency of 250 kHz and can deliver an output current of a maximum of 50 A. The IBC is based on a hard-switching full-bridge (FB) topology with a center-tapped (CT) synchronous rectifier (SR) on the secondary side, schematically shown in Figure 4.

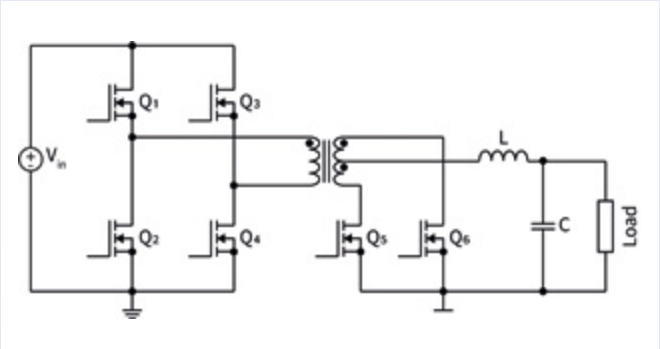

Figure 4: Simplified schematic of the 600-W IBC board in FB-CT configuration

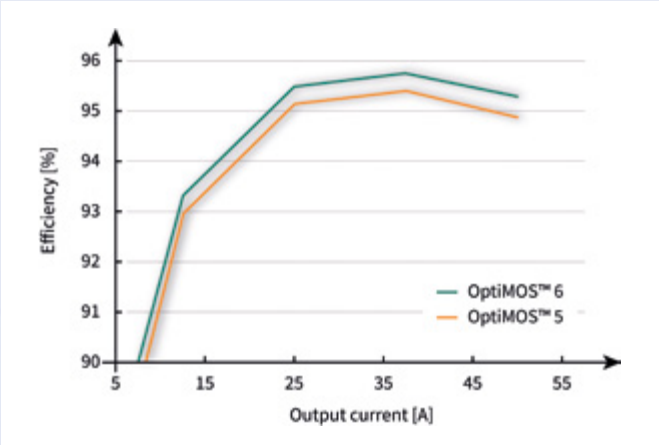

Figure 5: Efficiency in the 600-W IBC comparing the new and predecessor technology

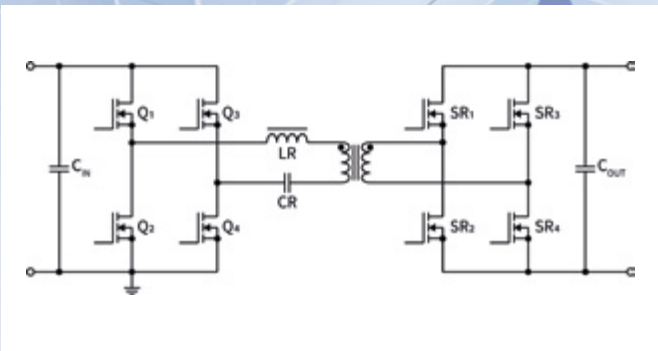

Figure 6: Schematic of the 1-kW IBC board with an FB LLC on the primary side

The primary side uses Infineon's latest trench MOSFET technology, OptiMOS™ 6, employing 100-V devices (***ISC030N10NM6***) with $R_{DS(on),max}$ = 3.0 mΩ. These devices come in a SuperSO8 package (PQFN 5 × 6 mm²) and replace the ***BSC050N10NS5*** from the predecessor OptiMOS™ 5 technology, which had a higher $R_{DS(on),max}$ of 5.0 mΩ (also coming in a SuperSO8 package). On the secondary side, the system uses 80-V MOSFETs as SRs. It utilizes either four paralleled ***OptiMOS™ 5 BSC040N08NS5*** devices with $R_{DS(on),max}$ = 4 mΩ and a SuperSO8 package from the predecessor technology, or four paralleled OptiMOS™ 6 ISZ053N08NM6 devices[i] with the industry's lowest $R_{DS(on),max}$ of 5.3 mΩ and a smaller PQFN 3.3 × 3.3-mm² package.

The results obtained from the comparison of measured efficiencies, presented in Figure 5, highlight the advantages of adopting OptiMOS™ 6 technology. Compared with the previous generation, the solution employing OptiMOS™ 6 technology demonstrates impressive efficiency improvements in excess of 0.4% from 20% load up to full load. Using a smaller package footprint reduces the PCB area allocated for SR devices by up to 64%. Additionally, the maximum temperature at the hotspot of the converter on the primary side decreases by 7.5°C.

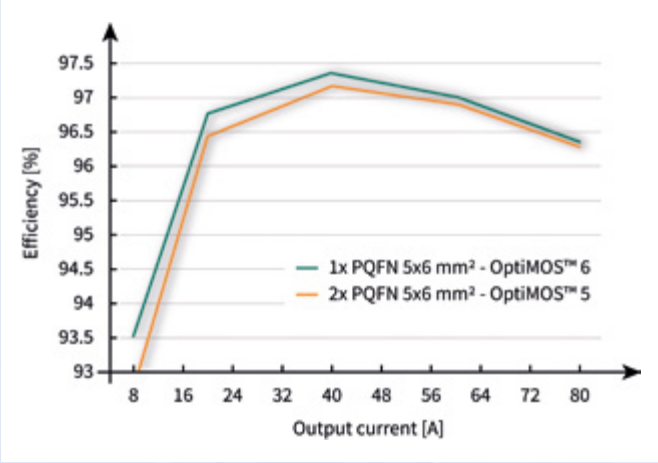

Figure 7: Efficiency in the 1-kW LLC IBC comparing the new and predecessor technology

EFFICIENCY MEASUREMENTS UNDER SOFT-SWITCHING CONDITIONS: TESTING A 1-KW IBC FOR DATA CENTERS

This 1-kW, 4:1, fixed-frequency LLC IBC operates as a DCX from an input that may vary from 42 V to 60 V. The soft-switching techniques employed in the LLC resonant topology allow a significant efficiency improvement in ***telecom*** and ***server power supplies***.[6–8]

In Figure 6, two OptiMOS™ 6 80-V power MOSFETs housed in a SuperSO8 package are paralleled on the primary-side FB. An FB configuration is formed using four ***OptiMOS™ 5 25-V IQE006NE2LM5*** source-down devices (PQFN 3.3 × 3.3 mm²) in parallel as SRs. The turns ratio of the transformer is 4:1. The resonant frequency of the LLC converter is 310 kHz. The switching frequency is fixed to match the resonance frequency of the tank. Zero-voltage switching for the primary switches and zero-voltage/zero-current switching for the SR switches are thus achieved by design.

The significantly improved device parameters of the new OptiMOS™ 6 80 V not only improve the overall efficiency of the converter but also allow the two paralleled ***SuperSO8 OptiMOS™ 5 80-V power MOSFETs BSC030N08NS5*** with $R_{DS(on),max}$ = 3 mΩ on the primary side to be replaced by just one OptiMOS™ 6 ISC014N08NM6 device,[i] with the industry's lowest $R_{DS(on)}$ of 1.45 mΩ. Figure 7 compares the efficiency for this case, revealing an improvement over the full load range, with up to 0.8% better values using the latest device technology. Additionally, the single device of the new generation remains even cooler than if two devices from the previous generation are used.

CONCLUSION

This article discusses Infineon's latest OptiMOS™ 6 trench MOSFET technology, featuring the new 80-V and 100-V power MOSFET devices.
The new OptiMOS™ 6 devices surpass their predecessors in all critical parameters, offering a combination of low on-state resistance and superior switching performance. With a focus on high-switching–frequency applications like ***telecom SMPS*** and ***solar energy systems***, this technology holds immense potential for bringing significant improvements to various other application fields.

i This product will launch soon. For engineering samples, click here to place a request.

The advances in overall device performance are remarkable, resulting from significant improvements at a device technology level. These improvements led to the creation of a unique device structure, the first to employ a 3D charge compensation in conjunction with a metal gate in a trench power MOSFET. As a result, this technology reduces on-resistance, dramatically lowers gate- and gate-drain charges and improves the switching homogeneity across the device area. These achievements translate into a significant enhancement in system efficiency in various applications across different load conditions.

The efficiency measurements carried out on several SMPS applications under both hard- and soft-switching conditions confirm the remarkable findings at the semiconductor device level. Depending on the topology and load condition, it is possible to raise efficiency by up to 1%, further highlighting the superiority of this new technology. Additionally, the much-improved device performance reduces the number of devices required by up to 50% without any adverse effect on the device temperature, demonstrating its potential to significantly lower costs and improve overall system reliability.

To learn more about the latest power MOSFET technology family and its potential to revolutionize the telecom power arena and other application fields, we encourage you to visit our ***webpage***.

References

- [1]Williams et al. (2017). ***"The Trench Power MOSFET: Part I - History, Technology, and Prospects."*** IEEE Transactions on Electron Devices, Vol. 64, No. 3, pp. 674–691.
- [2]Ejury, J., Hirler, F., & Larik, J. (2001). "New P-Channel MOSFET Achieves Conventional N-Channel MOSFET Performance." PCIM.
- [3]Schlögl et al. (2005). "A new robust power MOSFET family in the voltage range 80 V – 150 V with superior low RDSon, excellent switching properties and improved body diode." EPE.
- [4]Siemieniec et al. (2022). "A new power MOSFET technology achieves a further milestone in efficiency." EPE.
- [5]Li, S. (2020). "Intermediate Bus Converters for High-Efficiency Power Conversion: A Review." IEEE Texas Power and Energy Conference (TPEC).
- [6]Liu, R., & Lee, C.Q. (1988). "Analysis and design of LLC-type series resonant converter." IEE Electron Device Letters, Vol. 24, No. 24, pp. 1517–1519.
- [7]Yang et al. (2002). "LLC resonant converter for front end DC/DC conversion." APEC.
- [8]Jung, J., & Kwon, J. (2007). "Theoretical Analysis and Optimal Design of LLC Resonant Converter." EPE.

Wide-Bandgap Semiconductors for EVs (Podcast)

Electric and hybrid vehicles are seeking efficient and cost-effective power-conversion technologies. Wide-bandgap semiconductors provide higher performance compared with silicon. In this podcast with Filippo Di Giovanni, strategic marketing for the power transistor subgroup at STMicroelectronics, we will discuss the main challenges and the benefits that GaN/SiC can offer to the automotive industry.

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