

# Power MOSFET Design for Synchronous Rectification

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## Abstract

*Synchronous rectifying stages of power supplies are a typical application field for low-voltage power MOSFETs. To allow a high efficiency under all load conditions, the power MOSFET not only needs to meet general requirements like low on-resistance, low gate charge and good avalanche capability, but must also have a low output capacitance and low reverse-recovery charge. The paper discusses the requirements for device optimization and how those often conflicting requirements can be met.*

**Keywords:** MOSFET, synchronous rectification, SMPS, Simulation, Measurement

## INTRODUCTION

Several years ago the upcoming 80PLUS<sup>®</sup> requirements for SMPS (switched-mode power supply) forced the designers of power supplies to rethink the concept of secondary side rectification. At that time, conventional diodes with a forward voltage drop of roughly 0.5 V were used. In combination with large output currents these diodes generate high conduction losses, leading to a poor efficiency level at high output power. The change to SR (synchronous rectification) by using standard MOSFETs with low  $R_{DS(ON)}$  was the solution to increase the efficiency level above 80 %. Further design steps like improved PCB layout, enhanced snubber networks for better spiking behavior of the MOSFET, in addition to lower  $R_{DS(ON)}$ , increased the efficiency level to a peak of around 90 %.

However, the current 80PLUS platinum certification requires much more. The efficiency for single output PSUs (power supply units) with an AC input voltage of 230 V (e.g. server PSU) has to be above 90 %, 94 % and 91 % at respectively 20 %, 50 % and 100 % of the output power. An optimization at full load could be enabled by using the lowest available  $R_{DS(ON)}$  for the SR MOSFET, but this approach does not allow the highest performance to be reached at low output power. To reach or exceed the 80PLUS platinum certification requirements in the coming years, it is essential to have SR MOSFETs offering a well balanced ratio between switching losses and conduction losses. At the same time the absolute loss values need to be extremely low. The device must also be rugged to withstand critical operation conditions often manifesting as avalanche events. Due to unavoidable parasitic elements in the circuitry, it is also likely that the devices may enter avalanche mode for very short times at low avalanche energies repetitively even under regular operating conditions. As a consequence, the device is expected to be robust against such short repetitive avalanche events.

## APPLICATION REQUIREMENTS

### General synchronous rectification requirements

The power losses in the SR MOSFET must be separated into load dependent conduction losses and constant switching losses. Conduction losses are determined by the  $R_{DS(ON)}$  of the switch. They increase with increasing output load of the power supply. On the other hand the switching losses are constant over the whole output load, and are mainly determined by the gate charge  $Q_G$  and the output charge  $Q_{OSS}$ .

Further considering the turn-off process, also the stored charge  $Q_{RR}$  of the body diode must be removed and the output capacitance  $C_{OSS}$  has to be charged up to the input voltage of the SR stage as explained in Fig. 1. This process results in a reverse current peak  $I_{RRM}$  which is linked to the overall inductance of the commutation loop. The energy stored in this inductance is transferred to the output capacitance as soon as the

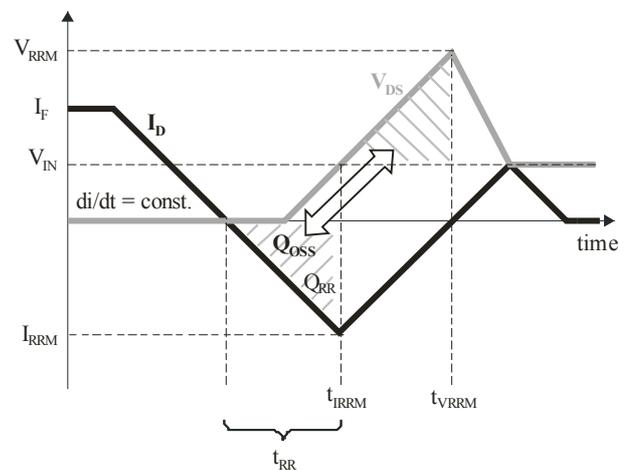


Fig. 1: Simplified model of the turn-off process of a Synchronous Rectification MOSFET

drain-source-voltage  $V_{DS}$  of the MOSFET exceeds the input voltage  $V_{IN}$  with a voltage spike carrying this energy. The amount of energy is defined by the reverse-recovery charge stored in the body diode  $Q_{RR}$  and the charge stored in the output capacitance  $Q_{OSS}$  and is lost in every switching cycle.

A high  $Q_{OSS} + Q_{RR}$  does not only generate power losses but also causes a large reverse current peak  $I_{RRM}$  as shown schematically in Fig. 1. The higher the reverse current peak, the higher the rate of voltage rise  $dv/dt$ , and thus the greater the turn-off voltage spike, will be. This high  $dv/dt$  can also trigger a dynamic re-turn-on of the MOSFET by raising the gate voltage above the threshold voltage due to the capacitive voltage divider  $C_{GD}/C_{GS}$ . To prevent this, a small output capacitance  $C_{OSS}$ , a small stored charge  $Q_{RR}$ , a non-critical ratio  $C_{GD}/C_{GS}$  and a narrow tolerance of all MOSFET capacitances are essential.

As the proposed device technology is intended for use in fast switching applications, the absolute value of the gate-drain-charge  $Q_{GD}$  and its variation over the manufacturing process are important. The gate-drain charge  $Q_{GD}$  and the overall gate resistance  $R_G$  are the main factors controlling the switching speed of the device. A small gate-drain-charge  $Q_{GD}$  is therefore advantageous and the overall variation of this parameter should be small to ease paralleling of the devices.

It is further known that avalanche events due to unclamped inductive switching can affect the device in a SR stage. In case of single pulse events found under critical operation conditions (as abrupt load changes, abrupt disconnection from the power grid), the energies which need to be dissipated by the device can be large. Also, the peak current densities may exceed the nominal current rating. Here a good suppression of the latch-up of the parasitic BJT is required and given for most modern MOSFETs. However, the avalanche capability is limited by the intrinsic temperature of the device where the intrinsic carrier density equals the background doping, leading to thermal destruction of the device. As active device areas become smaller due to a lower specific on-resistance not only the overall device volume for energy dissipation gets smaller but also the current densities increase. Repetitive avalanche events are often caused by small parasitic inductances. The number of repeated avalanche cycles, even when dissipating low energies in the range of  $1\mu J$ , may affect the device in case of poor device designs.

### How to target highest efficiency

To optimize SR MOSFET for highest efficiencies, a well balanced ratio between switching losses and conduction losses must be found. At low output loads the conduction losses only play a minor role while switching losses are dominant. For higher loads the weighting of the losses is the other way around. To calculate the losses and to get an indication how the technology will perform in the system, different figures-of-merit (FOM) need to be considered [1]. The  $FOM_G$  is the product of the  $R_{DS(ON)}$  and the  $Q_G$ , while the  $FOM_{OSS}$

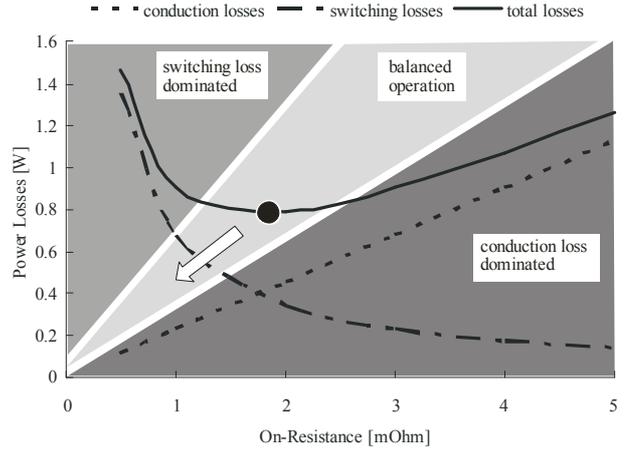


Fig. 2: Power losses per device vs. on-resistance in synchronous rectification for a given MOSFET technology ( $V_{IN} = 30 V$ ,  $V_{GS} = 10 V$ ,  $I = 15 A$ ,  $f = 125 kHz$ )

is the product of  $R_{DS(ON)}$  and  $Q_{OSS}$ . As the capacitances of a MOSFET are inversely proportional to the  $R_{DS(ON)}$ , this product is fixed over the whole  $R_{DS(ON)}$  range of a given technology. As illustrated in Fig. 2, the conduction losses increase linearly with higher  $R_{DS(ON)}$ . Since switching losses increase at low  $R_{DS(ON)}$  values, a local minimum is found considering the total power losses. Here the MOSFET generates the lowest losses in a given system and therefore the highest efficiency is found. Further optimization of an SR system cannot be done within this given MOSFET technology. Consequently, the main goal of a new SR MOSFET is moving this point of minimum losses to the bottom left corner in Fig. 2. This can only be achieved by a further massive reduction of switching losses and conduction losses at the same time. This will raise the whole system efficiency both at low output power and at high output power. An improvement of the  $FOM_{OSS}$  will mainly affect the system efficiency at low output power while the  $R_{DS(ON)}$  will primarily affect the efficiency at high currents. Also the stored charge  $Q_{RR}$  negatively affects the system efficiency at medium and high output power and adequate measures might be required to reduce it.

## DEVICE OPTIMIZATION

### Brief introduction of the device concept

Based on these findings, the influence of the manufacturing technology capabilities of a field-plate trench MOSFET will be discussed. The field-plate trench MOSFET is shown schematically in Fig. 3 and recently discussed in multiple publications [2-5]. The application of a field-plate principle leads to an almost constant field distribution in the vertical direction since the carriers in the drift region are laterally compensated by mobile carriers at the field-plate, thereby reducing the necessary drift region length and increasing the allowed drift region doping for a given breakdown voltage. Both contribute to the significantly reduced

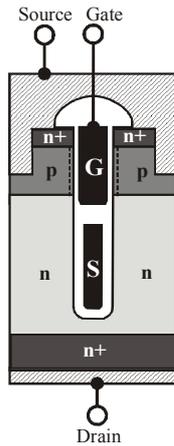


Fig. 3: Schematic structure of a field-plate MOSFET

area-specific on-resistance. Since the field-plate electrode is connected to the source electrode of the MOSFET and the gate is formed by a separate electrode, such a device offers an outstanding area-specific on-resistance and a low gate-charge at the same time.

### Improving the right device properties

Despite all the advantages, the introduction of charge-compensation is inevitably linked to an increase in the output capacitance  $C_{OSS}$  and the output charge  $Q_{OSS}$  due to the increased doping density compared to a standard MOSFET.

Here it is useful to consider the previously defined  $FOM_{OSS}$  since from an application point of view, the output charge for a given on-resistance is of interest. A simple optimization towards the lowest possible area-specific on-resistance by using a smaller cell pitch will lead to a degradation of the  $FOM_{OSS}$ .

Alternatively, a reduction of the  $Q_{OSS}$  is obviously possible by a further reduction of the drift region length, a lower drift region doping, and a decrease in the cell density. Unfortunately, these measures will degrade the area-specific on-resistance and/or affect the breakdown voltage.

Fig. 4 shows the dependence of the breakdown voltage on the trench depth and the linked drift region length at

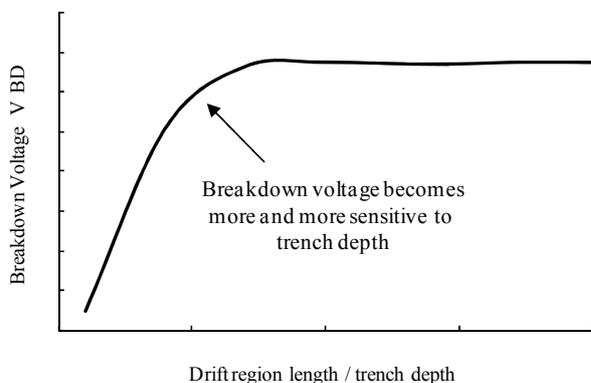


Fig. 4: Breakdown voltage dependence on trench depth / drift region length for constant doping level

a given doping level. The target is to minimize the trench depth without any deterioration of the breakdown voltage. The width and the depth of the trench will vary over the manufacturing process within a specific range and as such the charge in the mesa region, which forms a major part of the output charge, will vary as well.

Moreover, due to the process tolerances, the average trench depth must be deep enough to always ensure the required minimum blocking capability. Therefore a reduction of the trench depth variation by improved tools and better process control will allow for a simultaneous reduction of on-resistance and output-charge at the same time. Also, the variation of the trench width for a constant pitch does limit the device performance since the charge along the lateral direction must be compensated by the field-plate without exceeding the critical strength of the electric field. Again a better control of this parameter by improved tools and/or a more advanced lithography allows for a higher doping level linked to a better on-resistance and a more narrow range of the output charge variation at the same time. Of course there are many other process-related parameters where a better control directly leads to an improvement of the device parameters.

Independent of the exact device structure, these thoughts can be transferred to any similar device design. As example, Fig. 5 indicates the result for different ways of optimizing the  $FOM_{OSS}$  vs.  $R_{DS(ON)} \times A$ . Despite the clear improvement of both key parameters in the sweet spot, there are two particularly interesting facts to note. First, the strong reduction of the output-charge results in only a minor increase in the area-specific on-resistance compared to what would be achieved by a straightforward reduction of the on-resistance. Second, also the  $FOM_{OSS}$  of such an optimized device is competitive to devices with pure focus on output charge reduction.

### Faster switching and ease of paralleling

As already mentioned the absolute value of the gate-drain-charge  $Q_{GD}$  and its variation over the manufacturing process should be low. The requirement for a low variation range of this parameter is especially important when devices need to be connected in parallel

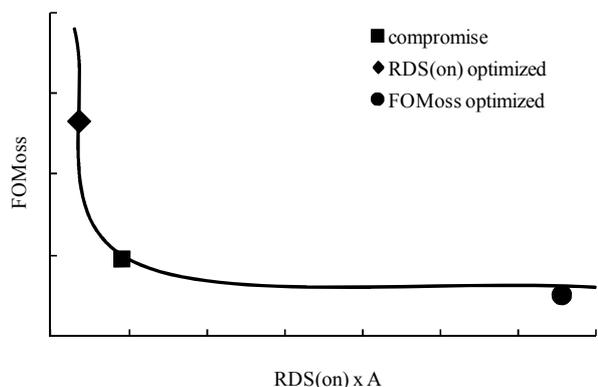


Fig. 5: Comparison of device performance of various optimized MOSFET devices

with each other, enabling a faster switching of the whole system. A small variation range of the  $Q_{GD}$  value also allows the minimization of safety margins. Here the optimized technology also benefits from the previously discussed improvements to the manufacturing process and equipment. Progress in the process details, a better process control and the optimized device geometry result in a much smaller range of the  $Q_{GD}$  compared to the predecessor technology as indicated in the cumulative plot shown in Fig. 6.

## DEVICE PERFORMANCE

### Test setup

To characterize the devices under real application conditions, a test bench was developed in a laboratory setup. To obtain meaningful results, a commercially available 750 W / 12 V server power supply unit with secondary side synchronous rectification was taken for verification. The topology is a phase-shift, full-bridge rectifier on the primary side [6] with hard-switched, center-tapped synchronous rectification stage on the secondary side as schematically shown in Fig. 7. To get comparable results it is essential always to have the same external laboratory conditions, such as constant temperature and use of the same measurement instruments for minimized tolerances. For the measurement of the AC input of the power supply, a Siemens power analyzer type B6040 was used. The output voltage was measured with a precision data acquisition unit type Agilent 34970A, and the current was logged using a high-current shunt resistor. To correctly analyze the voltage overshoot of the SR MOSFET, it is important to measure the signal as near to the package as possible, but not on the PCB. This avoids any influence of the parasitic stray inductances which can heavily affect the voltage signal due to the high di/dt environment.

Since it is essential in the development of new technologies to know as early as possible how the new device behaves in the target application, a simplified

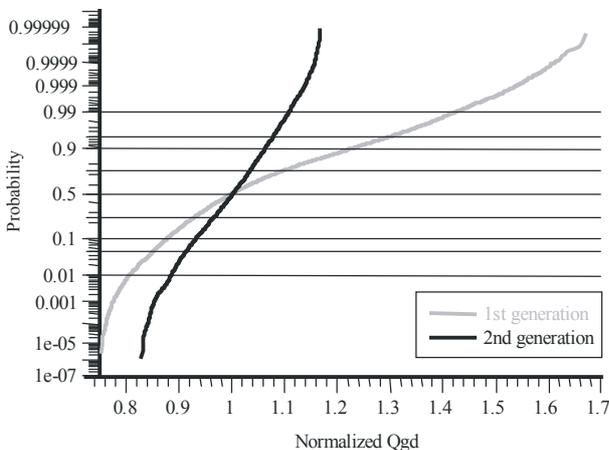


Fig. 6: Comparison of the range of the gate-drain charge  $Q_{GD}$  for 1<sup>st</sup> and 2<sup>nd</sup> device generation

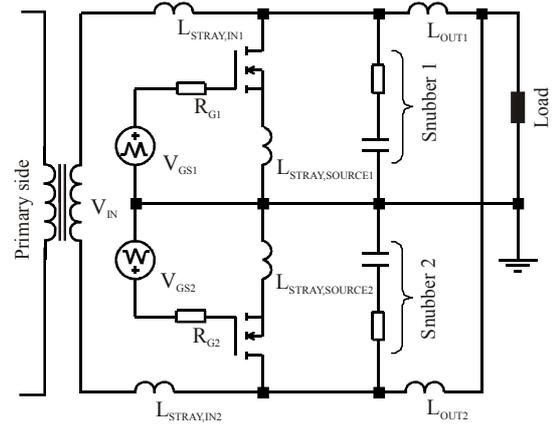


Fig. 7: Basic circuit for the hard-switched, center-tapped synchronous rectification test stage

synchronous rectification stage was implemented in a mixed-mode simulation circuit using Medici™ [7]. Both SR MOSFETs in the circuit shown in Fig. 7 are modeled by their full 2D structures. The input voltage  $V_{IN}$  reflects the voltage of the secondary side of the transformer. A safe dead-time of 250 ns was chosen for the gate voltages  $V_{GS1}$  and  $V_{GS2}$ . The simulations carried out reproduced the situation for a given operating point. The following parameter values were used in the simulations:  $L_{OUT1,2} = 10 \mu\text{H}$ ,  $L_{STRAY,IN1,2} = 20 \text{ nH}$ ,  $L_{STRAY,SOURCE1,2} = 2 \text{ nH}$ ,  $R_{G1/2} = 2 \Omega$ ,  $R_{Snubber1,2} = 2.7 \Omega$ ,  $C_{Snubber1,2} = 10 \text{ nF}$ .

### Voltage overshoot

As indicated before, voltage overshoots at turn-off of the SR MOSFET are a big challenge, especially for hard switched topologies. Designers need to ensure that the level of this peak does not exceed the maximum rating of the device. This often requires the use of a snubber network which is costly and furthermore typically decreases the performance of the SMPS [8]. A simple snubber consists of a series-connected resistor and capacitor, connected in parallel to the drain and source as shown in Fig. 7. Any reduction in the capacitance value improves the efficiency of the circuit.

Fig. 8 compares the simulated and measured voltage

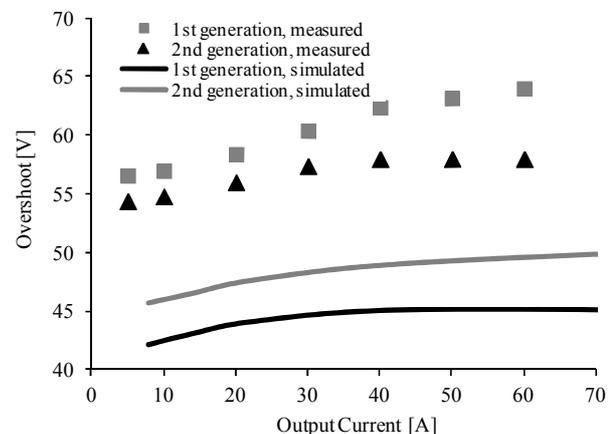


Fig. 8: Comparison of the voltage overshoot

overshoot (absolute values) in a synchronous rectifying stage for both device generations. Due to the lower output charge of the new device generation the voltage overshoot was clearly reduced over the full output current range. The results confirm the previously discussed improvement measures.

While the reduction in the overvoltage is equal in both the measurements and the simulations, the absolute values show a marked difference. The reasons are most likely caused by the simplifications done to the simulation circuit, i.e. the incomplete consideration of all parasitic elements in the real circuit.

A clear improvement is gained in the spiking behavior with 2nd MOSFET generation as compared to its predecessor technology over the full output current range. The reduced voltage spike reduces the stress for the MOSFET, leading to an improvement in device reliability, and also reduces the efforts involved in designing the snubber network.

### Efficiency of SR stage

In the measurements shown in Fig. 9 the efficiency is compared to the predecessor generation and a clear performance improvement was gained over the whole power range. The high-load efficiency is improved by up to 0.5 %, while at the same time the low-load efficiency is 0.3 % better. This result was achieved by the previously discussed improvements of the FOM<sub>G</sub> and FOM<sub>OSS</sub>. Thus, not only the R<sub>DS(ON)</sub> but also the switching charges like Q<sub>G</sub> and Q<sub>OSS</sub> are much lower than in the first generation device. Considering an efficiency level between 98 % and 99 % of the synchronous rectification stage, an improvement of 0.4 % clearly helps the designers of SMPS to reach their performance targets.

### Single-pulse avalanche ruggedness

During development, the single-pulse avalanche destruction current was investigated following a mixed-mode 2D simulation approach using two slightly different MOSFET cells as proposed in earlier work [9]. The good agreement of the simulated and measured destruction currents as shown in Fig. 10 indicates a proper chip design since no serious degradation is

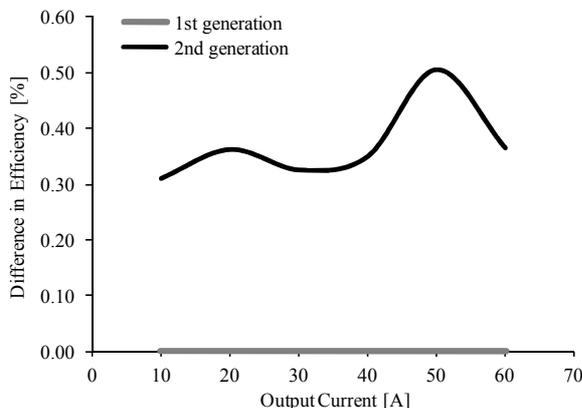


Fig. 9: Measured device efficiency in SR

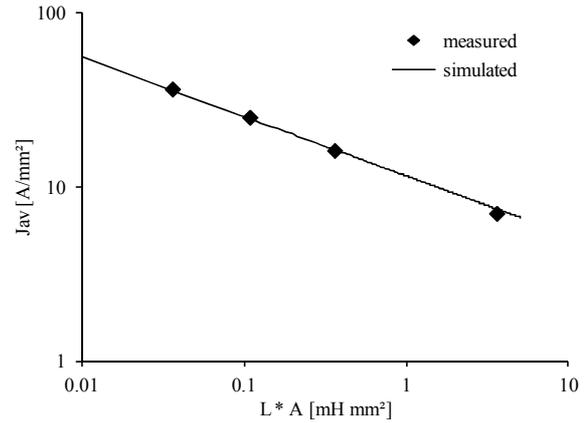


Fig. 10: Single-pulse avalanche destruction current

introduced by the real, three-dimensional device structure.

To compare the avalanche capability of the 1<sup>st</sup> and 2<sup>nd</sup> generation, single-pulse avalanche measurements were done for different inductances and temperature values. Fig. 11 presents the result of these measurements for devices having an identical active area. To estimate the intrinsic temperature, extrapolation lines are fit to the average failure current points determined at the various temperatures. The intersection point with the zero-current line is found at the intrinsic temperature of the device.

The thermal destruction is found at approximately the same intrinsic temperature for both device generations under identical conditions. Consequently, the improved device properties are not linked to an avalanche weakness.

### Repetitive avalanche ruggedness

As briefly discussed before, avalanche events can affect the device in a synchronous rectification stage. To learn more about the device behavior, the D.U.T. having an R<sub>DS(ON)</sub> = 2 mΩ underwent a repetitive avalanche stress test for a predefined number of cycles with the following, rather harsh conditions: I<sub>AV</sub> = 46 A, E<sub>AV</sub> = 240 μJ, f = 80 kHz, T<sub>AMB</sub> = 55 °C.

To monitor the device characteristics during the test, the devices were compared in efficiency and overshoot in the SR test bench before and after the repetitive

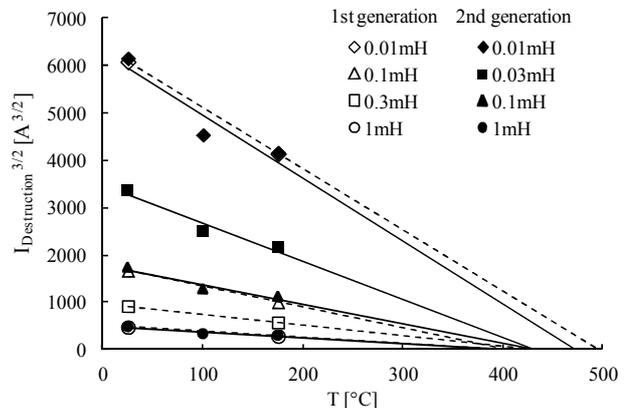


Fig. 11: Avalanche capability vs. junction temperature

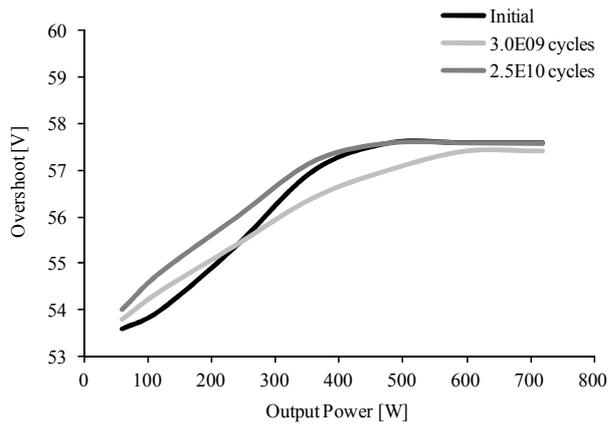


Fig. 12: Overshoot of repetitive avalanche stressed devices in a SR stage for a different number of cycles

avalanche stress. Fig. 12 indicates the voltage overshoot as a function of output power for a number of stress cycles, while Fig. 13 shows the measured difference in efficiency. The found changes were very low and in the range of the measurement precision.

## CONCLUSION

This paper discusses the optimization of MOSFET technologies designed to be used for synchronous rectification. To improve the overall efficiency it is clearly not sufficient to focus only on low  $R_{DS(ON)}$ . As the current efficiency targets also require high levels of low load performance, all switching losses need to be minimized at the same time. To fulfill these needs, the  $FOM_G$  and  $FOM_{OSS}$  have to be dramatically decreased simultaneously.

By using improved manufacturing setups this step is now possible, as practically proven by application measurements. The efficiency level can be increased by up to 0.3 %...0.5 % while at the same time the voltage overshoot can be reduced by up to 7 V. Such characteristics enable an easy design-in process with less effort for the designers of SMPS.

It is further shown that these improvements do not compromise the single-pulse avalanche capability of the

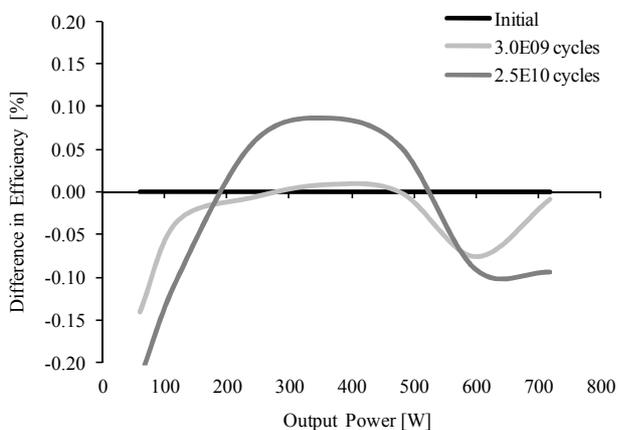


Fig. 13: Difference in efficiency for repetitive avalanche stressed devices in a SR stage for a different number of cycles

device and that no significant shift in the device performance is expected in case of repetitive avalanche events.

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