Boosting efficiency in resonant converters by the use of a new advanced power MOSFET technology

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Keywords

«power semiconductor device», «MOSFET», «new switching devices», «efficiency», «resonant converter»

Abstract

This work discusses the advantages of a new trench power MOSFET technology applying a new design approach. Along with the improvements recorded in the main switching figures of merit, the recently introduced technology is also proven to shine in soft-switching ZVS applications. It is shown how the new device design practically eliminates one of the loss mechanisms in the device itself when operated in ZVS, supporting a clear improvement in the overall system efficiency.

Introduction

Since their introduction, MOSFET technologies have been seen as excellent candidates for use as switches in power management circuits.
Low-voltage power MOSFETs based on charge-compensation using an isolated field-plate, as shown in Fig. 1, offer a significant reduction of the area-specific on-state resistance [1] – [12]. Thanks to their overall excellent performance, this class of devices has become established as the standard device of choice for applications requiring fast-switching power devices. Potential target applications include primary side switches and synchronous rectification stages of switch-mode power supplies, low-voltage motor drives and solar power optimizers. Consequently, these devices are used in both hard- and soft-switching topologies.
Soft-switching techniques, as employed for example in resonant topologies, allow a further improvement of the efficiency in power supplies used for telecom rectifiers or servers [13] - [15]. Although these techniques reduce losses on the primary side, they do not address the secondary side rectification-related losses. In order to also minimize losses on the secondary side, diodes were replaced by power MOSFETs acting as synchronous rectifiers (SR). This measure dramatically reduced the rectification conduction losses and enabled a further increase of the converter efficiency and the power density [16].

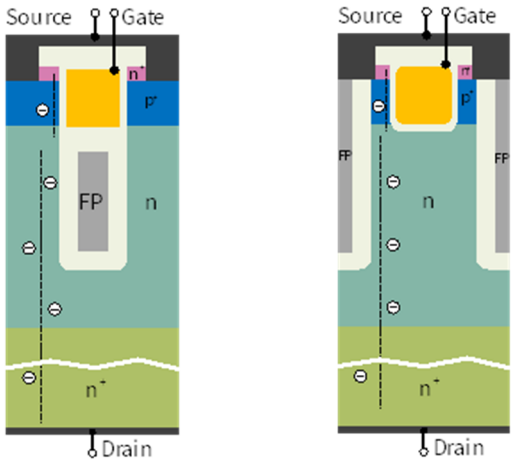

Fig. 1: Exemplary trench MOSFET structures
a) gate electrode stacked on top of the field-plate electrode in one trench
b) gate electrode and field-plate electrode arranged in separate trenches

As for any switched power device, losses related to the switching of the SR MOSFETs also contribute to the overall losses. This means that especially the output capacitance and the related charge of the power device will have a significant impact, as well as the reverse-recovery charge Q_{RR} in the case of body diode conduction. Consequently, the device structure plays an important role, as it not only defines the total amount of charge, but also alters the voltage dependence of the capacitance, which will vary more or less non-linearly with the voltage applied over the power semiconductor device. The device design also governs the value of the gate charge Q_G and of the gate-drain charge Q_{GD}. A low gate charge is desirable as it proportionally affects the driving losses. A part of the total gate charge is associated with the gate-to-drain charge Q_{GD}, which in hard-switching governs the drain voltage transient. A higher Q_{GD} impacts the transient speed, increases the switching losses, and forces the use of longer dead-times. Longer dead-times link to a longer time of body diode conduction and hence a larger reverse-recovery charge Q_{RR}.

Latest developments in the field of charge-compensated low-voltage power MOSFETs introduce a new device design that replaces the commonly used design based on stripe-shaped trenches by a grid-like approach [17]. This approach not only enables a further reduction of the area-specific on-resistance, but also provides an improvement in the figure-of merits.

This work focuses on the impact of the device properties on the performance and efficiency of the LLC resonant topology. Two different device structures employing charge-compensation with a stripe and grid layout configuration are investigated, and it is explained how the new device approach contributes towards a higher efficiency by addressing one of the main loss contributors in a resonant topology.

Novel device concept

New MOSFET devices are required to provide improvements across all figures of merit, as this is needed to enable high-frequency SMPS operation where losses are associated both with charges (switching) and on-state resistance (conduction). To meet these requirements, a novel cell-design approach was developed which explores a true three-dimensional charge compensation.

State-of-the-art MOSFET technologies currently use an insulated field plate underneath and separated from the gate electrode in a deep trench as shown in Fig. 1a. These employ a stripe layout as depicted in Fig. 2. The new design separates the field plate trench, which is now formed with a needle-like deep trench structure, from a grid-like gate trench which surrounds the needles as shown in Fig. 3. Fig. 1b shows the respective schematic cell cross section. This increases the silicon area available for current conduction, allowing for a further reduction in the overall on-resistance [17].

In order to improve the values of the two figures-of-merit $FOM_G = R_{DS(on)} \times Q_G$ and also $FOM_{GD} = R_{DS(on)} \times Q_{GD}$, the gate trench design aims to minimize its lateral extension.

However, the substantially smaller dimensions of the gate now impose a new challenge, as the use

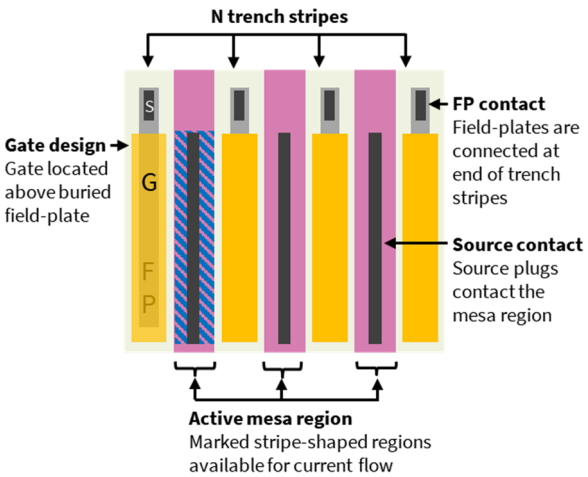

Fig. 2: Typical Trench MOSFET with commonly employed stripe layout approach, with gate electrode over field-plate electrode

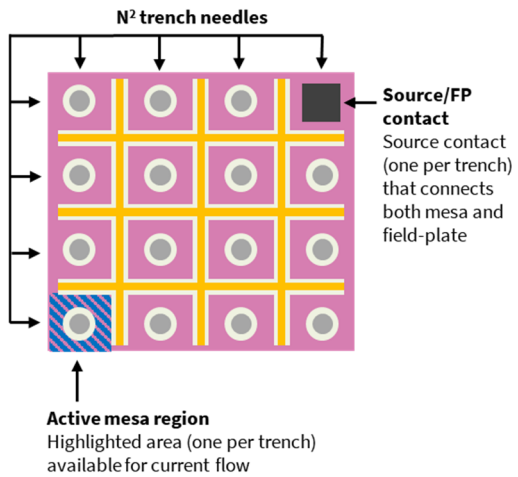

Fig. 3: Trench MOSFET structure with the new grid-like layout approach, with gate electrode and field-plate electrode in separate trenches

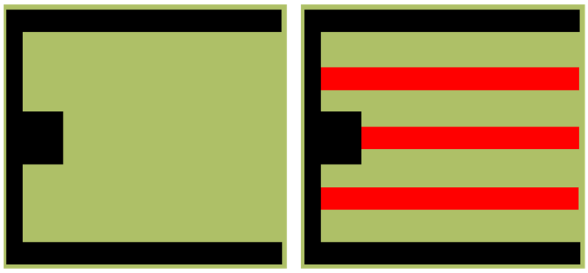

Fig. 4: Illustration of active area loss on a MOSFET chip due to the introduction of gate fingers marked in red. This area is lost for current conduction.

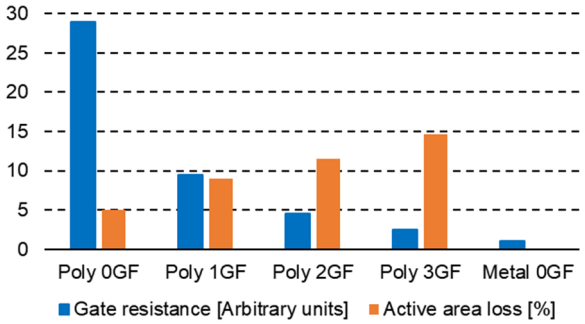

Fig. 5: Gate resistance and active area loss depending on the number of gate fingers (GF) for a best-in-class chip in a PQFN 3.3 x 3.3 mm² package [17]

of polysilicon as the gate material would result in unacceptably large internal gate resistances. This issue is usually solved by the introduction of gate fingers. However, the introduction of gate fingers reduces the active area available for current conduction, as the metal of the gate finger structure must be separated from the source metal area. This is schematically shown in Fig. 4, where the red stripes indicate the area being occupied by the gate fingers and the required lateral insulation against the source metal, i.e. the area that becomes unavailable for current conduction.

Fig. 5 illustrates the loss of active area by the introduction of gate fingers using the example of a best-in-class device in a PQFN (Power Quad Flat No-Lead) 3.3 x 3.3 mm² surface mount package. To avoid this rather significant loss of active area, a metal gate system has been introduced that not only reduces the internal gate resistance, but also significantly improves the gate resistance uniformity over the chip [17].

Fig. 6 summarizes the improvements in the main parameters over the previous technology generation for both voltage classes.

Improved switching behavior

The new device concept offers substantial benefits in switching performance, providing reductions in the switching losses under both hard and soft switching conditions. The metal gate in combination with the use of a gate grid layout, together with a direct connection of the field-plates to the source metal, realizes a device set-up that ensures a very fast and homogeneous transition at turn-on and turn-off. This not only minimizes switching losses, but also reduces the risk of an unwanted dv/dt induced parasitic turn-on of the MOSFET. To enable an understanding of the differences in the switching behavior between a traditional stripe layout and the grid layout approach used in the new technology, the potential distribution during the switching of the device is studied based on circuit simulations representing the chip. This approach uses a distributed SPICE model of the transistor and connects 25 x 30 transistor elements within a grid network, which extends over the chip in both directions. The connections between local gate, source and field-plates are modelled by resistive elements.

The values of the resistors represent the material properties of the material used and the geometric dimensions of the respective electrode or layer. The transistor cells, which are located on the crossing points of the resistor network, scale with the fraction of the chip area that results from the chosen number of elements in the grid. Other functional elements, like the gate-pad or gate and source runners, are added to the circuit as necessary for a more precise description of the chip.

A transient simulation of the distributed SPICE model now allows a realistic study of the chip

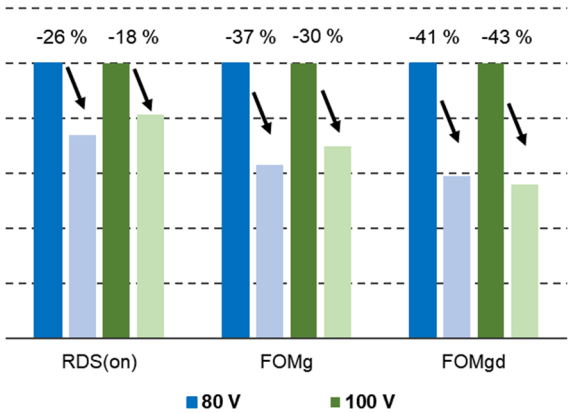

Fig. 6: Improvement in device performance for best-in-class devices in PQFN 5x6 package

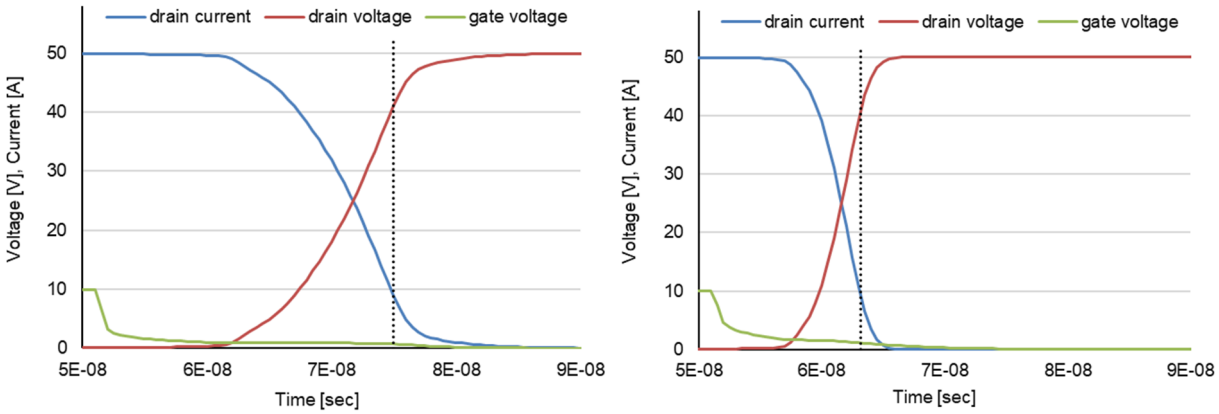

Fig. 7: Comparison of the circuit-simulated turn-off characteristics for the previous and new device technology

behavior. In contrast to the case of simple RC networks, this approach includes full device models for active cells. As such, this approach correctly considers the voltage-dependence of capacitances as well as feedback effects due to the miller capacitance, and yields the local signal propagation over the chip. Fig. 7 compares the simulated turn-off waveforms for the two technologies, assuming for both cases a chip size of 12 mm². The characteristics show that the new technology generation with the grid-like gate layout enables a shorter delay time, and clearly switches faster. It only needs approximately half the time of its predecessor.

Fig. 8 depicts the gate potential distribution over the chip at the point in time that is marked by the

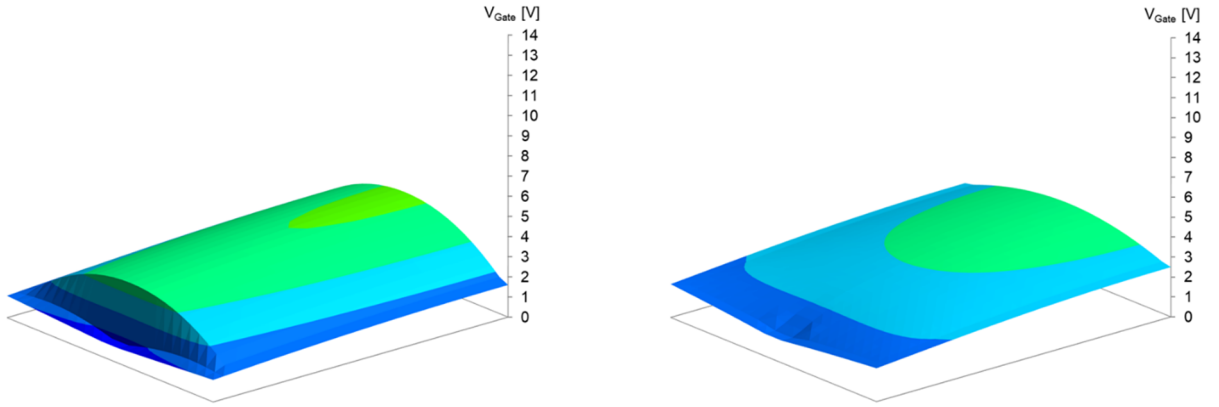

Fig. 8: Comparison of the gate potential distribution over the chip for the previous and new device technology at the point in time marked by the dotted line in Fig. 7

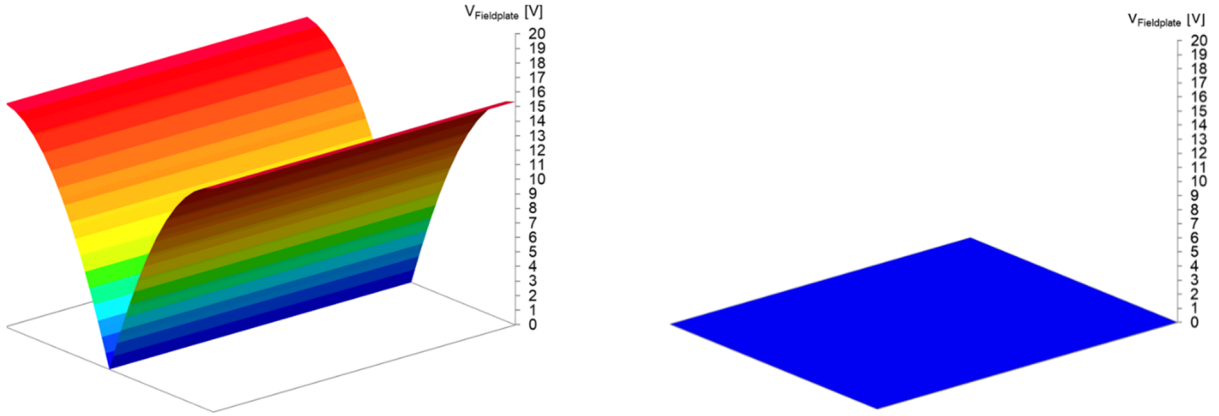

Fig. 9: Comparison of the field-plate potential distribution over the chip for the previous and new device technology at the point in time marked by the dotted line in Fig. 7

dotted line in Fig. 7, and is chosen for identical working points for both devices. Thanks to the combination of a metal gate with the gate grid layout, the new device shows a clearly improved homogeneity of gate potential across the chip. This supports faster switching of the chip. The improved switching homogeneity is also advantageous for device robustness, for example avalanche ruggedness, by reducing the probability that a part of the chip is affected by gate signal delays [18] or parasitic turn-on. Both effects degrade the device ruggedness as power dissipation is limited to just a part of the chip.

Fig. 9 now compares the distribution of the field-plate potential across the chip, which is actually completely flat for the new technology generation as the trench electrodes connect directly to the source metal. As can be seen from the comparison to the previous generation device with a stripe layout, the improved chip switches extremely homogeneously, supporting fast transitions between the on- and off-state and vice versa. Moreover, the direct connection between the source and field-plate practically eliminates any resistance in series with the output capacitance. This minimizes ohmic losses while charging and discharging the output capacitance.

This property of the device is especially important for its use in resonant topologies, as will be discussed in the following sections. It is further beneficial for achieving a high avalanche ruggedness, as an increased local field-plate potential may alter the local breakdown voltage [19], leading to an inhomogeneous power dissipation over the chip area.

The Intermediate-Bus Converter

The Intermediate-Bus Converter (IBC) within the so called intermediate-bus architecture (IBA) is a DC/DC converter which performs a mid-conversion to feed the downstream point-of-load (POL) step-down converters (see Fig. 10). This architecture is popular in telecom and server applications, where DSP chips and microcontrollers which operate at very low voltages (1.2 V ~ 5 V) are powered locally by the POL converters, yielding a more efficient system [20]. Since the loads have their supply voltages regulated by the POL converters, the IBC converter may be operated in open loop. Between the front-end power supply and the IBA load are two cascaded converters: the IBC and the POL converters. Now the IBA system must operate with high efficiency, and this requires the IBC

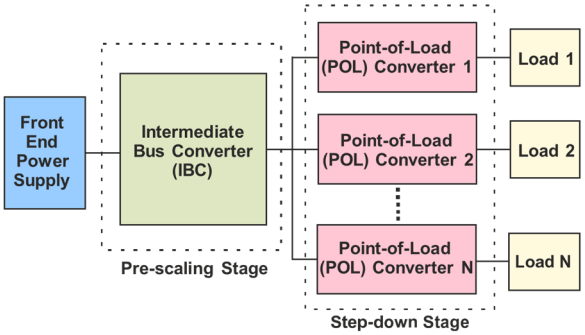

Fig. 10: System diagram of the intermediate bus architecture

converter to have an extremely high efficiency. For common 48 V telecom and datacom systems, the front-end power-supply voltage ranges between -40.5 V and -57 V [21]. Given the relatively narrow range of the IBC input voltage, and the requirement of extremely high converter efficiency, the LLC topology as depicted in Fig. 11 appears to be a perfect choice for this type of converter.

The LLC converter

General topology

The LLC is a resonant converter. Unlike conventional approaches based on pulse-width modulation (PWM) that work with a fixed frequency and a variable duty cycle, the LLC works with frequency modulation. Simply put, the LLC converter attains zero-voltage switching (ZVS) in the primary-side switches Q_1 to Q_4 for a wide range of output load.

The ZVS is realized through the transformer magnetizing inductance L_{MAG}. Its value has to be defined by taking into account the primary-side MOSFETs' output-capacitance C_{OSS}, as the magnetizing current I_{LMAG} must be tailored to

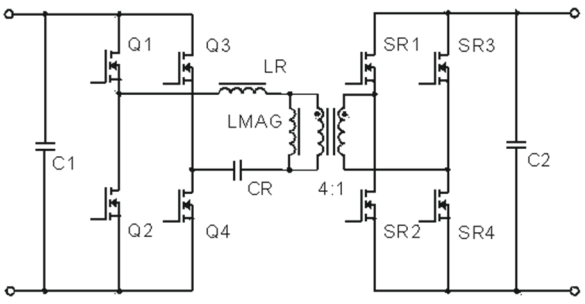

Fig. 11: Full-bridge LLC converter with full-bridge synchronous rectification on the secondary side

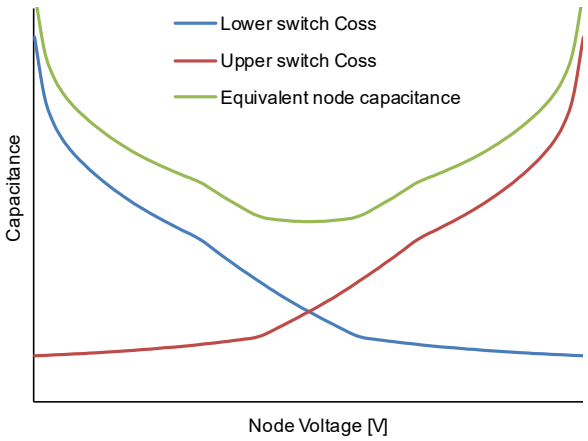

Fig. 12: Effective capacitance at the node between Q_1 and Q_2 or the node between Q_3 and Q_4 in the primary full-bridge (see Fig. 11) [22]

fully charge and fully discharge a bathtub-shaped effective phase-node capacitance, as seen in Fig. 12 [22]. This condition must be fulfilled over the entire specified input voltage range, regardless of the level of the output load. This ensures that all of the primary-side MOSFETs operate in soft switching.

Each MOSFET in the full bridge is switched at a constant 50 % duty cycle ratio. The inductor L_R forms a series-resonant circuit with the resonant capacitor C_R, which builds up a quasi-sinusoidal current fed through the transformer to the secondary side, which is rectified by the synchronous rectification stage SR_1 to SR_4. Details on the determination of the required values for L_{MAG}, L_R and C_R can be found in [23].

The SR MOSFETs operate in ZVS and quasi zero-current switching (ZCS), virtually eliminating most of the losses associated with their commutation. The resulting rectified current is split into an AC component, which is taken over by the output-capacitor's filter, and a direct current that flows to the load.

Fig. 13 illustrates the current path and the basic waveforms for the LLC converter in fully resonant operation.

Regulated LLC

The output voltage can be regulated by the variation of the switching frequency around the resonant frequency defined by L_R and C_R. Fig. 14 illustrates the dependence of the LLC voltage gain on the frequency. These AC transfer characteristics are the result of an AC analysis; here only the fundamental component of the square-wave voltage input to the resonant network contributes to the power transfer to output. The transformer, rectifier and filter are replaced by an equivalent AC resistance [23]. When the switching frequency equals the resonant frequency, the converter voltage gain is equal to one. ZVS switching is ensured by L_{MAG}, since the resonant current is exactly in phase with the transformer voltage at resonance.

When operated below resonance (within the ZVS/ZCS boundary), the converter is able to boost the input voltage, while switching frequencies higher than the resonant frequency lower the converter output voltage and the converter operates in step-down mode with ZVS

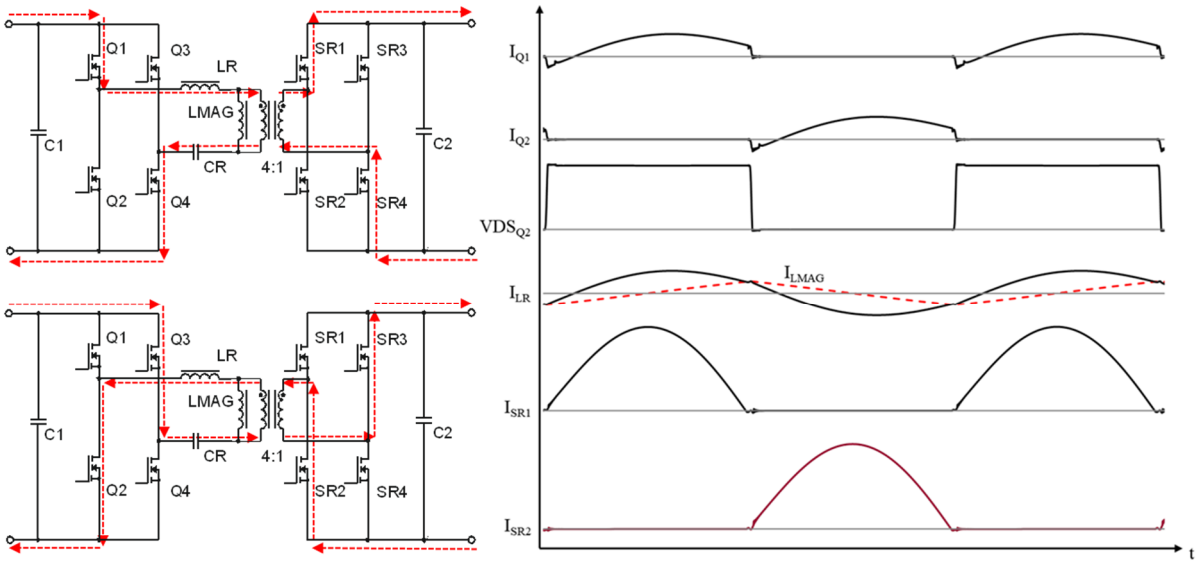

Fig. 13: Current path and basic waveforms for the LLC converter in fully resonant operation

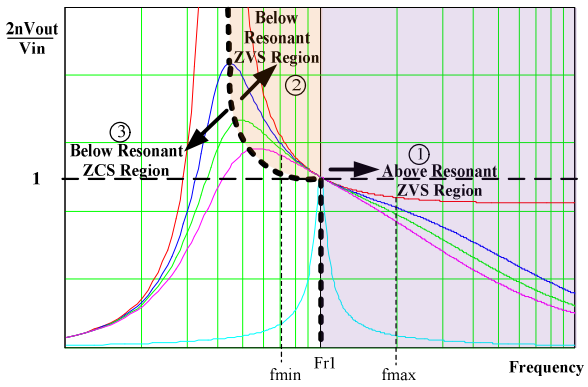

Fig. 14: Typical dependence of voltage-gain on frequency of an LLC resonant converter, shown for five different load conditions [23]

achieved by the phase-lag introduced in the current by the resonant tank.

Secondary side rectification

Fig. 11 also shows the synchronous rectification (SR) MOSFETs on the secondary side. These MOSFETs replace the previously used secondary-side rectifying diodes. Despite the added complexity and cost they clearly increase the gain in the overall converter efficiency [24]. This improvement in efficiency more than compensates the added circuitry cost through the savings obtained in the energy costs throughout the system's lifetime.

Synchronous rectification can be implemented in the LLC converter either by full-bridge or by a center-tapped full-wave rectifier. The full-bridge configuration for the synchronous rectifiers has the advantage of a simple transformer design (single secondary winding). The single-ended transformer allows better interleaving among primary and secondary windings, offering lower AC resistance. It also benefits from better switching FOMs, as in contrast to a center-tapped transformer it allows the use of MOSFETs with a lower breakdown voltage. The downside of the full-bridge configuration is its complexity and higher cost when compared with the center-tapped approach, as two SR MOSFETs are connected in series during rectification and two half-bridge drivers are required to drive the SR MOSFETs.

The full-bridge SR approach has gained traction, despite the aforementioned disadvantages, especially in high power designs that use PCB planar transformers, since the single secondary winding yields a more effective PCB layout. A simpler layout together with a single rectifier helps to reduce conduction losses, since the secondary windings have fairly high RMS currents flowing through them, especially when the converter output voltage is low.

Loss mechanism in the LLC contributed by the MOSFET

As mentioned above, in the LLC converter – at least when operated at resonance – all the MOSFETs are soft-switched (either at zero-voltage or at zero-current), meaning that the switching losses are assumed to be negligible. So the only losses to consider are the conduction and gate-drive losses.

The ZVS on the primary side occurs thanks to the transformer magnetizing current $I_{L_{MAG}}$ that forces a transfer of charge, on each half-bridge leg, between the output capacitances of Q_1 and Q_2 as well as of Q_3 and Q_4. This transfer of charge requires a certain amount of time to complete, which determines the required dead-time (i.e. the time during which both the high side and the low side MOSFETs are in the off-state). This time depends on the amount of the output charge Q_{OSS} of the primary-side MOSFETs. Consequently, this charge-transfer time may impose a limit on the maximum switching frequency, since part of the switching period is needed for the charge-transfer mechanism. Moreover, the higher the MOSFETs Q_{OSS}, the higher the required magnetization current. The higher this current is, the higher the corresponding conduction losses in the PCB tracks and in the transformer windings.

However, in addition to these there is another loss mechanism contributed by the power device itself, which is usually neglected: the so-called R_{OSS} related losses. Fig. 15 shows a simplified representation of the MOSFET, highlighting its field-plate resistance R_{OSS} in series with its field-plate capacitance C_{OSS}. Every time C_{OSS} is either charged or discharged, a large portion of the magnetizing current I_{LMAG} passes through R_{OSS},

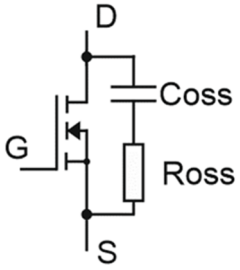

Fig. 15: MOSFET with its internal field-plate capacitance C_{OSS} and field-plate resistance R_{OSS}

causing conduction losses which may become significant, depending on the device setup.
The new MOSFET technology now has a much lower R_{OSS} value, as indicated by the practically non-existent field-plate voltage potential distribution during switching as shown in Fig. 9. In a resonant topology such as the LLC, this device property helps to achieve a significant reduction in the switching losses. The same is true for the secondary-side. Here a MOSFET with low Q_{OSS} and with low R_{OSS} further allows for an increase in the switching frequency and a consequent reduction in the size of the reactive elements (magnetics and capacitors), enabling in turn a higher power density.

Test results of 1 kW 4:1 IBC for datacenters

The test platform is represented by a 1 kW 4:1 open-loop LLC DC-DC intermediate bus converter (IBC), operating as a DC transformer from an input which may vary from 42 V to 60 V. The devices under test are located on the primary-side full-bridge of the converter. The converter requires MOSFETs with an effective $R_{DS(on),max}$ = 1.45 mΩ in each leg of the primary-side full-bridge. To achieve this, two 80 V MOSFETs in PQFN 5x6 mm² packages with an $R_{DS(on),max}$ = 3 mΩ are paralleled. On the secondary-side, four IQE006NE2LM5 25 V source-down devices in PG-TSON-8-4 3.3x3.3 mm² packages are used in parallel arranged in a full-bridge configuration (see Fig. 11). The turns ratio of the transformer is 4:1. The resonant frequency of the LLC converter is 310 kHz. The switching frequency is fixed, so that the converter operates at resonance over the whole input voltage and load range. ZVS for the primary-switches and ZVS / ZCS for the SR switches are achieved by design. Fig. 16 shows both sides of the board, which spans over a standard quarter-brick form factor. The use of different device generations on the primary-side calls for the use of different dead-times. To run comparable tests, the dead-times need to be adjusted such that the effective body diode conduction time is the same for both devices under investigation.

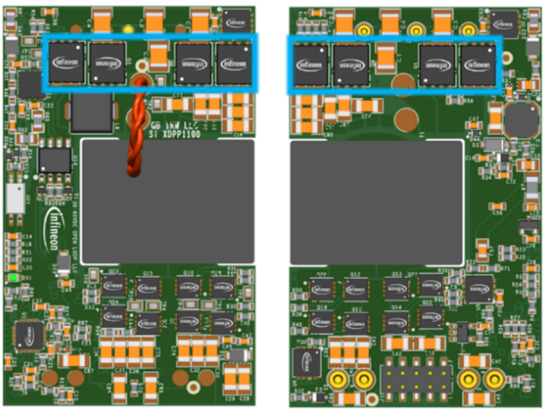

Fig. 16: Top and bottom view of the 1 kW LLC DC-DC board with the primary side MOSFETs (DUT) marked in blue

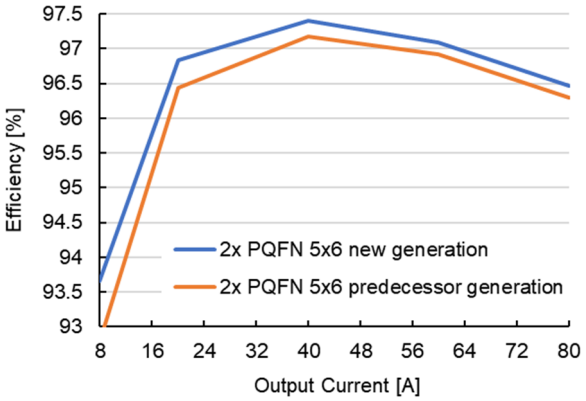

Fig. 17: Gained efficiency comparison for the use of two devices of each generation in the 4:1 LLC IBC (V_{IN} = 54 V)

First of all, the two 80 V primary side devices BSC030N08NS5 of the predecessor generation OptiMOS™ 5, based on a traditional design as depicted in Fig. 2, are replaced by two devices ISC031N08NM6 of the new device generation OptiMOS™ 6 that employ advanced design ideas as illustrated in Fig. 3. All devices come with a typical on-resistance of 2.6 mΩ. Fig. 17 compares the measured efficiencies. With the use of the new generation of devices, the overall efficiency improves over the full output current

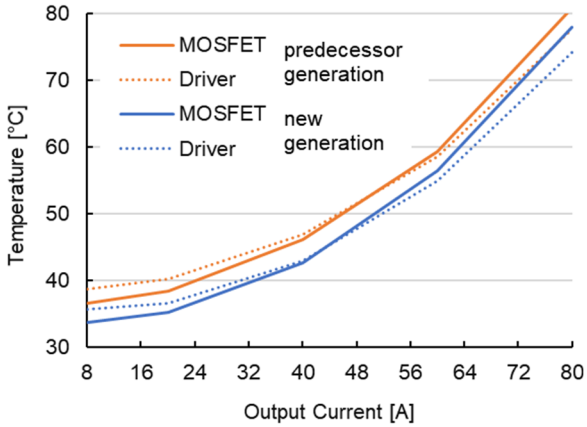

Fig. 18: Temperature comparison of the primary-side MOSFET and of the driver IC (V_{IN} = 54 V)

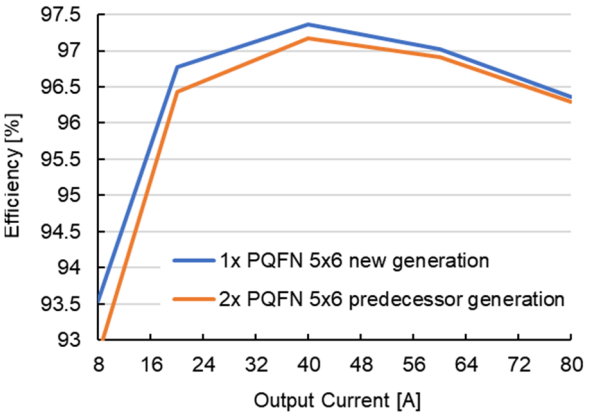

Fig. 19: Comparison of the gained efficiency improvement for the use of a different number of devices in the 4:1 LLC IBC (V_{IN} = 54 V)

range, with a peak improvement of almost 0.9 % at low load.

Fig. 18 indicates the temperature of the primary-side MOSFETs, where the temperature of the new OptiMOS™ 6 devices is lower than that of the previous OptiMOS™ 5 devices over the full load current range. The temperature also reduces for the driver ICs.

The significantly improved device parameters of the new technology generation not only improve the overall efficiency of the converter, but also allow the replacement of the two paralleled MOSFETs in each leg of the primary side by just one new OptiMOS™ 6 device ISC014N08NM6 with halved $R_{DS(on),max}$ of 1.45 mΩ. Fig. 19 compares the efficiency in this case. With up to 0.8 % better values for the latest device technology, the efficiency improvement is only slightly lower than in case of using two devices. Fig. 20 even indicates a lower package

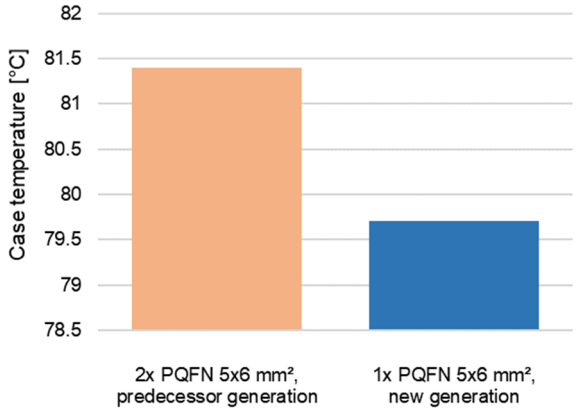

Fig. 20: Case temperature for the different number of used devices in the 1 kW LLC converter at maximum output current

temperature for the single die of the new generation compared to the two from the previous one.

The slightly lowered efficiency in this case can be explained by having the losses dissipated in just half of the devices. Also the output charge of the devices differ slightly which requires a properly adjusted dead time to achieve ZVS operation over the full load range. Together with a revised board layout with optimized placements of the single switches and the surrounding components, it is expected to deliver the same or higher efficiency as obtained using two paralleled devices.

Conclusion

This work discusses the performance of our latest power MOSFET technology in the resonant topology of an LLC converter. The MOSFETs use a unique device structure, which is the first to employ a three-dimensional charge compensation combined with the first ever use of a metal gate in a trench power MOSFET. The reduction achieved in the on-resistance, the dramatically-lowered gate charge and gate-drain charge, together with a low output charge and strongly improved switching homogeneity across the device area, enhance the system efficiency across all load conditions. The new device structure is also beneficial for the internal body diode of the MOSFET. Because the silicon area conducting current is increased, the body diode current density is decreased, which for the same current level means a decreased reverse recovery charge. Due to the resonant nature of the LLC topology, typical switching losses are eliminated to a large degree. Especially the losses due to the stored charge in the output capacitance of the power semiconductors are largely avoided, as this charge now swings from one MOSFET to the other one instead of being dissipated during a hard turn-on of the device. However, the swing current is linked to conduction losses due to the PCB tracks, the transformer windings and the internal series resistance R_{OSS} connected to the output capacitance C_{OSS} of the device structure, but this series resistance R_{OSS} is effectively eliminated in the new technology.

Efficiency measurements between the previous OptiMOS™ 5 and new OptiMOS™ 6 generation of devices in a 1 kW LLC IBC yield clear benefits for the new technology, and confirm the findings at the semiconductor level of an efficiency boost of up to 0.9 %. It is even possible to replace two devices of the previous generation with just one

using the new technology whilst still gaining up to 0.8 % in efficiency.
This not only represents an advantage in terms of a bill-of-materials (BOM) saving. Saving real space on the PCB opens the doors for a further optimization at the system design level, which is expected to further boost the efficiency.
Overall, these improvements offer a significant improvement not only for the demanding requirements of the telecom power arena, but also other application fields. The option to replace two devices by just one offers further chances to reduce converter sizes and increase the power density.

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