Stability and performance analysis of a SiC-based cascode switch and an alternative solution

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ABSTRACT

Wide band-gap semiconductors are most attractive as materials for power devices due to low losses, improved temperature capability and high thermal conductivity. Although silicon carbide Schottky diodes have been commercially available on the market for years, an active wide band-gap switch is still missing. Probably the best performance of upcoming devices is gained with normally-on concepts such as silicon-carbide JFETs and gallium-nitride HEMTs. However, the vast majority of power electronic topologies rely on normally-off switches. An alternative approach is the use of the cascode concept which combines a normally-on wide band-gap device with high blocking capability and a low-voltage normally-off silicon MOSFET. In this work, the performance and stability of such an arrangement is analyzed and an alternative solution is proposed.

KEYWORDS

JFET, MOSFET, SiC, Cascode, Stability, Performance

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SYMBOLS

V_{PT}	punch-through voltage of JFET
V_{PI}	pinch-off voltage of JFET
$R_{(DS)ON}$	on-resistance
$C_{GS,M}$	gate-source capacitance of MOSFET
$C_{GD,M}$	gate-drain capacitance of MOSFET
$C_{DS,M}$	drain-source capacitance of MOSFET
$C_{GS,J}$	gate-source capacitance of JFET
$C_{GD,J}$	gate-drain capacitance of JFET
$C_{DS,J}$	drain-source capacitance of JFET
$R_{G,M}$	gate-resistor of MOSFET
$R_{G,J}$	gate-resistor of JFET
$V_{BR,M}$	breakdown voltage of MOSFET
$V_{PLAT,M}$	plateau voltage of MOSFET
$V_{GS,M}$	gate-source voltage of MOSFET
$V_{DS,M}$	drain-source voltage across MOSFET
$V_{GS,J}$	gate-source voltage of JFET
$Q_{GD,M}$	gate-drain charge of MOSFET
$g_{fs,J}$	transconductance of JFET
V_{DS}	drain-source voltage
Q_{DS}	drain-source charge
V_{SS}	supply voltage
V_{OSC}	voltage amplitude of superimposed oscillation
$V_{OVERSHOOT}$	maximum overshoot voltage
L_S	source inductance of cascode
L_{stray}	stray inductance
I_{DC}	load current
E_{on}	turn-on switching losses
E_{off}	turn-off switching losses
T_j	junction temperature
t_{av}	duration of avalanche

1. INTRODUCTION

Recently a number of active wide band-gap power devices have been announced [1-6]. Several device concepts have been proposed such as BJT [2], MOSFET [3,4], normally-off and normally-on vertical JFET [5,6] or normally-on quasi-vertical JFET [7]. Fig. 1 depicts the basic structures of the aforementioned devices. All devices show specific strengths and weaknesses.

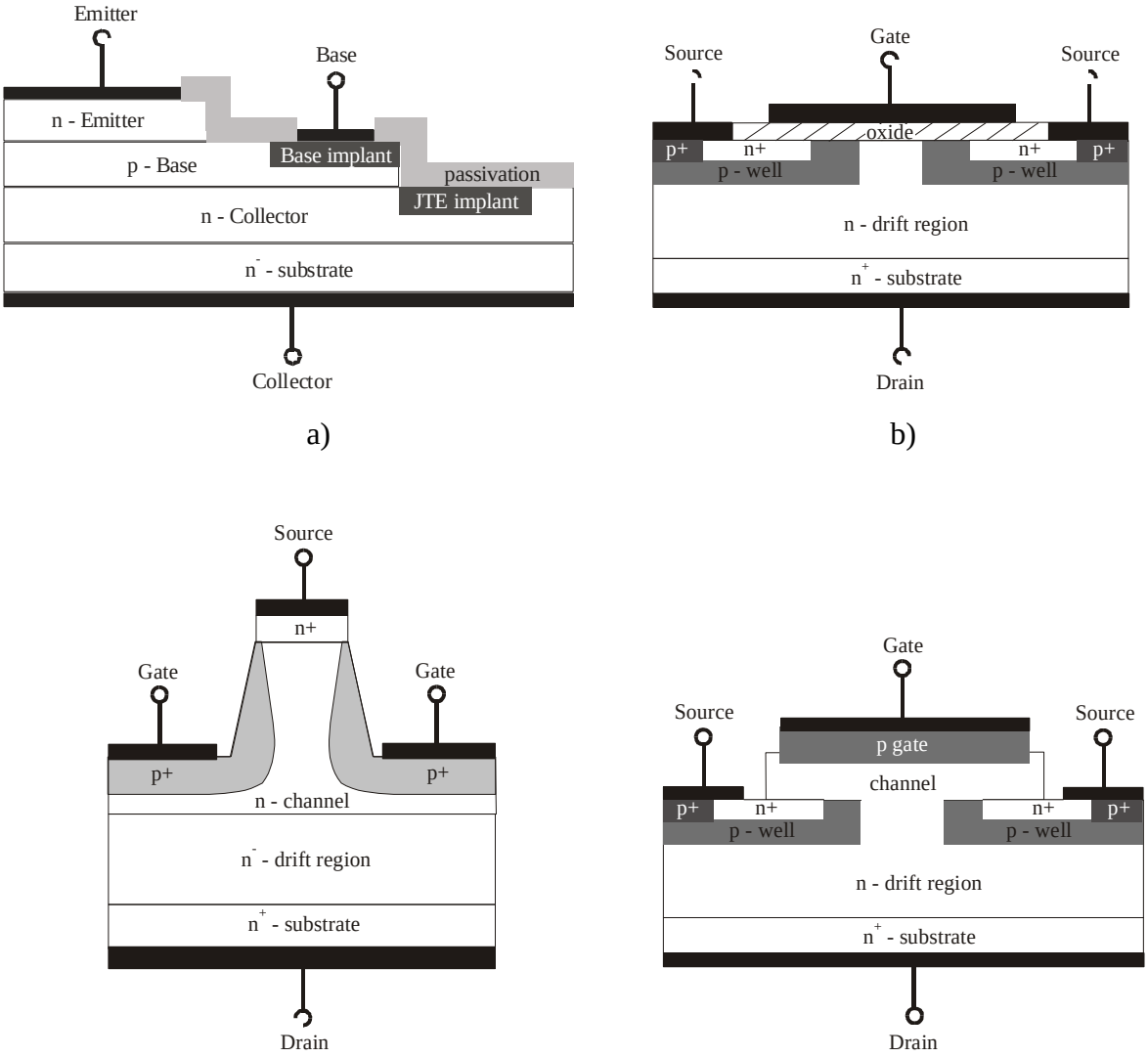

Fig. 1: Basic structure of
a) SiC BJT
b) SiC MOSFET
c) vertical normally-off SiC JFET
d) quasi-vertical normally-on SiC JFET

The BJT is a normally-off device, but being current-controlled it requires the use of a special driver circuit. Current gain degradation might occur due to stacking faults [8,9].

The MOSFET is a voltage-controlled normally-off device which makes this device rather user-friendly. The MOSFET also has an inherent body diode. However, the overall performance is affected by low channel mobility due to the presence of interface traps which limits the transconductance and currently requires a larger gate voltage range to drive the device for its full performance. Also the decrease in the threshold voltage of SiC MOSFETs at high temperature is still not satisfying. Moreover the high density of extrinsic defects is still an issue which can negatively affect SiC MOSFETs [9]. However, first MOSFETs are meanwhile available in the 1200 V class where their offer a very good performance [4].

Vertical JFET devices, irrespective of whether they are normally-on or normally-off, lack an inherent drain-source body diode due to the structure, which is very similar to a static-induction transistor (SIT). In addition, the gate-drain overlap is quite large, resulting in a high gate-drain capacitance, which slows down the device. The triode like output characteristic caused by the short channel requires matching of the channel region to the required blocking voltage [7]. At elevated temperatures the leakage current cannot be neglected, and the temperature coefficient of the on-resistance is relatively large. All JFET devices have a pn-junction which controls the device. This pn-junction starts to conduct at positive gate voltages of ~3V. In case of a normally-off JFET, a significantly larger gate voltage is required to fully turn-on the device, leading to a large gate current. Therefore specially designed driver circuits are needed. Also first vertical JFET devices are already available [6].

The normally-on quasi-vertical JFET is a voltage-controlled device with a lateral channel and a drain-source body diode. The device shows, like a MOSFET, an advantageous pentode-like output characteristic. The temperature coefficient of the on-resistance is lower than for a normally-off JFET. The gate-source and gate-drain capacitances of the JFET are smaller compared to the MOSFET because of the smaller overlap region between the gate and drain. The normally-on device may also require a special gate driving circuit, although many standard drivers are basically capable of driving such a device. The long-term reliability of all JFETs benefits from the absence of a gate oxide (which would be very sensitive to environmental influences, e.g. humidity), and the fact that the main functional part of the device is located in the semiconductor volume and not at an interface. In addition, the pinch-off voltage of a JFET is stable over long time-scales even at elevated operation temperatures.

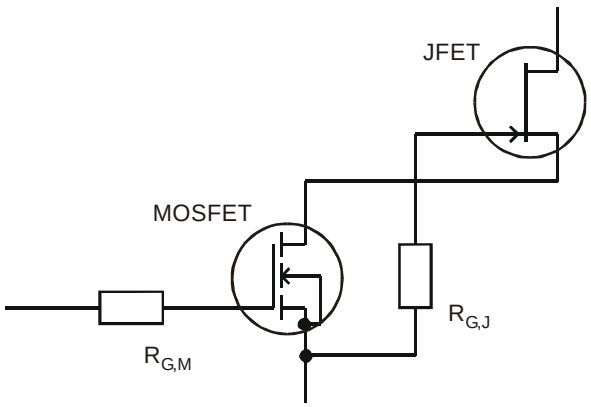

Fig. 2: Cascode switch formed by a normally-off MOSFET and a normally-on JFET

Regarding good forward conduction, low switching losses and fulfillment of all reliability requirements, the normally-on SiC JFET therefore seems to be the most promising device. Devices with a lateral channel further benefit from the presence of an inherent body diode and from more favourable output characteristics and lower leakage currents at elevated temperature [7]. However, although topologies exist which require the use of normally-on devices [10], today almost all application topologies rely on normally-off devices. Consequently, it is impossible to simply replace a normally-off device by a normally-on switch. Also most available gate driver units are not capable of delivering the required negative gate voltage to turn-off the JFET. Furthermore a driver supply voltage failure would result in a short circuit damaging the power electronic unit.

To allow for an easy replacement of common silicon power devices in today's applications, a cascode arrangement looks promising [11]. Fig. 2 gives the basic circuit of such a cascode switch. A low-voltage silicon power MOSFET drives the high-voltage silicon-carbide JFET. However, the introduction of a second switch causes additional losses and might result in instabilities under certain conditions. Occasionally also the limitation of the maximum dv/dt is from interest if a further minimization of the loop inductance in a power electronic device is not possible or if it requires too much efforts. In such cases a reduction of the dv/dt can be reached by several measures as discussed in [12], nevertheless such measures lead to increased switching losses. A properly designed cascode circuit should also help to improve the overall performance in such cases.

To ensure the reliable operation of the cascode as a power switch, the following requirements must be fulfilled:

- the turn-on- and turn-off-process must be actively controlled by the gate (controllability of dv/dt and di/dt)
- there should be little or no oscillation in the switching processes
- none of the devices should be driven into avalanche mode
- for 650 V devices, total losses must be significantly lower than competitive devices such as Superjunction-MOSFET (SJ-MOSFET)

2. THE SiC-JFET CASCODE

Fig. 3 shows the JFET structure in more detail. The JFET comprises a cell structure design, surrounded by a p^+/p^- JTE (junction termination extension) edge termination structure as used in Infineon´s SiC thinQ! MPS (merged PN Schottky) diodes. The n-doped epitaxial layer is grown on a highly-doped 4H-SiC substrate. The doping density and thickness of the epitaxial layer serving as both the drift region and the voltage sustaining region of the device depend on the required maximum blocking voltage. Due to the much larger breakdown field strength of silicon-carbide compared to silicon, the thickness of the drift region is much lower and the drift region doping much larger than in a silicon device designed for the same breakdown voltage. The p-SiC areas are realized by ion implantation of aluminum and n-SiC areas by nitrogen implantation. The activation requires a subsequent annealing step at 1700 °C. Standard polyimide is used for passivation. In order to decrease the internal distributed gate resistance and thus reduce switching losses, the ohmic contact metallization on top of the gate must be sufficiently thick.

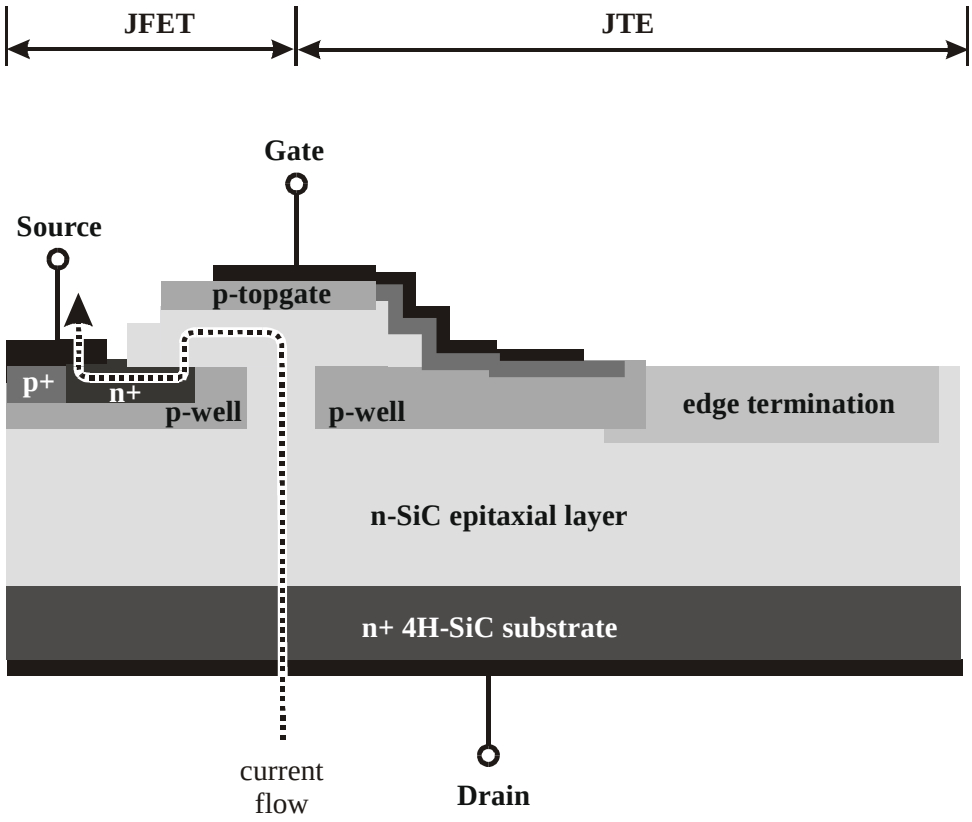

Fig. 3: Structure of the SiC-JFET including edge termination and indication of current path

The current path is indicated in fig. 3 by an arrow. The channel is depleted if a negative voltage is applied to the top gate. Note that channel depletion is not only caused by the top gate but also by the p-well connected to source acting as a back gate. The channel will be completely depleted if the pinch-off voltage is reached. Further increasing the negative gate voltage will finally lead to punch-through. It is advantageous if the window between the pinch-off voltage and the punch-through voltage is large. For the devices used in this investigation, the pinch-off voltage is centered at V_{PI} = -13.5 V while the punch-through voltage is found at V_{PT} = -24 V.

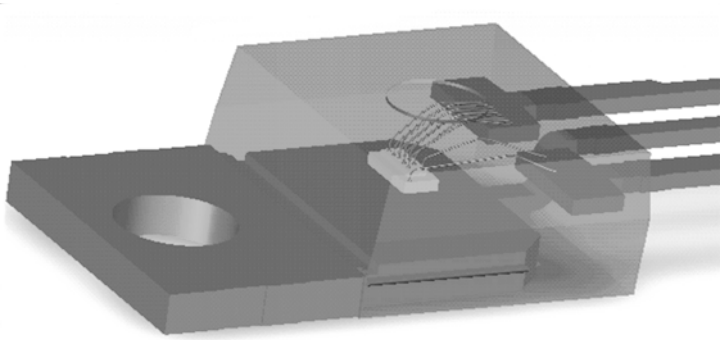

Fig. 4: Realization of a complete cascode as a chip-on-chip solution in a TO-220 package

To realize the cascode, the first SiC-JFET demonstrators were available having a blocking voltage of ca. 1000 V. To complete the cascode, 30V OptiMOS™3 devices were used. The cascode can be built using separate discretes or can be integrated into a single TO-220 package employing a chip-on-chip technique. Here the smaller MOSFET resides on the source metallization of the JFET. Fig. 4 illustrates the sample construction. The on-resistance of the investigated cascode is $R_{(DS)ON}$ = 75mΩ. Here the MOSFET is responsible for about 15% of the overall on-resistance.

3. CONTROLLABILITY ANALYSIS

A typical application of a high-voltage power MOSFET is found in power factor correction (PFC) stages of power supplies. Consequently, for the stability analysis a simplified equivalent circuit of a PFC stage was used as shown in Fig. 5. The cascode itself is modeled by the elements within the dotted square. All measurements were done in a commonly available 600 W Boost PFC stage following the basic schematic as shown in Fig. 5.

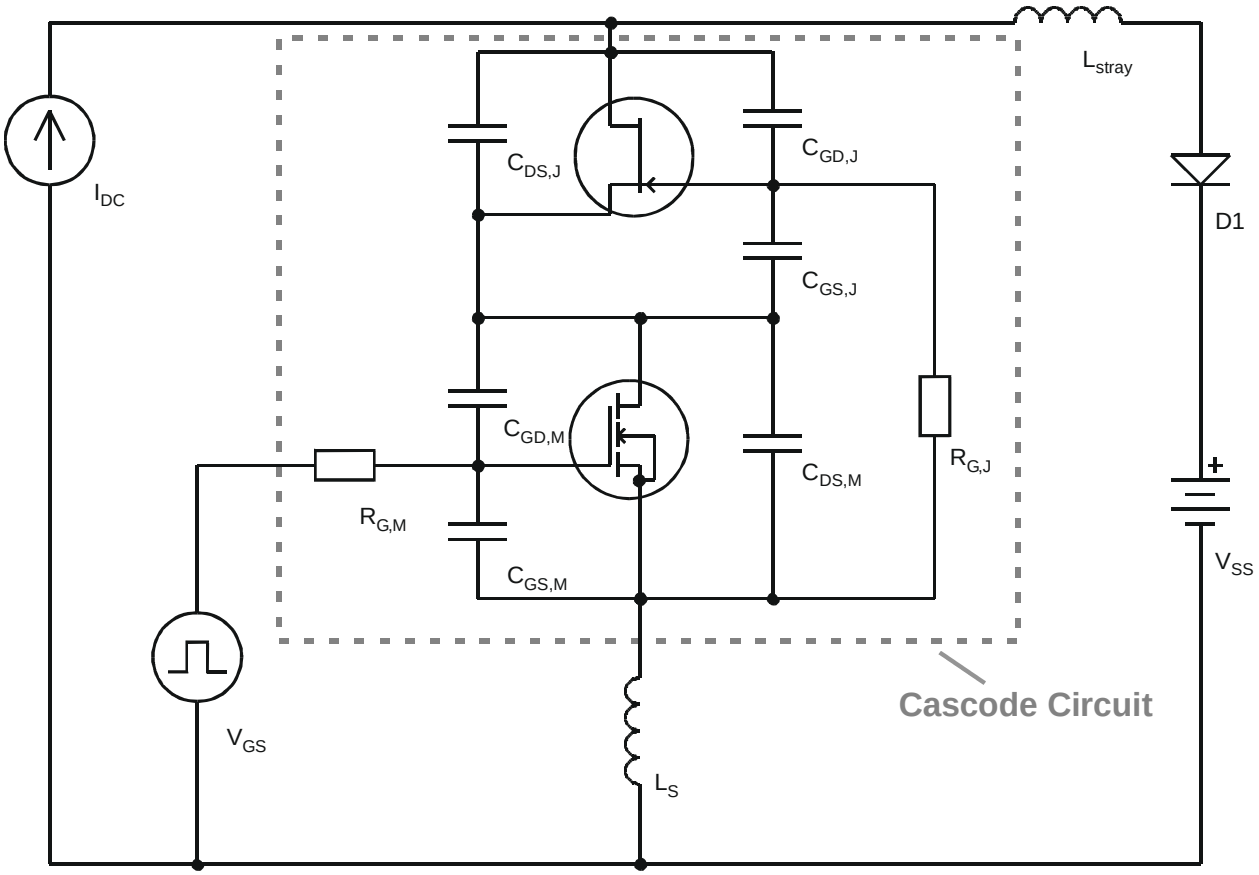

Fig. 5: Simplified equivalent circuit of a simple PFC stage using a cascode switch arrangement

3.1 Turn-On Process

Fig. 6 illustrates the turn-on process of the cascode arrangement. Before the cascode is turned on, there is a current driven by the current-source I_{DC} through L_{stray} and D1 (Fig. 6, circuit 0). During turn-on the gate-source capacitance $C_{GS,M}$ is charged via $R_{G,M}$ until the plateau voltage $V_{PLAT,M}$ is reached (Fig. 6, circuit I). Now the MOSFET channel becomes conductive and a displacement current flows through $C_{GD,M}$ (Fig. 6, circuit II). Since this lowers the drain-to-source voltage of the MOSFET $V_{DS,M}$, there must be a displacement current through $C_{DS,M}$ as well (Fig. 6, circuit III). In parallel to $C_{DS,M}$, there is also the gate-source capacitance $C_{GS,J}$ of the JFET (Fig. 6, circuit IV). This additional current flow is delayed by the JFET gate resistor $R_{G,J}$. The rising gate voltage at the JFET allows a current flow through the JFET (Fig. 6, circuit V). As in case of the MOSFET, the drain-source voltage of the JFET $V_{DS,J}$ is lowered and a displacement current flows through $C_{DS,J}$ (Fig. 6, circuit VI).

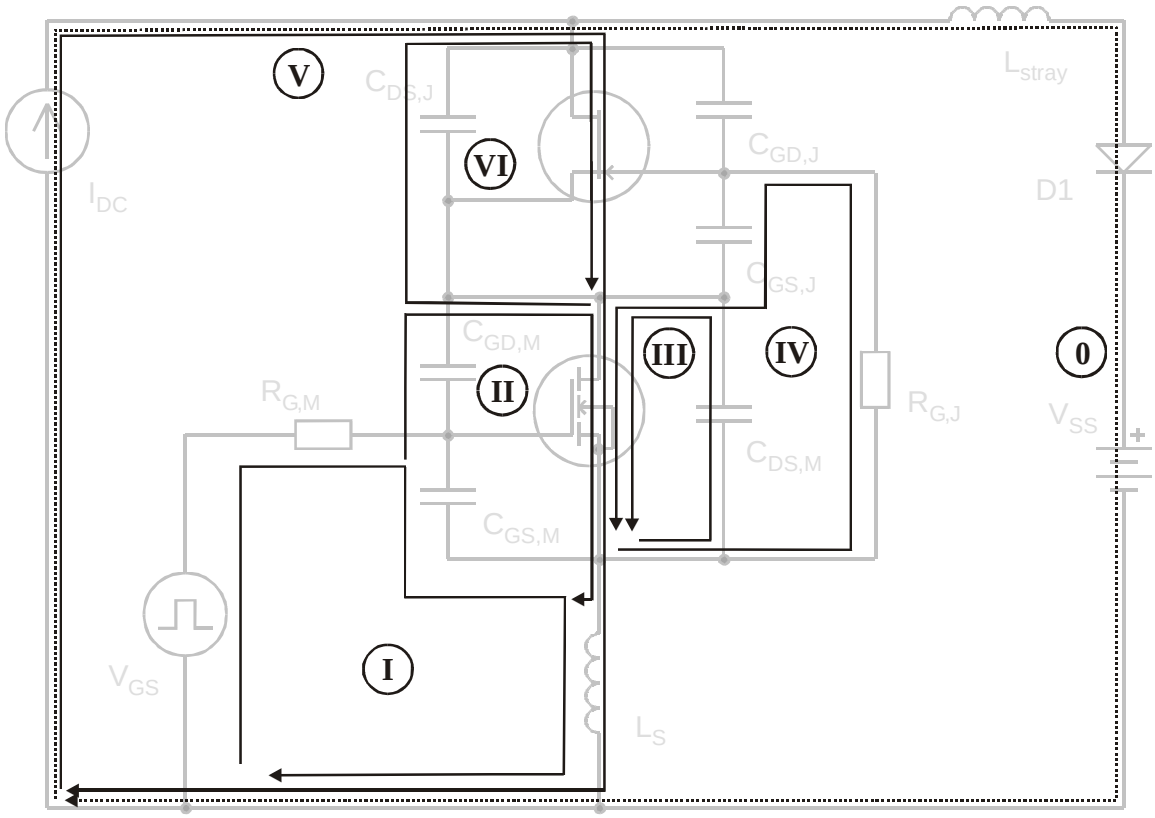

Fig. 6: Basic turn-on process of the cascode arrangement

In normal cases (except for very fast switching or very low load current), an equilibrium is established that leads to a roughly constant di/dt and V_{DS} across the complete cascode. To keep full control of the turn-on process and allow for a limitation of the di/dt and dv/dt, the MOSFET must operate in linear mode until the JFET is fully turned-on. In most cases the stray inductance L_S at the source of the cascode limits the di/dt and provides the required stability:

$$L_S > \lambda \tag{1},$$

with:

$$\lambda = \frac{C_{GD,M}\ R_{G,M}}{g_{fsJ}} \tag{2},$$

g_{fsJ} being the forward transconductance of the JFET.
However, the MOSFET might reach the end of the plateau phase before the JFET can support the entire current. In this case, there is no longer any control connection between the JFET and the MOSFET and both devices are charged independently. Now the gate resistor of the MOSFET $R_{G,M}$ has no influence on the rest of the switching process and the rise of the JFET gate voltage $V_{GS,J}$ is now controlled by the JFET gate resistance $R_{G,J}$ and the JFET input capacitance $C_{GS,J} + C_{GD,J}$.
Under this condition the controllability is only achieved if the following condition is fulfilled:

$$\frac{Q_{GD,M} \cdot R_{G,M}}{\left(V_{GS,M} - V_{PLAT,M}\right)\left(1 - \frac{L_S}{\lambda}\right)} \geq \frac{I_{DC}\left(L_S + \lambda\right)}{V_G - V_{plat}} + C_{GS,J} \cdot R_{G,J} \tag{3}.$$

Hence the MOSFET switching time must be at least equal to or larger than the time needed for the current to rise and the delay time between the MOSFET and JFET.

If di/dt during turn-on is not self-limited by the source inductance L_S, a limitation can be obtained in practice by a reasonably large value of the MOSFET gate resistor $R_{G,M}$. Also, for optimum controllability and minimum switching losses a small JFET gate resistor is required ($R_{G,J} \rightarrow 0$).

3.2 Turn-Off Process

Keeping complete control of the turn-off process of the cascade, which requires the active limitation of the resulting di/dt and dv/dt, is more difficult than in the case of the turn-on process. Before the cascode is turned off, the current is driven through the cascode by the current source I_{DC} (Fig. 7, circuit 0). At the beginning of the turn-off process the gate of the MOSFET is discharged via the gate resistor $R_{G,M}$ until the plateau voltage is reached (Fig. 7, circuit I). Now the voltage across the MOSFET starts to rise. The capacitances $C_{GD,M}$ (Fig. 7, circuit II) and $C_{DS,M}$ (Fig. 7, circuit III) are charged by the channel current of the JFET. Both capacitances form the output capacitance of the MOSFET. At the same time the rising voltage across the MOSFET causes a displacement current through $C_{GS,J}$ (Fig. 7, circuit IV) and $C_{GD,J}$ (Fig. 7, circuit V). This current flow leads to a reduction of the gate-source-voltage of the JFET. All these displacement currents reduce the channel current of the MOSFET; additionally the displacement current through $C_{GD,J}$ also reduces the channel current of the JFET (Fig. 7, circuit VI). Of course it is basically the load current which causes the recharging of the capacitances. Due to the decrease of the current through the cascode, the current starts to flow again through L_{stray} and D1 (Fig. 7, circuit VII).

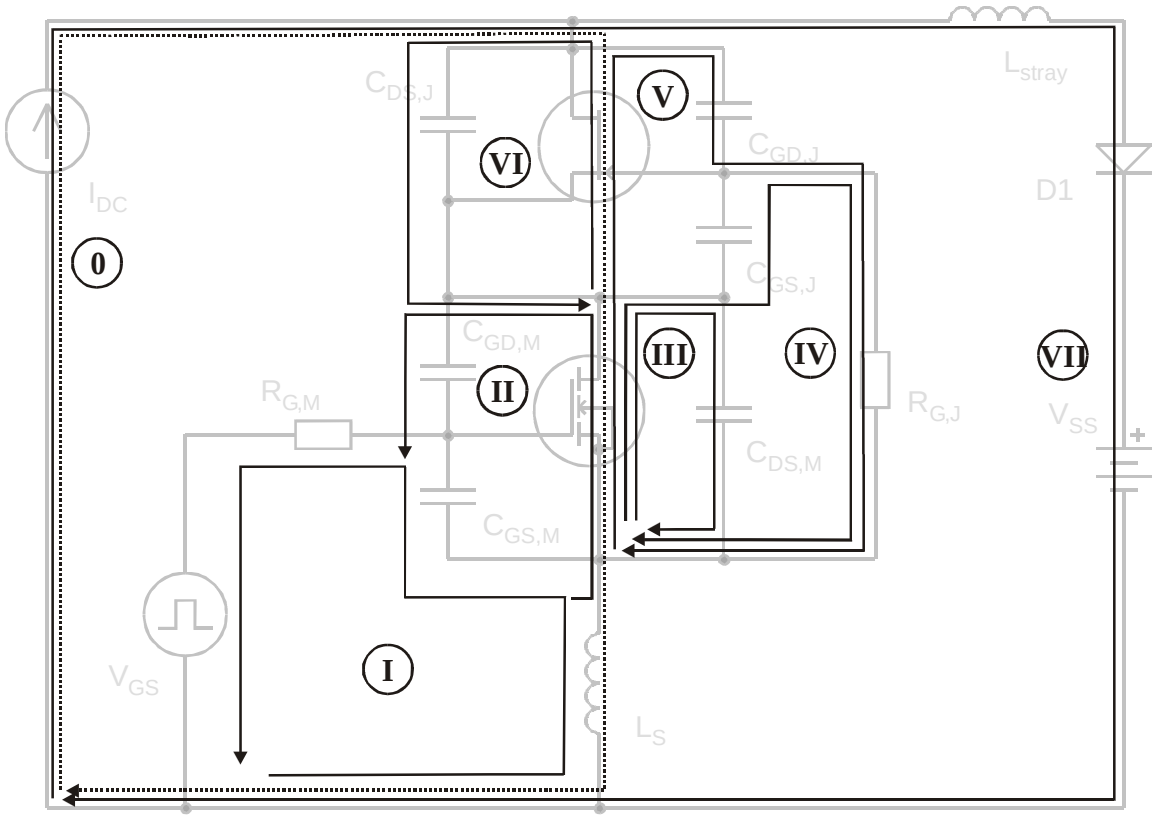

Fig. 7: Basic turn-off process of the cascode arrangement

In contrast to the turn-on process there are now more scenarios which might occur during the continuation of the turn-off process, most of which should be avoided to keep control.
If the MOSFET chosen is too big with respect to the load current, the MOSFET displacement currents through $C_{DS,M}$ and $C_{GD,M}$ will be larger than the respective displacement current through $C_{DS,J}$ and $C_{GD,J}$ of the JFET. Under this condition the channel current through the MOSFET disappears and the MOSFET leaves the linear mode. In order to allow the JFET current to flow, the $V_{GS,J}$ is clamped as the JFET is still in linear mode. The voltage rise is now only controlled by the load current. If the cascode is switched too fast and/or the stray inductance is too large, the JFET can be driven into avalanche. If a gate resistor for the JFET is present (which is considered to be the normal case), the voltage across the MOSFET will be higher than $V_{GS,J}$ and the MOSFET might also be driven into avalanche.
If, on the other hand, the MOSFET size is chosen correctly, the load current is used to charge the output capacitance of both devices ($C_{GD,M} + C_{DS,M} + C_{GS,J} + C_{GD,J}$). The MOSFET is operated in the linear region while the JFET is still fully on. The gate-source voltage $V_{GS,J}$ of the JFET decreases till the JFET reaches the linear region. Now the $C_{DS,J}$ is charged and the channel current of the JFET is reduced. A further reduction of the JFET channel current now needs a reduction of the $V_{GS,J}$ which is controlled by the voltage $V_{DS,M}$ across the MOSFET which in turn is controlled by the gate resistance $R_{G,M}$. Even if a JFET gate resistor $R_{G,J}$ is present, the voltages at the MOSFET and JFET will rise concurrently, while the dv/dt at the cascode will increase at least till the outer voltage V_{SS} is reached. The dv/dt at the MOSFET stays roughly constant.
Once the voltage across the cascode is larger than the sum of the outer voltage V_{SS} and the voltage drop across the freewheeling diode D1 (due to the presence of the stray inductance), the current through the freewheeling diode starts to rise which makes the cascode current fall. The voltage increase at the cascode will finally stop if the entire current is taken over by the freewheeling diode.
For high currents and large di/dt with respect to the present value of the stray inductance, the voltage increase might exceed the breakdown voltage of either the JFET or the MOSFET. In both cases controllability is lost. The only way to avoid this scenario is to choose a reasonably high gate resistance $R_{G,M}$.
As the JFET channel current finally disappears, the $V_{GS,J}$ of the JFET falls below the pinch-off voltage V_{PI} and can even reach the punch-through voltage V_{PT} of the JFET's gate-source structure. To avoid avalanche of the MOSFET, the breakdown voltage of the MOSFET should be somewhat larger than the pinch-off voltage of the JFET.

In summary, complete control of the turn-off process and therefore an active control of the resulting dv/dt and di/dt is only possible if the MOSFET stays in linear mode over the complete turn-off process.
It is also essential to keep the offset between the drain-source-voltage of the MOSFET and the gate-source-voltage of the JFET as small as possible. This offset is mainly caused by the voltage drop across the JFET gate resistor, and delays the turn-off of the JFET. If this delay becomes too long, the MOSFET enters avalanche mode. Once this point is reached, the controllability of the cascode via the gate of the MOSFET is lost and the remaining part of the turn-off process is governed by the load current. High di/dt and dv/dt as well as oscillations are likely consequences. To keep control of the turn-off process, the following condition must be met:

$$\frac{C_{GS,J}\Big|_{V_{DS}=V_{DSS}} R_{G,J}}{C_{GD,M}\Big|_{V_{DS}=0} R_{G,M}} V_{plat,M} < V_{BR,M} + V_{PI} \qquad (4).$$

A violation of the condition given by Eqn. 4 will result in losing control. Likely consequences are driving either the MOSFET or the JFET into avalanche mode, the occurrence of large di/dt and dv/dt, and the triggering of oscillations.

3.3 Avoidance of Oscillations

Oscillations may occur during the cascode switching processes as shown in Fig. 8. They are caused by the capacitive elements of the cascode arrangements, which form resonant circuits with unavoidable inductive elements in the complete circuit. In particular, the turn-off process is critical even if the controllability condition according to Eqn. 4 is met.

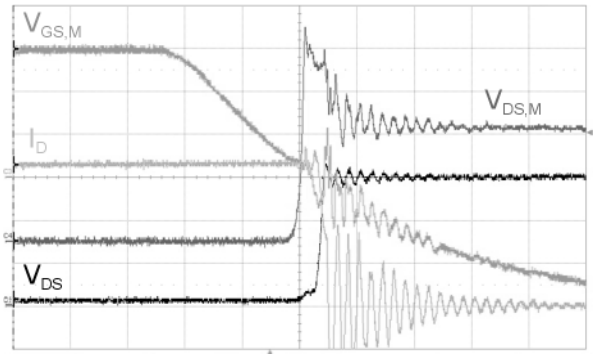

Fig. 8: Measured oscillations during the turn-off of a cascode switch formed by a 1000 V SiC JFET and a 30 V n-channel MOSFET
(time base: 50 ns/div, $V_{GS,M}$: 5 V/div, $V_{DS,M}$: 10 V/div, V_{DS}: 100 V/div, I_D: 10A/div)

Oscillations may start during the switching process since at that time all the necessary ingredients are present – capacitances, at least one active element and an inductance. Firstly, both devices work in linear mode simultaneously during turn-off. This might cause an amplification of oscillations in the case of a positive feedback to the gate of the MOSFET. Secondly, most capacitances decrease during the turn-off process due to an increase of the width of the space-charge region. This results in reduced attenuation of any oscillations which appear. Thirdly, there is always a stray inductance present. The oscillations are triggered by the common voltage overshoot across the cascode during turn-off.
To find conditions for the avoidance of oscillations, the circuit can be described by an appropriate differential equation. The capacitances $C_{GD,J}$, $C_{GD,M}$ and $C_{GS,M}$ (c.f Fig. 5) were cancelled for reasons of simplicity and since they are rather small which leads to Eqn. 5.

$$L_{stray}R_{G,J}C_{DS,M}\frac{d^4i}{dt^4} + L_{stray}\left(\frac{C_{DS,M}}{C_{GS,J}}+1\right)\frac{d^3i}{dt^3} + R_{G,J}\left(\frac{C_{DS,M}}{C_{DS,J}}+1\right)\frac{d^2i}{dt^2} + \frac{1}{C_{DS,J}}\left(\frac{C_{DS,M}}{C_{GS,J}}+\frac{C_{DS,J}}{C_{GS,J}}+1\right)\frac{di}{dt} + \frac{g_{fs,J}}{C_{GS,J}C_{DS,J}} = 0 \quad (5).$$

Oscillations are attenuated as long as the real parts of the zeros of the characteristic polynomial are negative, which is desirable It is clear that completely cancelling the JFET gate resistor results in the lowest switching losses. On the other hand the JFET gate resistor acts as the most effective damping element of the oscillations and thus cannot be eliminated. Another damping element is, to some extent, the MOSFET gate resistor $R_{G,M}$. A larger value helps, but also increases switching losses. Finally a lower value of the stray inductance L_{stray} also supports the avoidance of unwanted oscillations.

3.4 Verification

To verify the results of the controllability analysis, the combination of a 30 V MOSFET and a 600 V SiC JFET was investigated by circuit simulation. The circuit used is the PFC stage already shown in Fig. 5 having a stray inductance L_{stray} = 40 nH and a source inductance L_S = 4 nH. An appropriate SPICE model for the 600 V SiC JFET was provided based on the results of extensive 2D device simulation work. Here, the simulations included forward-, output- and reverse-characteristics for the JFET and the bodydiode as well as the small-signal capacitances in dependence on the drain-source-voltage and the gatecharge characteristics for varying drain-source-voltages.

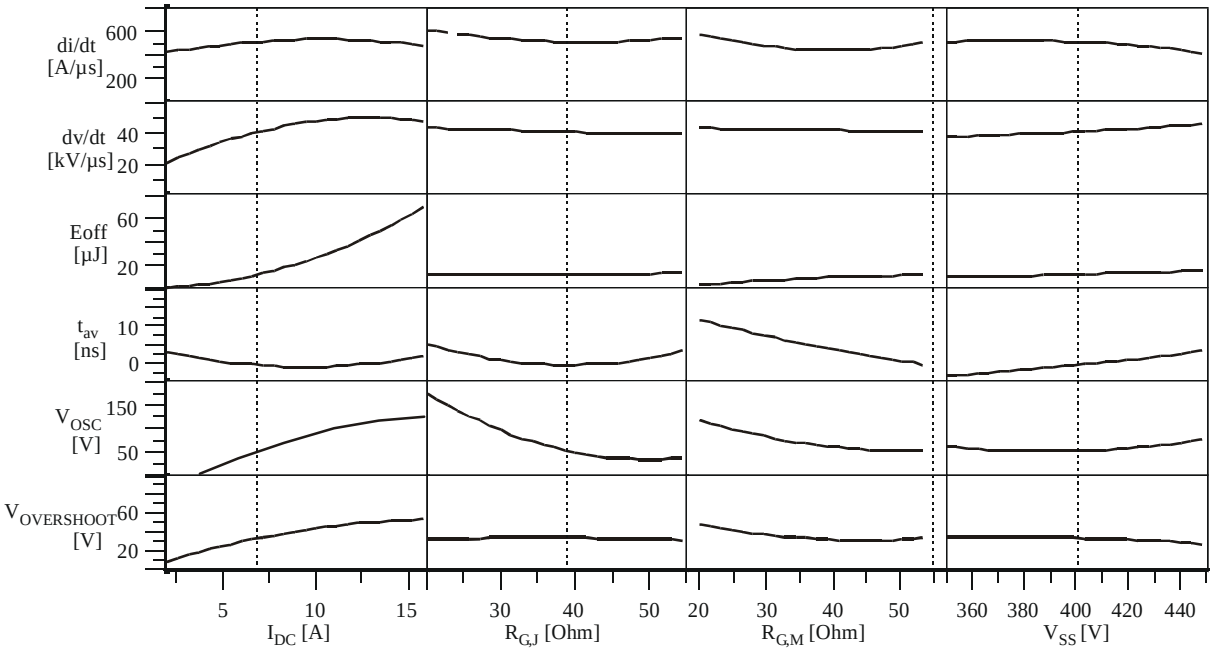

Fig. 9: Model for the turn-off analysis of a 600 V cascode switch based on a simulation DoE

The investigation shown in this work was done using four input parameters: the MOSFET gate resistor $R_{G,M}$, the JFET gate resistor $R_{G,J}$, the switched current I_{DC} and the supply voltage VSS. These input parameters have been varied to form a fully squared-type DoE (Design of Experiments). Fig. 9 shows the corresponding model for the turn-off process of the cascode as derived from the full set of simulations. Chosen output parameters are the di/dt and dv/dt, turn-off losses E_{off}, the amplitude of superimposed oscillations V_{OSC} on the voltage across the cascode, the maximum overvoltage peak $V_{OVERSHOOT}$ superimposed on the voltage across the cascode and the time tav for the MOSFET being in avalanche mode.
With the chosen parameters of V_{SS} = 400 V, $R_{G,J}$ = 39 Ω and $R_{G,M}$ = 55 Ω, avalanching of the MOSFET and the occurrence of self-amplifying oscillations are safely prevented over the whole current range of interest. Thus these two values of the gate resistors allow safe operation of this cascode arrangement. A crosscheck is done by using these values first in Eqn. 1 for turn-on:

$$
\begin{aligned}
&L_S > \lambda \\
&\lambda = \frac{C_{GD,M}\, R_{G,M}}{g_{fs,J}} = \frac{60\text{pF}\ 55\Omega}{3\text{S}} = 1.1\text{nH} \\
&L_S = 4\text{nH} \\
&4\text{nH} > 1.1\text{nH}
\end{aligned}
\tag{6},
$$

and again in Eqn. 4 for turn-off:

$$
\begin{aligned}
\frac{C_{GS,J}\Big|_{V_{DS}=V_{DSS}}\ R_{G,J}}{C_{GD,M}\Big|_{V_{DS}=0}\ R_{G,M}}\, V_{plat,M} &< V_{BR,M} + V_{PI} \\
\frac{100\text{pF}\ 39\Omega}{60\text{pF}\ 55\Omega}\, 3.4\text{V} &< 40\text{V} - 14\text{V} \\
4.02\text{V} &< 26\text{V}
\end{aligned}
\tag{7}.
$$

Obviously the values found by the simulation DoE fulfill the analytically derived conditions.

4. PERFORMANCE ANALYSIS

4.1 Performance of cascode solution in comparison to Superjunction-MOSFET

To characterize the performance of the cascode, again the previously shown PFC stage of a power supply was chosen. Here the operating voltage is usually in the range of 400 V, which requires devices with a blocking voltage of 600 V. However, the first SiC-JFET demonstrators had a significantly higher blocking voltage of ca. 1000 V but a larger $R_{DS(ON)}$ than would be obtainable with a fully optimized device for this voltage class. A cascode using these JFETs and 30 V n-channel MOSFETs was assembled and measured.

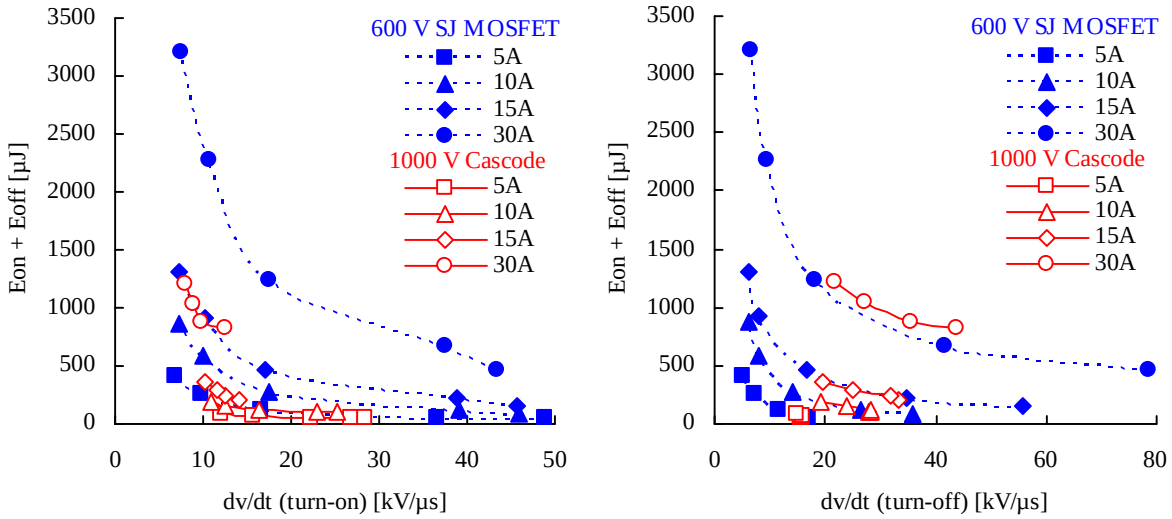

Fig. 10: Measured losses vs. dv/dt for a 1000 V SiC JFET cascode and a 600 V SJ MOSFET

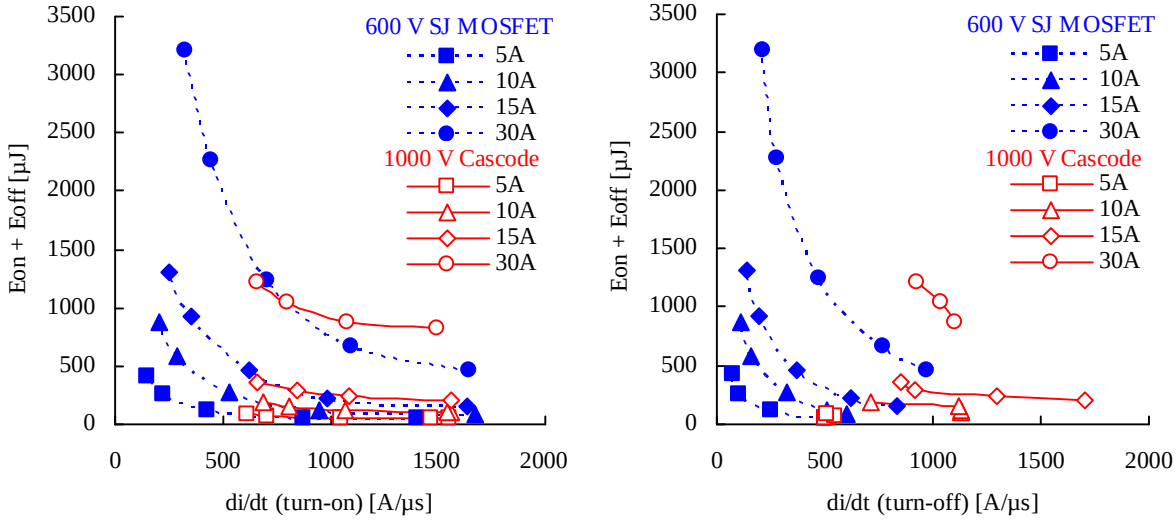

Fig. 11: Measured losses vs. di/dt for a 1000 V SiC JFET cascode and a 600 V SJ MOSFET

Fig. 10 shows the dependence of the measured losses on the maximum dv/dt during turn-on and turn-off compared with a 600 V Superjunction-MOSFET (SJ-MOSFET) [13]. Both devices had the same on-resistance. Fig. 11 gives the comparison of measured losses as a function of the maximum di/dt. Although the cascode circuit has a much higher breakdown voltage it outperforms the SJ-MOSFET. Both di/dt and dv/dt can be controlled, although the measured values are larger than in case of the SJ-MOSFET.

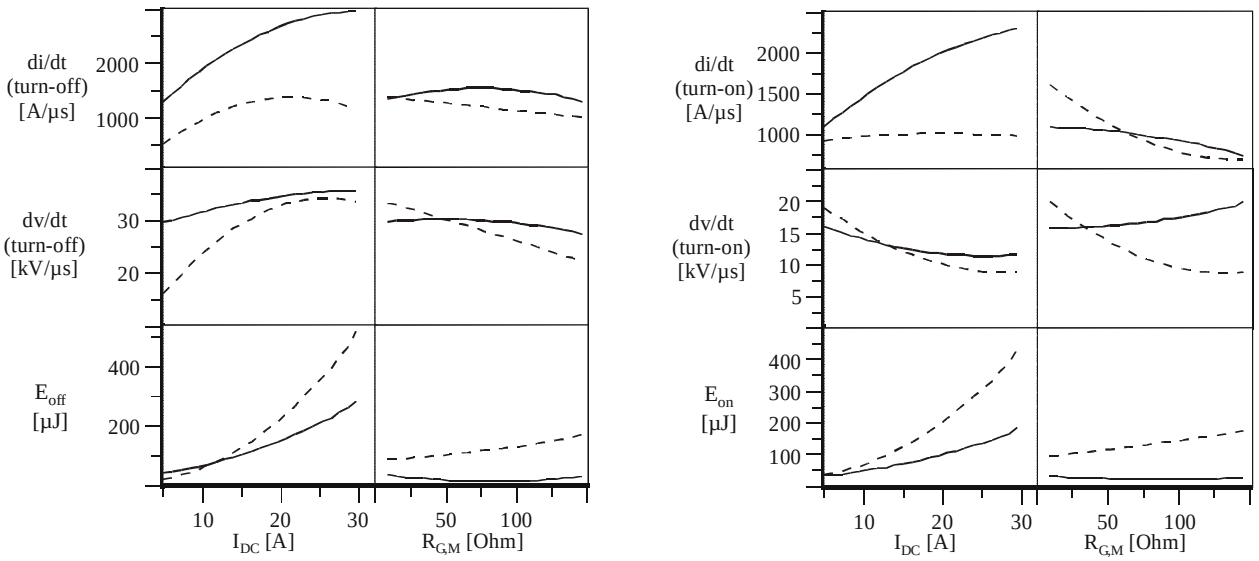

Fig. 12: Comparison of measured (dotted lines) and simulated (straight lines) values for a cascode using a SiC JFET

These measurements were later compared with SPICE simulations of these devices [14]. The comparison allows the estimation of deviations between measurements and simulations. Fig. 12 compares the dependencies of the turn-on and the turn-off process. It can be seen that in general the simulations give lower losses and larger dv/dt and di/dt. This fact relates to the simplifications introduced in the simulation circuit. The circuit does not include all of the parasitic elements responsible for slowing down the switching processes during measurements.

To allow for an analysis of the behavior of a real 600 V cascode, a SPICE model for a 600 V SiC JFET completely based on 2D device simulations is used. By means of circuit simulations the behavior of the 600 V cascode was compared to that of the 600 V SJ MOSFET. The values of both gate resistors were chosen in a way that all previously derived controllability conditions for safe switching are met. Fig. 13 shows the simulated comparison of the total switching losses as a function of dv/dt, while fig. 14 gives the results as a function of di/dt.

The measured setup using the first SiC JFET demonstrators already showed advantages in the performance compared against a 600 V SJ MOSFET, but oscillations were sometimes observed in the measurements as well as in the simulations, especially at low currents. In contrast, the simulated setup with the 600 V SiC JFET showed a further improvement in performance compared to the SJ MOSFET. In the simulated parameter range, no oscillations were observed.

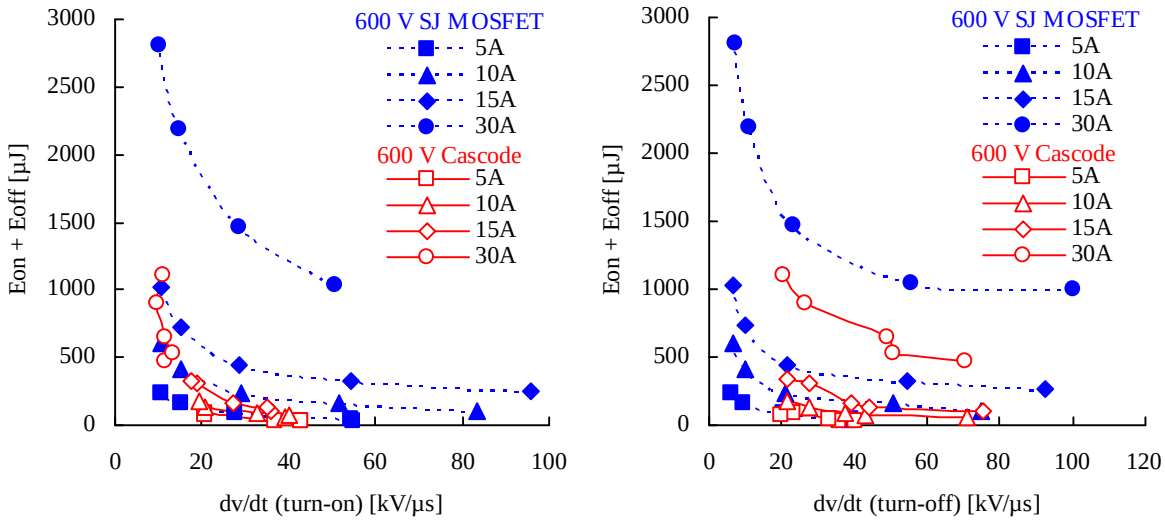

Fig. 13: Simulated losses vs. dv/dt for a 600 V SiC JFET cascode and a 600 V SJ MOSFET

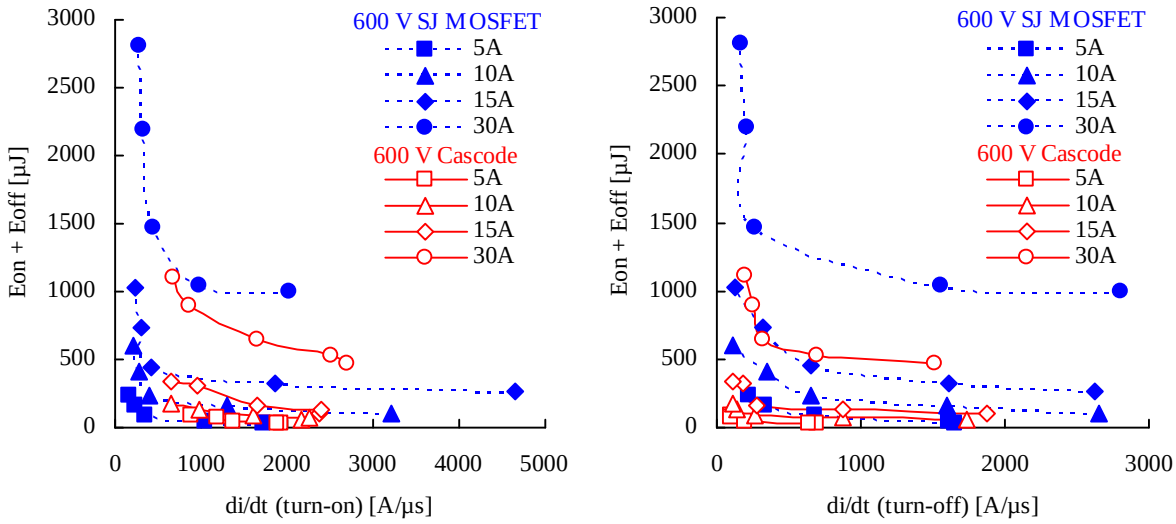

Fig. 14: Simulated losses vs. di/dt for a 600 V SiC JFET cascode and a 600 V SJ MOSFET

4.2. The direct-driven JFET as an alternative solution

The cascode outperforms available silicon-based SJ devices, however it is clear that a stand-alone JFET would behave significantly better due to two main reasons.

Firstly, the cascode has a much larger output capacitance than a single JFET due to the capacitances of the low-voltage MOSFET as depicted in Fig. 15. The output capacitance of the cascode behaves like a JFET, but with a significant charge offset. This larger output charge is directly responsible for an increase of the turn-on losses in an inverter topology. Fig. 16 gives a

comparison of the turn-on waveforms for a cascode switch and a stand-alone JFET in an identical environment. The cascode shows a noticeably higher reverse-recovery-like current peak, which triggers oscillations in the circuit. In case of the stand-alone JFET the waveform has a lower current peak and looks smooth. Regarding the turn-on losses the cascode circuit consumes 440 µJ while the stand-alone JFET needs only 160 µJ. As a consequence for a cascode arrangement, the MOSFET size must be carefully chosen to find an optimum between the conduction losses and switching losses of the cascode.

Secondly, the cascode switching speed must be limited to reliably control the maximum di/dt and dv/dt. As shown before in the controllability analysis, this is mainly achieved using relatively large gate resistors of both the MOSFET and the JFET. Unfortunately, this also significantly lowers the switching speed and therefore causes larger switching losses than in the case of a stand-alone JFET.

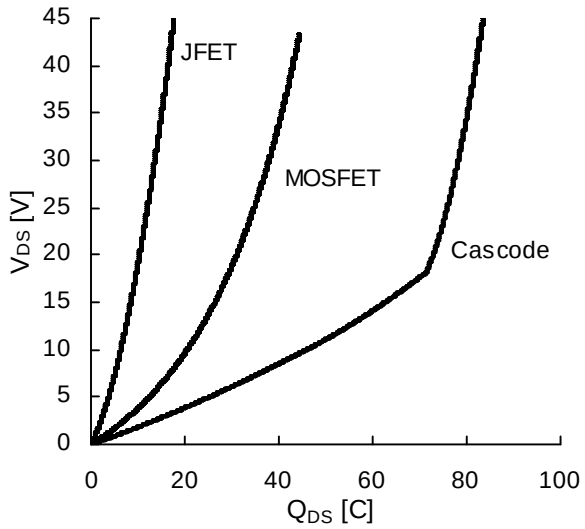

Fig. 15: Gate-drain-charge at a constant current of 1 mA (device in off-state)

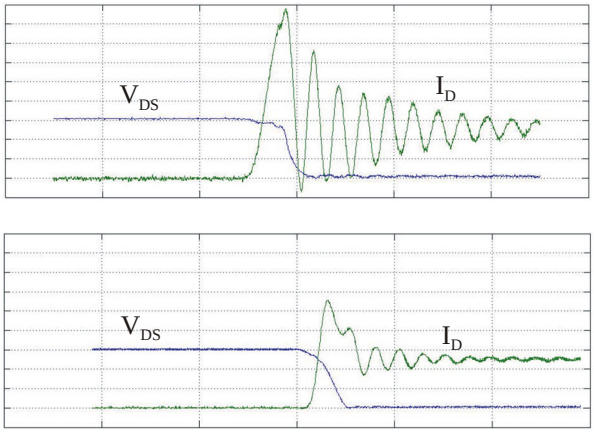

Fig. 16: Turn-on waveforms of a cascode switch (top) and a stand-alone JFET (bottom) in the same inverter circuit (time base: 100 ns/div, I_D: 4 A/div, V_{DS}: 200 V/div)

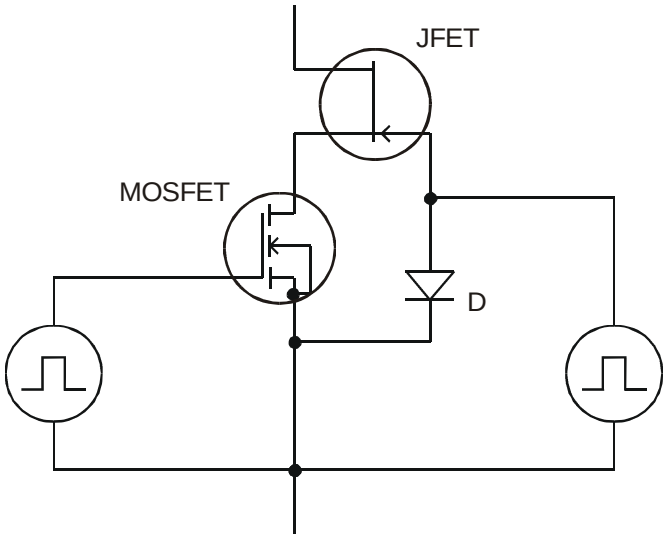

Fig. 17: Modified cascode circuit with separate driver units for MOSFET and JFET

Therefore an alternative solution called a “direct-driven JFET” is proposed, as shown in Fig. 17. Here a second driver for the MOSFET guarantees that the MOSFET is always turned-on as long as the driver power supply is present [15,16]. A diode ensures that during startup, or in case of a gate driver failure, the classic cascode solution comes into being and serves as a normally-off device. In normal operation, the circuit acts like a stand-alone JFET and avoids the discussed limitations of a classic cascode circuit. The additional driver can easily be integrated into a single driver IC. Fig. 18 shows the block diagram of a typical application circuit using the dedicated driver unit 1EDI30J12Cx which is currently being developed.

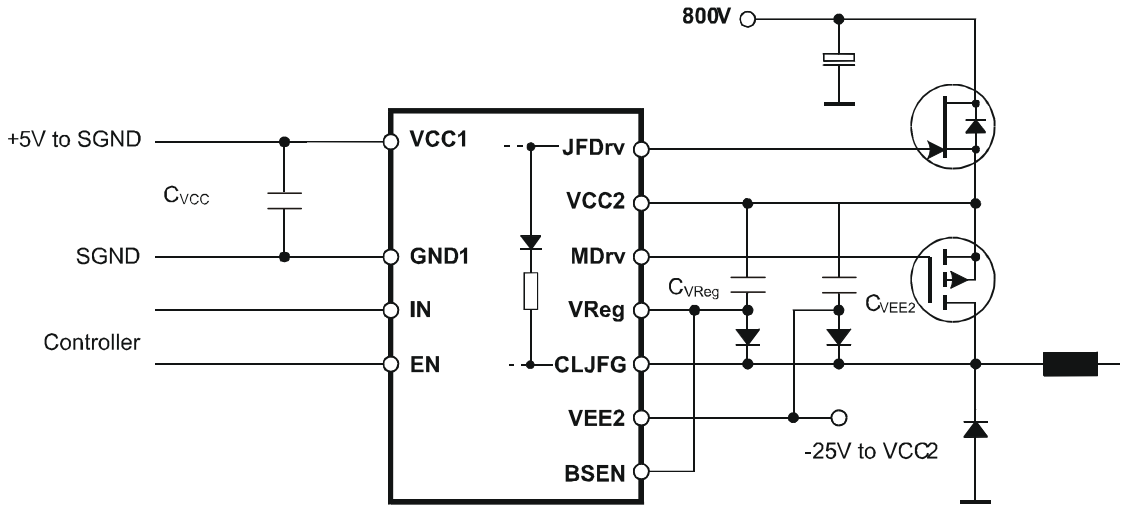

Fig. 18: Block diagram of typical application circuit using the proposed driver IC

For application testing, the JFET and MOSFET in a direct-driven configuration was implemented in a half-bridge topology using a state-of-the-art power module assembly. Fig. 19 shows the turn-on and turn-off switching with a DC voltage of V_{SS} = 600 V and a load current of I_{DC} = 30 A. Here, three 100 mΩ direct-driven JFETs were paralleled without external gate resistors. With an appropriate driver, this circuit acts like a conventional normally-off system from a customer point of view. The extracted switching energies are E_{on} = 460 µJ for turn-on and E_{off} = 213 µJ for turn-off. This translates to a reduction of switching losses by a factor of 10 compared to a commercially available 1200 V Si IGBT with a Si freewheeling diode using a trench cell and field stop design [17], which has E_{on} = 4000 µJ for turn-on and E_{off} = 2700 µJ for turn-off under the same conditions; I_{DC} = 30 A, V_{SS} = 600 V and T_j = 125 °C.

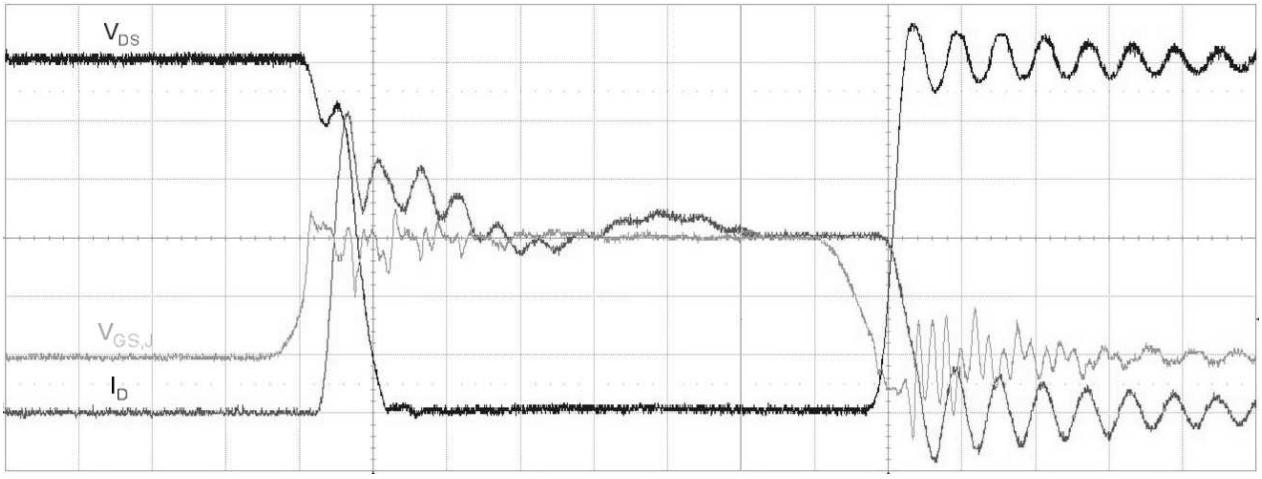

Fig. 19: Switching waveforms for paralleled direct-driven SiC-JFET (3x 100 mΩ) at a load current of I_{DC} = 30 A and a DC voltage of V_{SS} = 600 V without external gate resistor.
(time base: 50 ns/div, gate voltage: 10 V/div, drain voltage: 100 V/div, drain current: 10 A/div)

5. CONCLUSION

Recently a number of active wide band-gap power devices have been announced. The normally-on JFET seems to be the most promising device in terms of performance and reliability although normally-on devices are less suited for power-electronic applications today.
A cascode arrangement offers the possibility of realizing normally-off power devices using such SiC JFETs. In this work, the stability and performance of such a cascode approach formed by a normally-on SiC JFET having a high blocking voltage and a normally-off silicon MOSFET having a low blocking voltage is analyzed. Conditions are derived that guarantee full controllability of the cascode switch and that attenuate possible oscillations. Although such a cascode arrangement outperforms available silicon power devices, the performance suffers from additional losses introduced by the MOSFET. An alternative solution, the direct-driven JFET, is proposed offering the full performance of a SiC JFET device. Using a specially-designed driver IC, the direct-driven SiC JFET is as easy to use as any normally-off power device.

REFERENCES

[1] N. Kaminski: State-of-the-art and Future of Wide Band-gap devices, Proc. EPE, Barcelona, 2009

[2] M. Domeij, A. Lindgren, C. Zaring, A.O. Konstantinov, J.-O. Svedberg, K. Gumaelius, I.Keri, H. Grenell, M. Östling, M. Reimark: 1200V 6A SiC BJTs with very low V_{CESAT} and fast switching, Proc. PCIM, Nuernberg, 2010

[3] A. Agarwal and S.-H. Ryu: Status of SiC Power Devices and Manufacturing Issues, Proc. CS MANTECH Conference, pp. 215-218, Vancouver, 2006,

[4] Cree Inc.: CMF20120D-Silicon Carbide Power MOSFET 1200V 80mΩ, datasheet, http://www.cree.com

[5] R. Kelley, G. Stewart, A. Ritenour, V. Bondarenko, D.C. Sheridan: 1700V Enhancement-mode SiC VJFET for High Voltage Auxiliary Flyback SMPS, Proc. PCIM, Nuernberg, 2010

[6] Semisouth Inc.: Power Semiconductor products,
http://www.semisouth.com/products/products.html

[7] M. Treu, R. Rupp, P. Blaschitz, K. Rüschenschmidt, T. Sekinger, P. Friedrichs, R. Elpelt, D. Peters: Strategic considerations for unipolar SiC switch options: JFET vs. MOSFET, Proc. IAS, New Orleans, 2007

[8] H. Lendenmann, J.P. Bergmann, F. Dahlquist, C. Hallin: Degradation in SiC bipolar devices: source and consequence of electrically active dislocations in SiC, Proc. Materials Science Forum, Vol. 433-436, pp.901-906, 2003

[9] M. Treu, R. Rupp, G. Sölkner: Reliability of SiC Power Devices and its Influence on their Commercialization – Review, Status and Remaining Issues, Proc. IRPS, Anaheim, 2010

[10] M.H.Rashid: *Power Electronics – Circuits, Devices and Applications*, Pearson Education Inc., 2004

[11] B.J. Baliga, M.S. Adler: Composite Circuit for Power Semiconductor Switching. European Patent EP 0 063 749 B1, 1982

[12] D. Aggeler, J. Biela and J.W. Kolar: Controllable dv/dt Behaviour of the SiC MOSFET/JFET Cascode An Alternative Hard Commutated Switch for Telecom Applications, Proc. APEC, Palm Springs, 2010

[13] Infineon Technologies AG: IPW60R075CP – CoolMOS Power Transistor, datasheet, http://www.infineon.com

[14] SIMetrix Technologies Ltd.: SIMetrix – SPICE and Mixed Mode Simulation, User's Manual, 2010

[15] A. Melkonyan: *High Efficiency Power Supply using new SiC Devices*, PhD thesis, University of Kassel, 2006

[16] D. Domes, X. Zhang: CASCODE LIGHT – normally-on JFET stand alone performance in a normally-off Cascode circuit. Proc. PCIM, Nuernberg, 2010

[17] Infineon Technologies AG: FP35R12KT IGBT module, datasheet, http://www.infineon.com