The 1200V Direct-Driven SiC JFET power switch

Ralf Siemieniec, Uwe Kirchner
INFINEON TECHNOLOGIES AUSTRIA AG
Siemensstrasse 2
A-9500 Villach, Austria
Tel. +43 51777 6876
Fax: +43 4242 3020 6876
E-Mail: ralf.siemieniec@infineon.com
URL: http://www.infineon.com

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Abstract

Wide band-gap semiconductors are most attractive as materials for power devices due to low losses, improved temperature capability and high thermal conductivity. Although silicon carbide Schottky diodes have been commercially available for years, an active wide band-gap switch has still been missing. In this work, the 1200 V SiC JFET is introduced as commercially available SiC power switch. The JFET offers an excellent performance while being a normally-on device. As an alternative to get a normally-off behavior, the direct-driven JFET concept is proposed which combines a normally-on JFET with a low -voltage normally-off silicon MOSFET. An intelligent driver solution is developed to benefit from the full JFET performance. Application tests indicate excellent performance of the proposed solution.

Introduction

Efficiency, power density and weight are key parameters in applications like photovoltaic inverters, uninterruptable power supplies and high-speed drives. The fundamental value propositions of the SiC JFET in comparison to known device concepts arise from:

- resistive forward characteristic in first and third quadrant
- monolithic integrated body diode, comparable to available SiC schottky diodes in terms of stored charge
- low output capacitance
- low gate charge
- low switching losses

Application relevant topologies such as buck-, boost-, H4-, B6- and three level inverters can benefit from these features. Due to the low switching losses, the resistive forward characteristic and the negligible charge of the freewheeling diode the efficiency can be improved over the full load range. Simultaneously the switching frequency can be increased from 16 kHz to 48 kHz or even 100 kHz, to allow smaller magnetic components with less copper and thus reduced copper losses. Furthermore, PCB mounted magnetic components are possible.

The integrated body diode of the proposed device enables reactive power and harmonic compensation in the power grid to fulfill the upcoming requirements, especially in solar applications. In the conductive phase of the integrated body diode, the channel of the JFET can also be turned on in parallel to allow a further reduction of the conduction losses in this phase.

Due to the possible fast switching and the low output capacitance, the dead time in a bridge topology can also be reduced to allow more power to be transferred. Compared to an IGBT, the dead-time can be dramatically reduced from currently 1 µs to only 50 ns.

The excellent device characteristics offer several benefits for the user. Obviously the power electronic system will show a clearly improved efficiency, but also the power density will be increased, both with reduced overall system cost.

Device and Driver Concept

Overview on active SiC power device concepts

Recently a number of active wide band-gap power devices have been announced [1-5]. Several device concepts have been proposed such as the BJT [2], MOSFET [3,4], normally-off vertical JFET [5] or normally-on quasi-vertical JFET [6]. Fig. 1 depicts the basic structures of the aforementioned devices. All devices show specific strengths and weaknesses which will be briefly discussed here.
The BJT is a normally-off device, but being current-controlled it requires the use of a special driver circuit. Current gain degradation might occur due to stacking faults [7,8].
The MOSFET, the first SiC-based active switch ever to be made commercially available, is a voltage-controlled normally-off device, which makes this device rather user-friendly. The MOSFET also has an inherent body diode. The overall performance is affected by the reduced channel mobility due to the presence of interface traps. This limits the transconductance of the device and currently requires a larger gate voltage range to drive the device for its full performance. However, the MOSFET offers excellent performance in the 1200 V class, but might be less suited for lower voltage classes.
True vertical JFET devices, irrespective of whether they are normally-on or normally-off, lack an inherent drain-source body diode due to the structure, which is in fact a static-induction transistor (SIT). In addition, the gate-drain overlap is quite large, resulting in a high gate-drain capacitance,

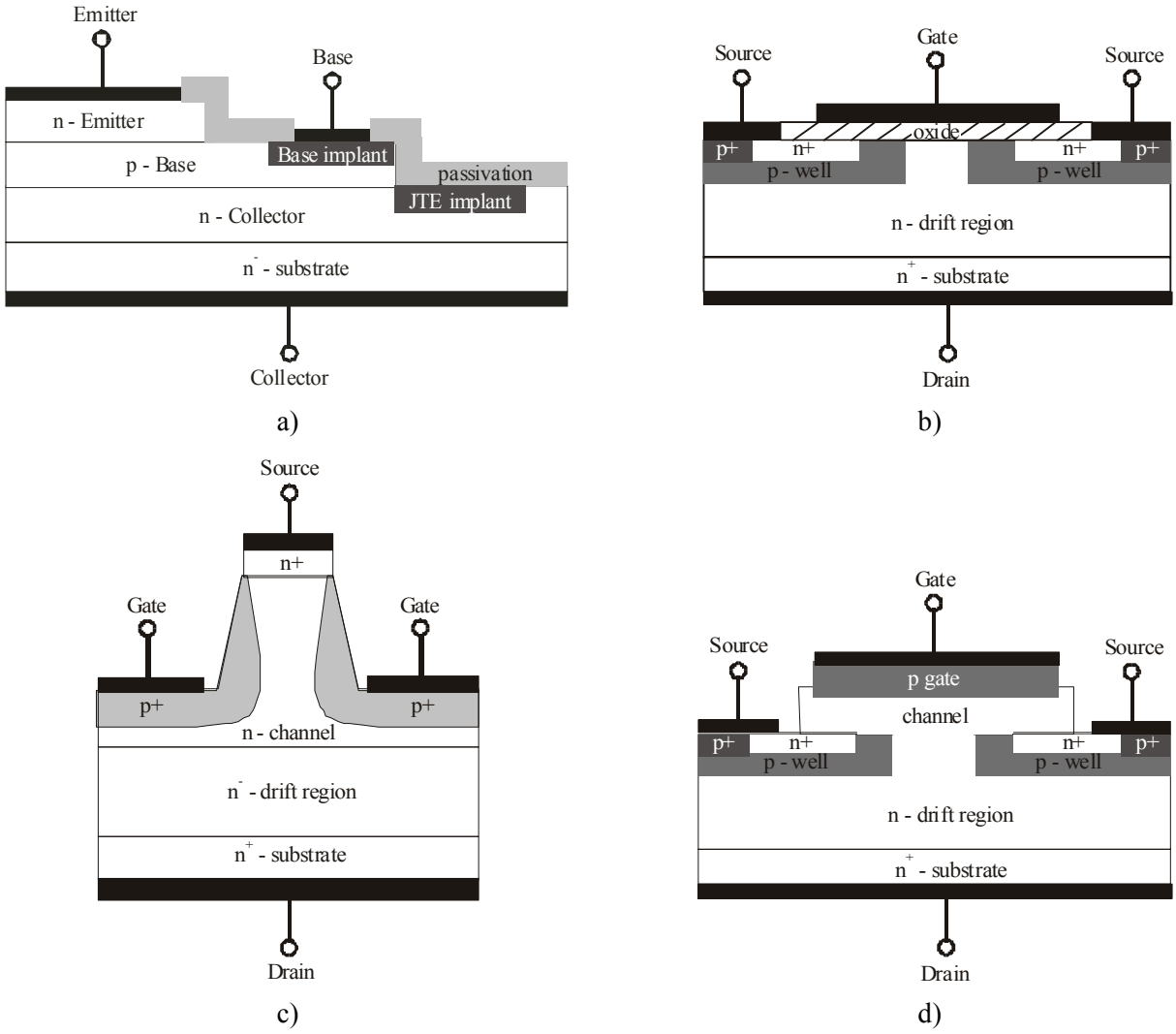

Fig. 1: Basic structure of a) SiC BJT
b) SiC MOSFET
c) vertical normally-off SiC JFET
d) quasi-vertical normally-on SiC JFET

which slows down the device. The triode like output characteristic caused by the short channel requires matching of the channel region to the required blocking voltage [6]. At elevated temperatures the leakage current cannot be neglected, and the temperature coefficient of the on-resistance is relatively large. All JFET devices have a pn-junction controlling the device which starts to conduct at positive gate voltages of ~3 V. In case of a normally-off JFET, a significantly larger gate voltage is required to fully turn on the device, leading to a large gate current. Therefore specially designed driver circuits are needed.
Another option is the normally-on quasi-vertical JFET with a lateral channel and an inherent drain-source body diode. The device shows, like a MOSFET, an advantageous pentode-like output characteristic. The temperature coefficient of the on-resistance is lower than for a normally-off JFET. The gate-source and gate-drain capacitances of the JFET are smaller compared to the MOSFET because of the smaller overlap region between the gate and drain. The normally-on device may also require a special gate driving circuit, although many standard drivers are basically capable of driving such devices. The long-term reliability of all JFETs benefits from the absence of a gate oxide and the fact that the main functional part of the device is located in the semiconductor volume, and not at an interface.

Proposed Normally-On JFET Structure

Regarding good forward conduction, low switching losses and fulfillment of reliability requirements, the normally-on silicon-carbide JFET is one of the most promising devices [6].
Fig. 2 shows the basic structure of such a device. The JFET maintains a lateral channel despite being a vertical power device. In contrast to a SiC-MOSFET solution, the SiC-JFET does not suffer from limitations in the channel mobility, and does not have to consider gate oxide reliability issues – both of which would lead to an increase of the on-resistance. Therefore, the JFET allows for a low area-specific on-resistance which directly affects the chip costs. In difference to a fully vertical JFET structure as proposed in [9], the structure presented has an inherent free-wheeling diode for commutation purposes. The JFET also allows low-loss reverse conduction through the channel.
While it is also possible to realize a normally-off JFET, the disadvantages of such a solution are considered to be too large. To make a normally-off JFET, the channel width must be significantly reduced, which adversely affects the saturation current and strongly enhances the temperature dependence of the on-resistance; also the area-specific on-resistance itself degrades. It must be also considered that the voltage range for control of the device is rather small, since the gate diode starts conducting at voltages of about 3 V.

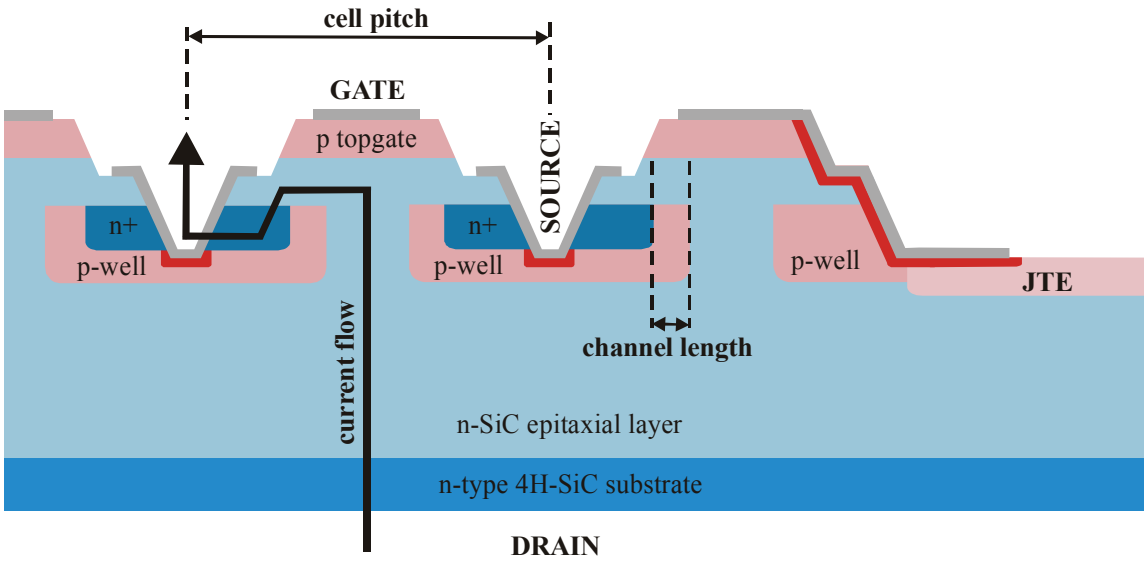

Fig. 2: Schematic structure of the SiC-JFET

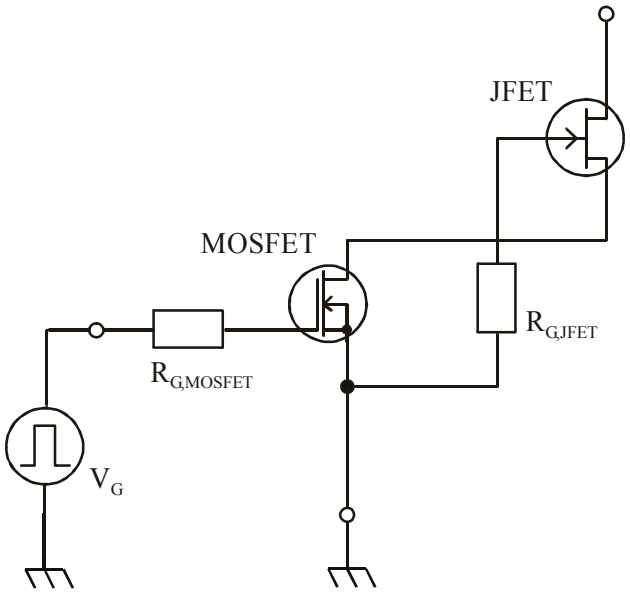

Fig. 3: Conventional cascode switch

Although topologies exist which require the use of normally-on devices [10], today almost all application topologies use normally-off devices. Consequently, it is impossible to simply replace a normally-off device by a normally-on switch. Also most available gate driver units are not capable of delivering the required negative gate voltage to turn off the JFET. Furthermore, a driver supply voltage failure would result in a short circuit damaging the power electronic unit. To allow the easy replacement of common silicon power devices in today's applications, a cascode arrangement looks promising [11]. Fig. 3 shows such a cascode switch. A low-voltage silicon power MOSFET drives the high-voltage SiC-JFET. However, the introduction of a second active switch causes additional conduction and switching losses, and the switching performance will need to be limited in order to avoid oscillations and to guarantee full controllability of the cascode switch [12]. Consequently, an alternative solution is recommended.

The "Direct-Driven JFET" concept

The proposed "Direct-Driven JFET" solution shown in Fig. 4 uses a second driver for the MOSFET. This solution guarantees that the MOSFET is always turned on as long as the driver power supply is present [13]. In normal operation, the circuit acts like a stand-alone JFET and avoids the limitations of

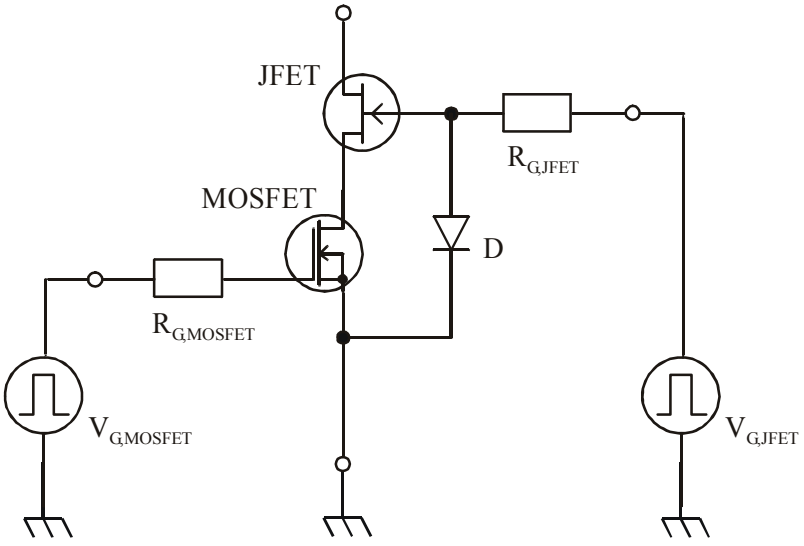

Fig. 4: Schematic of the proposed direct-driven JFET

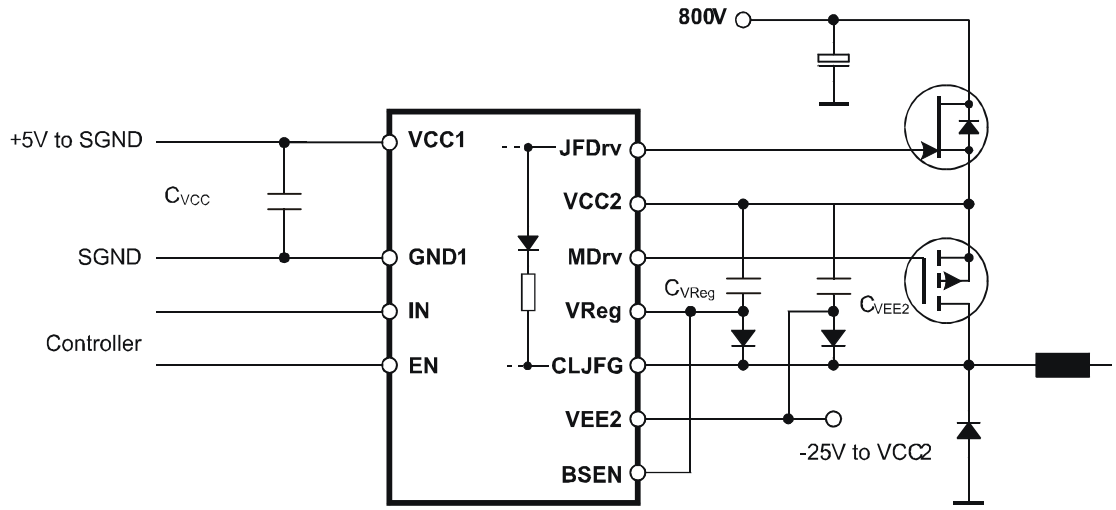

Fig. 5: Block diagram of typical application circuit using the proposed driver IC

a real cascode circuit. In this configuration there are no switching losses due to the MOSFET and no limitations to the switching performance to gain stability. This also allows for a reduction of the conduction losses in the MOSFET by choosing the device having the lowest on-resistance. Therefore, the additional conduction losses introduced by the MOSFET account for less than 3%.
In the case of a failure in the driver power supply, or in other parts of the device, the diode D ensures that the circuit behaves like a standard cascode circuit. Therefore the normally-off feature of the real cascode is reserved for irregular operation modes.
The additional low voltage driver block together with the required logic part can easily be integrated into a single driver IC. Fig. 5 shows the block diagram of a typical application circuit using the dedicated driver unit 1EDI30J12Cx being currently under development. As can be seen in Fig. 5 the use of a p-channel MOSFET is advantageous. Using a p-channel device prevents an increase of the source-inductance in the gate-drive loop of the JFET and simplifies the gate-drive circuit due to the avoidance of a floating source potential of the JFET.

Device performance in a typical application

Measurement setup

Most topologies of interest have to be simplified to allow an analysis of the device behavior. As an example we consider here an H4 bridge. This topology, and the commutation from one conducting leg to the other, is shown schematically in Fig. 6.
The H4 bridge is one of the most important topologies used in current photovoltaic inverters. The power switches are driven with a symmetrical pulse pattern (the diagonal branches are always conductive at the same time). As a consequence, hard commutation of the inherent body diode of the JFET, or of the freewheeling diode in case of an IGBT, occurs at each cycle. This hard commutation is

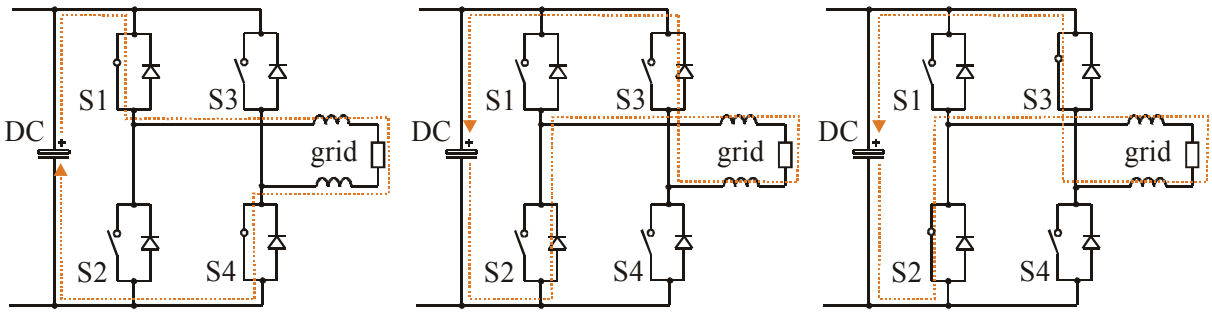

Fig. 6: Commutation in the H4 bridge topology

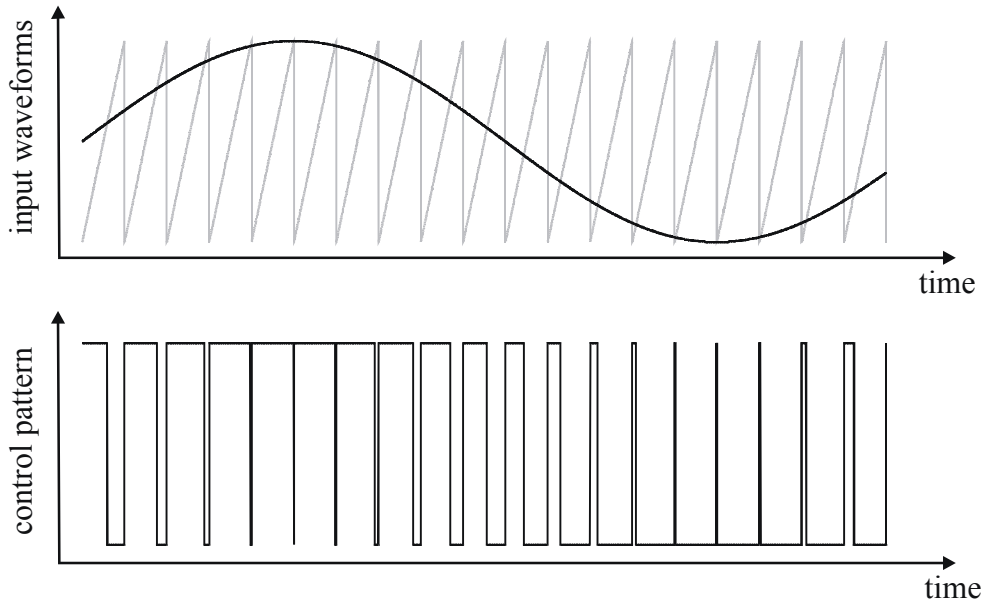

Fig. 7: Generation of the H4 bridge control pattern

the reason that silicon-based MOSFETs cannot be used in such a topology, due to the huge reverse-recovery charge of those devices.
The pulse pattern to control the switches is generated, for example, by the subharmonic method as shown in Fig. 7. Here a sinusoidal signal is compared with a sawtooth waveform. If the latter waveform is less than the sinusoidal one, the output signal is high and otherwise low. This generated pulse pattern is used to drive the diagonal switches S1 and S4 and the inverted pattern to drive S2 and S3. Between the turn-off and the turn-on of the diagonals and vice versa a delay time is necessary to avoid a shot-through in the legs of the bridge. In this phase the current will commutate to the freewheeling diodes on the opposite diagonal. Here the switches are turned on after the required delay time for removing the stored charge of the diodes. As the result the current flows continuously and shows a sinusoidal shape. The investigation of the device switching losses of such a circuit is difficult due to the fact that the turn-on time, the turn-off time and the operating point are all modulated by a sine wave. Therefore it is advantageous to simplify the circuit to allow a fast and easy investigation on application relevant device parameters. Considering a hard-switching topology, as in case of the H4 bridge, a boost stage in a half-bridge topology as shown in Fig. 8 is an equivalent replacement to study the device behavior.
Here the operating point is constant due to the constant DC input voltage and a non-sinusoidal constant pulse pattern. The current is measured in the source (emitter) path of the switch by a shunt with a low inductance and a high bandwidth to avoid negative impacts on the circuit. This simple circuit employs the well-known double-pulse method. The inherent body diode (in the case of the SiC-JFET) or the separate freewheeling diode (in the case of the IGBT) interacts as a boost diode. To

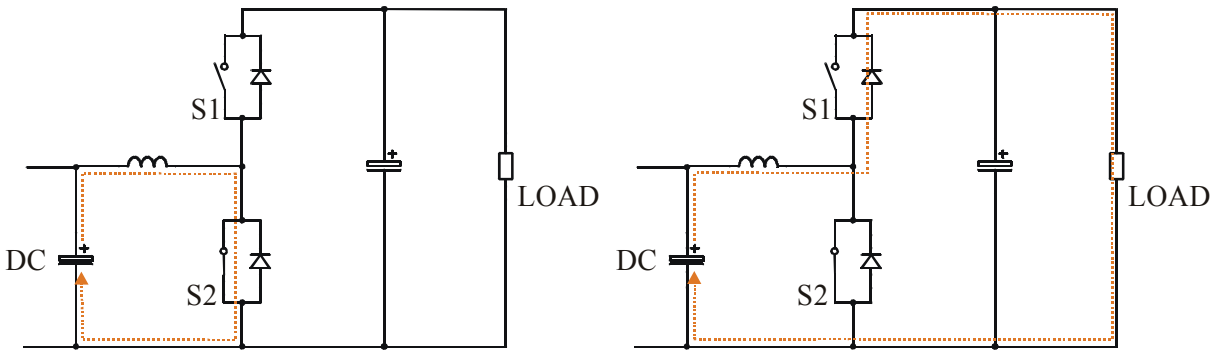

Fig. 8: Body diode commutation in a boost stage

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simulate different applications and conditions, a SiC Schottky diode can be used in parallel to the JFET body diode or instead of the bipolar freewheeling diode.
For the comparison of the IGBT and SiC JFET, a new test bench was developed. The topology follows the previously discussed half-bridge topology of a boost stage. The setup provides the different required gate-control voltages of 0 V to +15 V for the IGBT and -20 V to 2 V for the SiC JFET. The PCB layout was optimized to have an equal stray-inductance in the gate-control loop for both devices, however the resistance of the gate loop was slightly different – 5 Ω in the case of the IGBT and 8 Ω in the case of the SiC JFET. The delay time is adapted according to the device used. A value of 100 ns is used for the SiC JFET and 1 µs for the IGBT. During the main phase of body diode conduction the JFET channel is open to minimize the conduction losses of the internal body diode.

Simulation setup

To investigate the device behavior in the application, the simplified circuit was implemented in a circuit simulator [14]. However the modeling of a real circuit is a complex task, since – especially in case of fast switching devices – even small parasitic elements in the circuit start to influence the measurement results. The interactions of fast switching devices with their environment can not be neglected. In particular the commutation-loop impedance, the source stray inductance and the gate-loop impedance are fundamental parameters and part of the device feedback loop.
The origins of those parasitic elements are the layers on the PCB itself and also the packages of the power semiconductor devices. Therefore the parasitic of the PCB were analyzed using Ansys Q3D Extractor® which results in a complex electrical network representing the whole board [15]. The generated netlist can easily be used in the Spice simulations. Also the package of the power device was modeled using this method. As the result, the behavior of the device in a given environment can be much better predicted. Efficiency, EMC, ringing and the behavior under several conditions can be more easily analyzed and improved.
To reproduce the electrical behavior of the semiconductor itself, a Spice model of the SiC JFET was built based completely on the results of 2D device simulations in a first stage. [12]. For the results presented in this work, the device model was later adapted in accordance with the results of a complete stationary and dynamical device characterization.

Simulation and measurement results

Based on the previously described simulation setup, the SiC JFET behavior was studied and compared to other devices such as our High Speed 3 IGBT series. As an example Fig. 9 compares the turn-on losses of a 100mΩ SiC-JFET in direct-driven configuration and a discrete High Speed 3 IGBT rated for 25 A [16] in simulation and measurement. Here the SiC JFET shows clearly lower turn-on losses

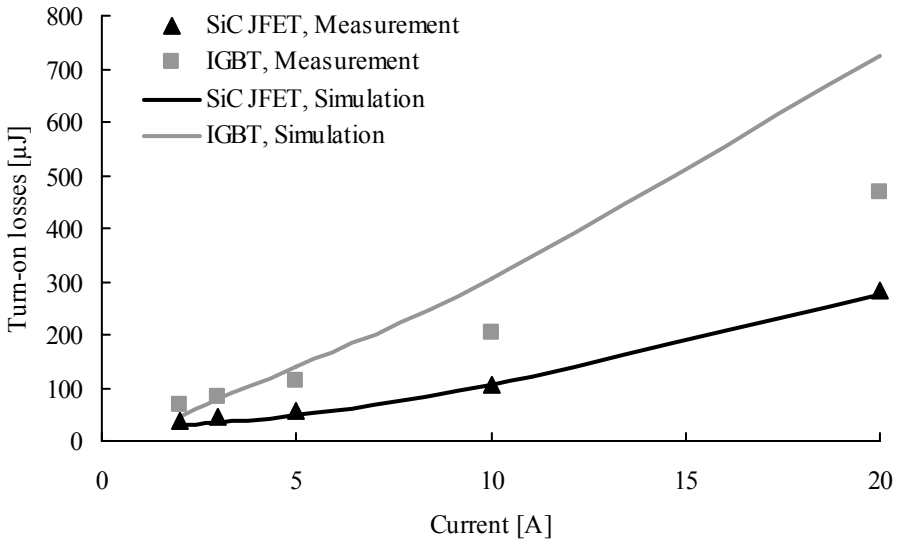

Fig. 9: Comparison of turn-on losses in simulation and in measurement for the 1200V SiC-JFET and the High Speed IGBT3 (R_G = 2 Ω, L_{Source} = 5 nH)

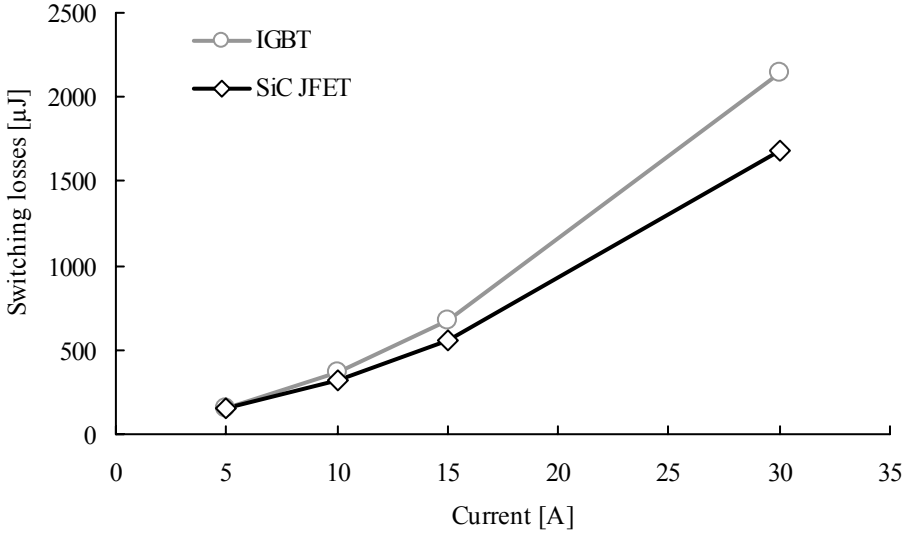

Fig. 10: Overall switching losses as function of current (T_j = 75 °C, R_G = 8 Ω, L_{Source} = 35 nH)

over the full investigated current range. The deviations between the simulated and measured values for the IGBT are related to the necessary simplifications in the device model, namely the difficulties in the modeling of the excess carrier injection and removal for the full range of current, voltage and temperature conditions.

Fig. 10 gives a comparison of the total switching losses between the SiC JFET and the High Speed 3 IGBT at an elevated temperature of about 75 °C. This temperature is a typical average value for devices used in solar inverters. Again the SiC JFET outperforms the IGBT, especially under high load conditions.

As a next step, these results were evaluated in a real application. Here, the previously described 4H bridge topology was chosen. Fig. 11 gives a comparison of the overall system efficiency between the case of the SiC JFET and that of the High Speed 3 IGBT under identical conditions. The system employing the SiC JFET switch is capable of increasing the system efficiency over the full load range and comes close to the 99 % limit at the point of its maximum efficiency. The results confirm other reports where it was shown that with the use of SiC-based power switches overall efficiencies of 99% might be reached, and an efficiency benefit of around 2% over the full load range in comparison to an IGBT was possible [17].

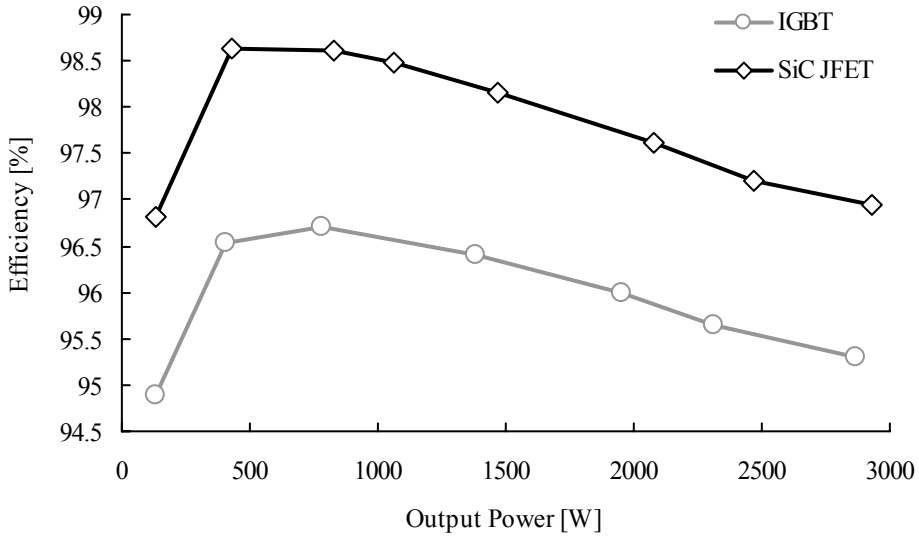

Fig. 11: Comparison of the efficiency for SiC JFET and IGBT in a H4 bridge topology (V_{DC} = 400 V)

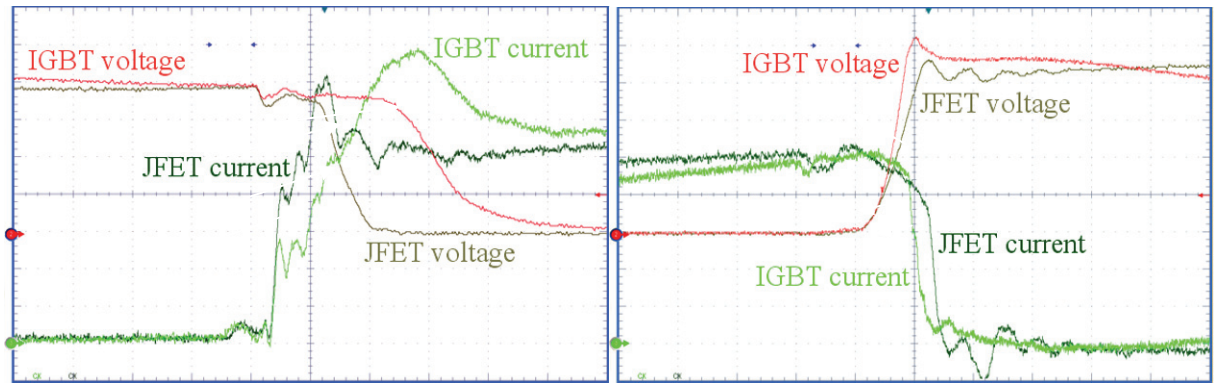

Fig. 12: Comparison of turn-on (left) and turn-off (right) waveforms of IGBT and SiC JFET (voltage 100V/div, current 2A/div, time 20ns/div)

Finally, the switching waveforms for both devices are shown in Fig. 12. Here, the turn-on- and turn-off-waveforms at a drain (collector) current of 10 A are shown. For the turn-on of both devices the switching waveforms are comparable. During the turn-off the JFET has a smoother switching behavior leading to reduced overvoltage peaks compared to the IGBT. These waveforms are a good indication of the excellent switching properties of the device. Considering the presented measurement results, the 1200V direct-driven SiC JFET is perfectly suited for use in photovoltaic inverters.

Conclusion

In this work, the properties of a normally-on SiC JFET as a fast-switching power device are discussed. The Direct-Driven JFET solution is presented which allows the usage of the JFET in topologies employing normally-off devices.

Despite the different topologies used in photovoltaic inverters, the direct-driven SiC JFET is best suited for use in DC/AC stages of single-phase and three-phase solutions. Here, the suggested solution can replace the currently used IGBT. The general requirements for these systems include high efficiency at partial and full load, high reliability, easy maintenance, low noise to fulfill EMC requirements and efficient cooling to allow lightweight systems. Therefore, applicable power semiconductors should combine low switching losses, resistive characteristics in the in first and third quadrant, a linear dependency in the output capacitance, negligible charge of the freewheeling diode, an appropriate Miller capacitance to avoid the onset of oscillations, and a high ruggedness and reliability.

The SiC-JFET is very capable of meeting all of these requirements. However, the device must be optimized to be best suited to the requirements during the development process. To avoid large numbers of different manufactured samples, application simulations using compact models based on the results of device simulations were used in a first step and compared with the performance of commonly used devices. First priority was given to the evaluation of overall switching losses. For these investigations, a hard-switching topology was used.

Measurements of the proposed Direct-Driven SiC JFET in comparison to an IGBT in a well-known 4H bridge topology showed an efficiency benefit of around 2% over the full load range and that the presented solution will be a most attractive choice for use in photovoltaic inverters.

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