Stability and performance analysis of a cascode switch

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Abstract

Wide band-gap semiconductors are most attractive as a material for power devices due to low losses, improved temperature capability and high thermal conductivity. Although silicon carbide Schottky diodes have been commercially available on the market for years, an active wide band-gap switch is still missing. Probably the best performance of upcoming devices is gained with normally-on concepts such as silicon-carbide JFETs and gallium-nitride HEMTs. However, the vast majority of power electronic topologies do rely on normally-off switches. An alternative way is the use of the cascode concept which combines a normally-on wide band-gap device with high blocking capability and a low-voltage normally-off silicon MOSFET. In this work, the performance and stability of such an arrangement is analyzed and an alternative solution is proposed.

Keywords: JFET, MOSFET, SiC, Cascode, Stability, Performance

INTRODUCTION

Recently a number of reports suggest the availability of active wide band-gap power devices within the next few years [1]. Regarding good forward conduction, low switching losses and fulfillment of reliability requirements, the normally-on silicon-carbide JFET is one of the most promising devices [2]. Fig. 1 shows the basic structure of such a device. Although topologies exist which require the use of normally-on devices [3], today almost all application topologies use normally-off devices. Consequently, it is impossible to simply replace a normally-off device by a normally-on switch. Also most available gate driver units are not capable to deliver the required negative gate voltage to turn-off the JFET. Furthermore a driver supply voltage failure would result in a short circuit damaging the power electronic unit.
To allow an easy replacement of common silicon power devices in today's applications, a cascode arrangement looks promising [4]. Fig. 2 shows such a cascode switch. A low-voltage silicon power MOSFET drives the high-voltage silicon-carbide JFET. However, the introduction of a second switch causes additional losses and might result in instabilities under certain conditions. To ensure a reliable operation of the cascode as a power switch, the following requirements must be fulfilled:

- the turn-on- and turn-off-process must be actively controlled by the gate (controllability of dv/dt and di/dt)
- there should be no or little oscillations in the switching processes
- none of the devices should be driven into avalanche mode
- total losses must be reasonably lower compared to already available devices such as SJ-MOSFETs

CONTROLLABILITY ANALYSIS

A typical application of a high-voltage power MOSFET is found in power factor correction (PFC) stages of power supplies. Consequently, for the stability analysis a simplified equivalent circuit of a PFC stage was used as shown in Fig. 3. The cascode itself is modeled by the elements within the dotted square.

Turn-On Process

During turn-on the gate-source-capacitance CGS,M is charged via RG,M till plateau voltage Vplat,M is reached. Now the MOSFET channel becomes conductive and a displacement current thru CGD,M

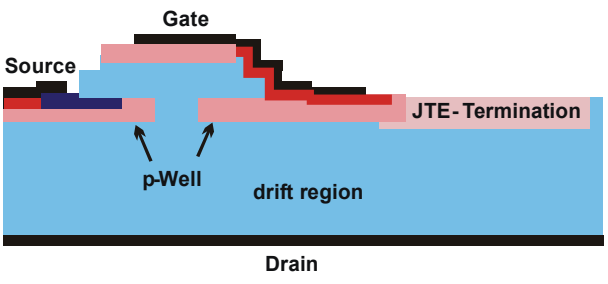

Fig. 1: Basic structure of a vertical normally-on silicon-carbide JFET

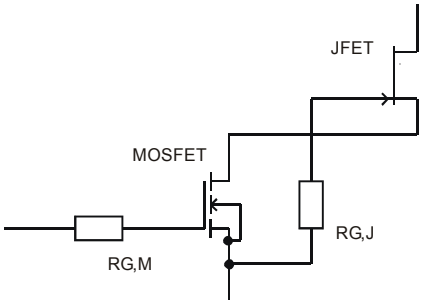

Fig. 2: Cascode switch formed by a normally-off MOSFET and a normally-on JFET

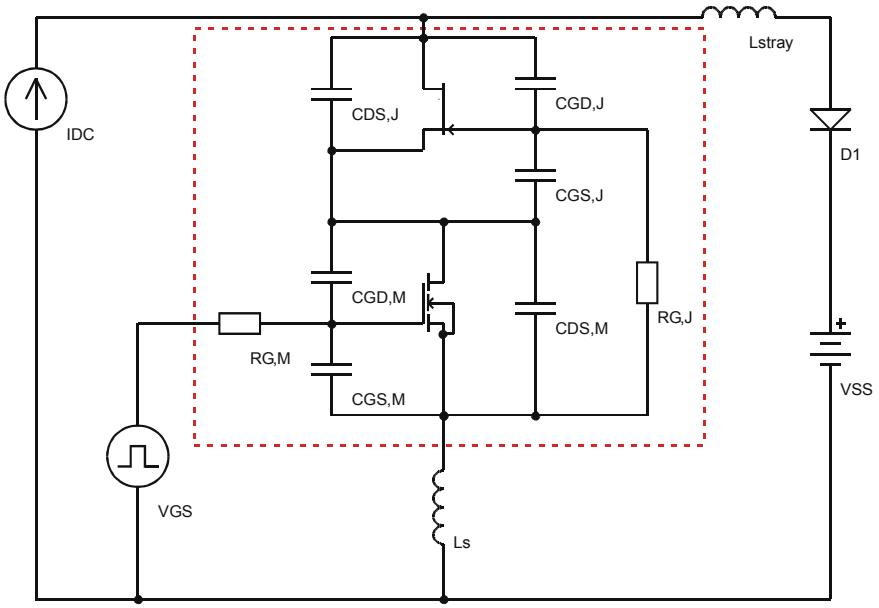

Fig. 3: Simplified equivalent circuit of a simple PFC stage using a cascode switch arrangement

flows. Since this lowers the drain-to-source voltage of the MOSFET VDS,M, there must be a displacement current thru CDS,M as well. In parallel to CDS,M, there is also the gate-source capacitance CGS,J of the JFET. This additional current flow is delayed by the JFET gate resistor RG,J. The rising gate voltage at the JFET allows a current flow thru the JFET. In normal cases (except very fast switching or very low load current) an equilibrium is established that leads to a roughly constant di/dt and VDS across the complete cascode. To keep full control of the turn-on process and allow for a limitation of the di/dt and dv/dt, the MOSFET must operate in linear mode until the JFET is fully turned-on. In most cases the stray inductance Ls at the source of the cascode limits the di/dt and provides the required stability:

$$L_S > \lambda \qquad (1),$$

with:

$$\lambda = \frac{C_{GD,M}\, R_{G,M}}{g_{fsJ}} \qquad (2),$$

g_{fsJ} being the forward transconductance of the JFET.
However, the MOSFET might reach the end of the plateau phase before the JFET can support the entire current. In this case, there is no control connection between JFET and MOSFET anymore and both devices are charged independently. Now the gate resistor of the MOSFET RG,M has no influence on the further switching process and the rise of the JFET gate voltage VGS,J is now controlled by the JFET gate resistance RG,J and the JFET input capacitance CGS,J+CGD,J.
Under this condition the controllability is only given if the following condition is fulfilled:

$$\frac{Q_{GD,M} \cdot R_{G,M}}{\left(V_{G,M} - V_{plat,M}\right)\left(1 - \frac{L_s}{\lambda}\right)} \geq \frac{I_{DC}\left(L_s + \lambda\right)}{V_G - V_{plat}} + C_{GS,J} \cdot R_{G,J} \qquad (3).$$

If the di/dt during turn-on is not limited by the present source inductance L_S itself, a limitation can be practically reached by a reasonably large value of the MOSFET gate resistor RG,M. Beside this, best controllability and lowest switching losses require a small JFET gate resistor RG,J $\rightarrow$0.

Turn-Off Process

Keeping complete control of the turn-off process of the cascode which translates into an active limitation of the resulting di/dt and dv/dt is more difficult than in case of the turn-on process.
At the beginning of the turn-off process the gate of the MOSFET is discharged via the gate resistor RG,M until the plateau voltage is reached. Now the voltage across the MOSFET starts to rise. The capacitance CGD,M is charged while CDS,M is discharged by the channel current of the JFET (both capacitances form the output capacitance of the MOSFET). At the same time the rising voltage across the MOSFET causes a displacement current through CGS,J and CGD,J. This current flow leads to a reduction of the Gate-Source-voltage of the JFET. All these displacement currents reduce the channel current of the MOSFET, additionally the displacement current through CGD,J also reduces the channel current of the JFET. Of course it is basically the load current which causes the recharge of the capacitances.
In difference to the turn-on process there are now more scenarios which might occur during the continuation of the turn-off process where most of them should be avoided to keep control.
If the MOSFET is chosen too big with respect to the load current, the MOSFET displacement currents through CDS,M and CDG,M are larger than the respective displacement current through CDS,J and CDG,J of the JFET. Under this condition the channel

current through the MOSFET disappears and the MOSFET leaves the linear mode. In order to allow the JFET current to flow, the VGS,J is clamped as the JFET is still in linear mode. The voltage rise is now only controlled by the load current. In case the cascode is switched to fast and/or the stray inductance is too large, the JFET can be driven into avalanche. If a gate resistor for the JFET is present (which is considered to be the normal case), the voltage across the MOSFET will be higher than VGS,J and the MOSFET might also be driven into avalanche.
Otherwise, if the MOSFET size is correctly chosen, the load current is used to charge the output capacitance of both devices (CGD,M + CDS,M + CGS,J + CGD,J). The MOSFET is operated in the linear region while the JFET is still fully on. The gate-source voltage VGS,J of the JFET decreases till the JFET reaches the linear region. Now the CDS,J is charged and the channel current of the JFET is reduced. A further reduction of the JFET channel current now needs a reduction of the VGS,J which is controlled by the voltage VDS,M across the MOSFET which in turn is controlled by the gate resistance RG,M. Even if a JFET gate resistor RG,J is present, the voltages at MOSFET and JFET will rise concurrently, where the dv/dt at the cascode will increase at least till the outer voltage VSS is reached. The dv/dt at the MOSFET stays roughly constant.
Once the voltage across the cascode is larger than the sum of the outer voltage VSS and the voltage drop across the freewheeling diode D1 (due to the presence of the stray inductance), a current through the freewheeling diode starts to rise which makes the cascode current fall. The voltage increase at the cascode will finally stop if the entire current was taken over by the freewheeling diode.
For high currents at large di/dt with respect to the present value of the stray inductance, the voltage increase might exceed the breakdown voltage either of the JFET or of the MOSFET. In both cases controllability is lost. The only way to avoid this scenario is to choose a reasonably high gate resistance RG,M.
If the JFET channel current finally disappears, the VGS,J of the JFET falls below the pinch-off voltage VPI,J or even reaches the punch-through voltage VPT,J of the JFETs gate-source-structure. To avoid avalanche of the MOSFET, the breakdown voltage of the MOSFET should be reasonably larger than the pinch-off voltage of the JFET.
A complete control of the turn-off process and therefore an active control of the resulting dv/dt and di/dt is only possible if the MOSFET stays in linear mode over the complete turn-off process.
It is also most important to keep the offset between the Drain-Source-Voltage of the MOSFET and the Gate-Source-Voltage of the JFET as small as possible. This offset is mainly caused by the voltage drop across the JFET gate resistor and delays the turn-off of the JFET. If this delay becomes to long, the MOSFET enters avalanche mode. Once this point is reached, the controllability of the cascode via the gate of the MOSFET is lost and the remaining part of the turn-off process is governed by the load current. High di/dt and dv/dt as well as oscillations are likely consequences. To keep control of the turn-off process, the following condition must be met:

$$\frac{C_{GS,J}\big|_{V_{DS}=V_{DSS}}\, R_{G,J}}{C_{GD,M}\big|_{V_{DS}=0}\, R_{G,M}} V_{plat,M} < V_{BR,M} + V_{PI,J} \qquad (4).$$

A violation of the condition given by Eqn. 4 will result in loosing control. Likely consequences are driving either the MOSFET or the JFET into avalanche mode, the occurrence of large di/dt and dv/dt and the triggering of oscillations.

Avoidance of Oscillations

Oscillations may occur during the cascode switching processes as shown in Fig. 4. They are caused by the capacitive elements of the cascode arrangements which form resonant circuits with unavoidable inductive elements in the complete circuit. Especially the turn-off process is critical even if the controllability condition according to Eqn. 4 is met.
Oscillations may start during the switching process since at that time all the necessary ingredients are present – capacitances, at least one active element and an inductance. First, both devices work in linear mode simultaneously during turn-off. This might cause an amplification of oscillations in case of a positive feedback to the gate of the MOSFET. Second, most capacitances decrease during the turn-off process due to an increase of the space-charge width. This results in a decreased attenuation of appearing oscillations. Third, there is always a stray inductance present. The necessary trigger of the oscillations is given by the common voltage overshoot across the cascode while turning-off.
To find conditions for the avoidance of oscillations, the circuit can be described by an appropriate differential equation. The capacitances CGD,J, CGD,M and CGS,M (c.f Fig. 3) were cancelled for reasons of simplicity and since they are rather small which leads to Eqn. 5.

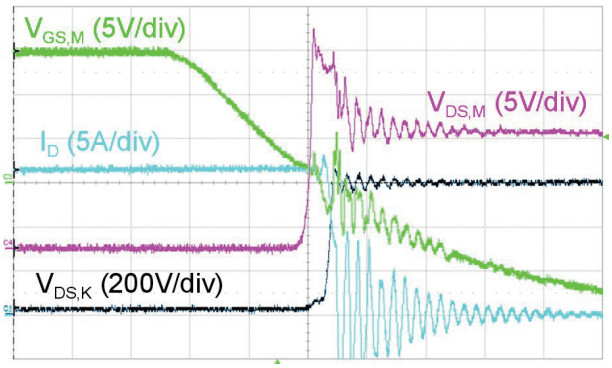

Fig. 4: Measured oscillations during the turn-off of a cascode switch

$$L_{stray} R_{G,J} C_{DS,M} \frac{d^4 i}{dt^4} + L_{stray} \left(\frac{C_{DS,M}}{C_{GS,J}} + 1 \right) \frac{d^3 i}{dt^3} +$$
$$R_{G,J} \left(\frac{C_{DS,M}}{C_{DS,J}} + 1 \right) \frac{d^2 i}{dt^2} + \qquad (5).$$
$$\frac{1}{C_{DS,J}} \left(\frac{C_{DS,M}}{C_{GS,J}} + \frac{C_{DS,J}}{C_{GS,J}} + 1 \right) \frac{di}{dt} + \frac{gfs_J}{C_{GS,J} C_{DS,J}} = 0$$

Oscillations are attenuated as long as the real parts of the zeros of the characteristic polynomial are negative which is desired. It is clear that completely cancelling the JFET gate resistor results in lowest switching losses. On the other hand the JFET gate resistor acts as the most effective damping element towards oscillations and thus cannot be eliminated. Another damping element is, to some extent, the MOSFET gate resistor RG,M. A larger value helps, but also increases switching losses. Finally also a lower value of the stray inductance L_{stray} supports the avoidance of unwanted oscillations.

Verification

To verify the results of the controllability analysis, the combination of a 40 V MOSFET and a 600 V SiC JFET was investigated by circuit simulation. The used circuit is the PFC stage as already shown in Fig. 3 having a stray inductance $L_{stray} = 40$ nH and a source inductance $L_s = 4$ nH. An appropriate Spice model for the 600 V SiC JFET was provided based on the results of extensive 2D device simulation.

The investigation shown in this work was done using four input parameters: the MOSFET gate resistor RG,M, the JFET gate resistor RG,J, the switched current IDC and the supply voltage VSS. These input parameters have been varied to form a fully squared-type DoE (Design of Experiments). Fig. 5 shows the corresponding model for the turn-off process of the cascode as derived from the full set of simulations. Chosen output parameters are the di/dt and dv/dt, turn-off losses Eoff, the amplitude of superimposed oscillations Vosc on the voltage across the cascode, the maximum overvoltage peak Vovershoot superimposed on the voltage across the cascode and the time tav for the MOSFET being in avalanche mode.

With the chosen parameters of VSS = 400 V, RG,J = 39 Ω and RG,M = 55 Ω, an avalanche of the MOSFET as well as the occurrence of self-amplifying oscillations is safely prevented over the whole current range of interest. Thus the two values of the gate resistors allow safe operation of this cascode arrangement. A crosscheck is done by using these values first in Eqn. 1 for turn-on:

$$\begin{aligned} L_S &> \lambda \\ \lambda &= \frac{C_{GD,M} R_{G,M}}{g_{fsJ}} = \frac{60\text{pF}\ 55\Omega}{3\text{S}} = 1.1\text{nH} \\ L_S &= 4\text{nH} \\ 4\text{nH} &> 1.1\text{nH} \end{aligned} \qquad (6),$$

and again in Eqn. 4 for turn-off:

$$\frac{C_{GS,J}\big|_{V_{DS}=V_{DSS}} R_{G,J}}{C_{GD,M}\big|_{V_{DS}=0} R_{G,M}} V_{plat,M} < V_{BR,M} + V_{PI,J}$$
$$\frac{100\text{pF}\ 39\Omega}{60\text{pF}\ 55\Omega} 3.4\text{V} < 40\text{V} - 14\text{V} \qquad (7).$$
$$4.02\text{V} < 26\text{V}$$

Obviously the values found by the simulation DoE fulfill the analytically derived conditions.

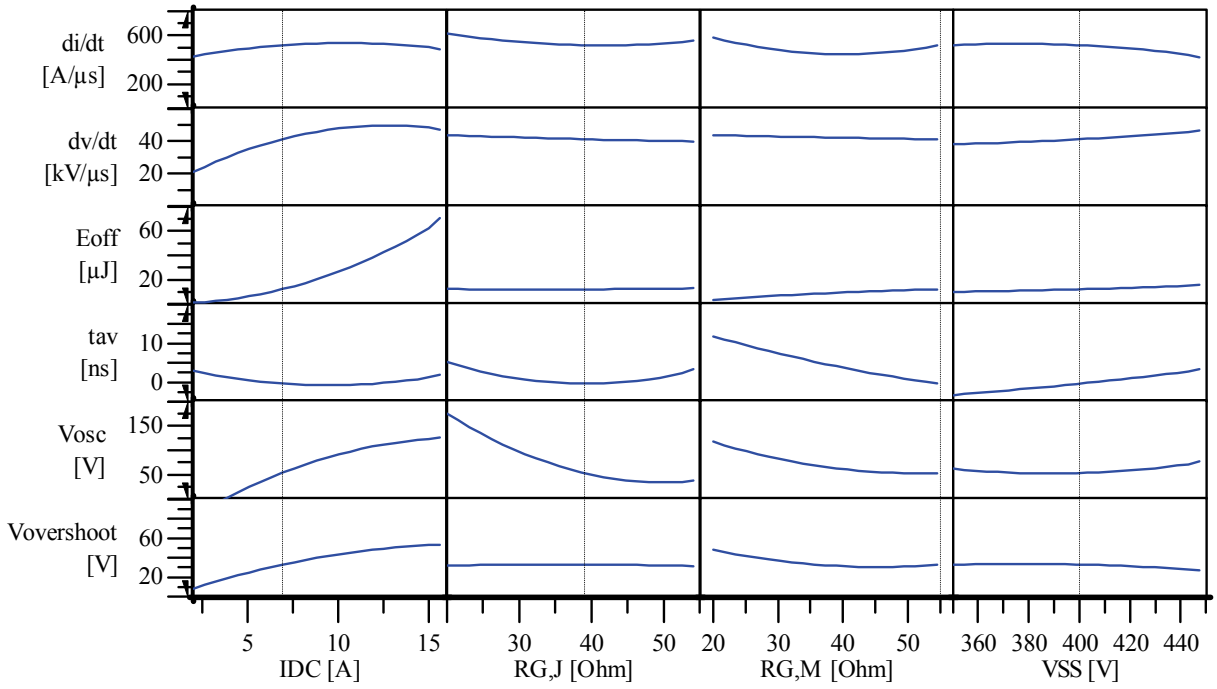

Fig. 5: Model for the turn-off analysis of a 600 V cascode switch based on a simulation DoE

PERFORMANCE ANALYSIS

To characterize the performance of the cascode, again the already known PFC stage of a power supply was chosen. Here the operating voltage is usually in the range of 400 V which requires devices with a blocking voltage of 600 V. However, SiC-JFET demonstrators had a significantly larger blocking voltage of app. 1000 V and yet a larger Rds(on) as a fully optimized device. A cascode using these JFETs and 30 V MOSFETs was assembled and measured.

Fig. 6 shows the measured losses in dependence of the maximum dv/dt during turn-on. These measurements were also done for all remaining di/dt and dv/dt at turn-on and turn-off and later compared with Spice simulations. The comparison allows the estimation of deviations between measurements and simulations. Fig. 7 gives that comparison for the turn-off process. It can be seen that the simulations tend to give lower losses and larger dv/dt and di/dt. This fact relates to simplifications introduced to the simulation circuit. The circuit does not reflect all parasitic elements which will affect a slow-down of the switching processes during measurements.

To allow for an analysis of the behavior of a real 600 V cascode, the Spice model for the 600 V SiC JFET based on 2D device simulations is used again. By means of simulations the behavior of the 600 V cascode was compared to that of the 600 V SJ MOSFET. The values of both gate resistors were chosen in a way that all previously derived controllability conditions for safe switching are met. Fig. 8 gives a comparison of the simulations.

The measured setup using first SiC JFET demonstrators already showed advantages in the performance compared against a 600 V SJ MOSFET, but oscillations were sometimes observed in the measurements as well as in the simulations, especially at low currents. In contrast, the simulated setup with the 600 V SiC JFET showed an even more improved performance in comparison with the SJ MOSFET. In the simulated parameter range, no oscillations were observed.

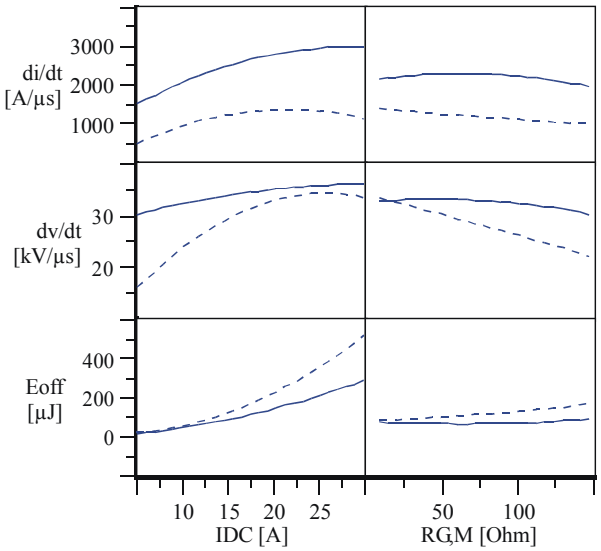

Fig. 7: Comparison of measured (dotted lines) and simulated (straight lines) values at turn-off for a cascode using a SiC JFET

The cascode outperforms available SJ silicon devices, however it is clear that a stand-alone JFET would perform clearly better due to two main reasons:

First, the cascode has a much larger output capacitance than a single JFET due to the capacitances of the low-voltage MOSFET as depicted in Fig. 9. The larger output charge is directly related to an increase of the turn-on losses in an inverter topology. Fig. 10 gives a comparison of the turn-on waveforms for a cascode switch and a stand-alone JFET in an identical environment. The cascode shows a clearly higher reverse-recovery-like current peak which triggers oscillations in the circuit. In case of the stand-alone JFET the waveform owns a lower current peak and looks smooth. Regarding the turn-on losses the cascode circuit consumes 440 µJ while the stand-alone JFET needs only 160 µJ. As a consequence the MOSFET size

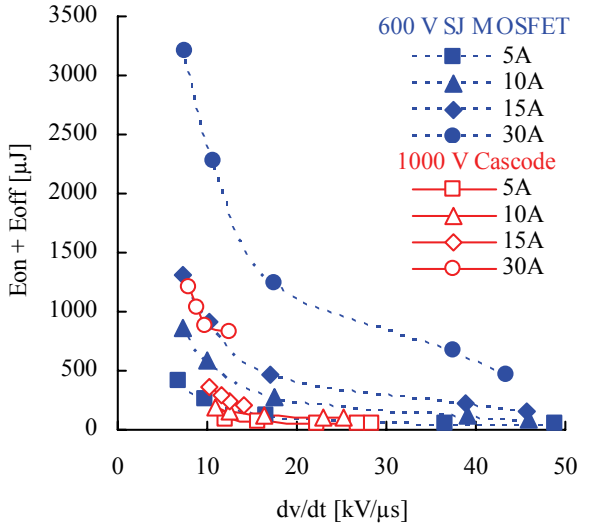

Fig. 6: Measured losses vs. dv/dt at turn-on for a 1000 V SiC JFET cascode and a 600 V SJ MOSFET

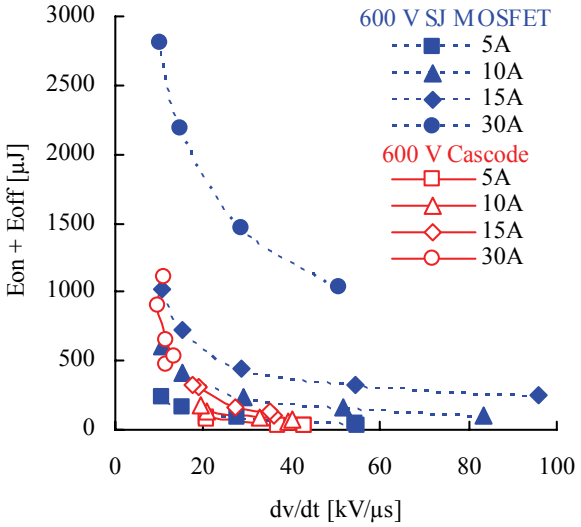

Fig. 8: Simulated losses vs. dv/dt at turn-on for a 600 V SiC JFET cascode and a 600 V SJ MOSFET

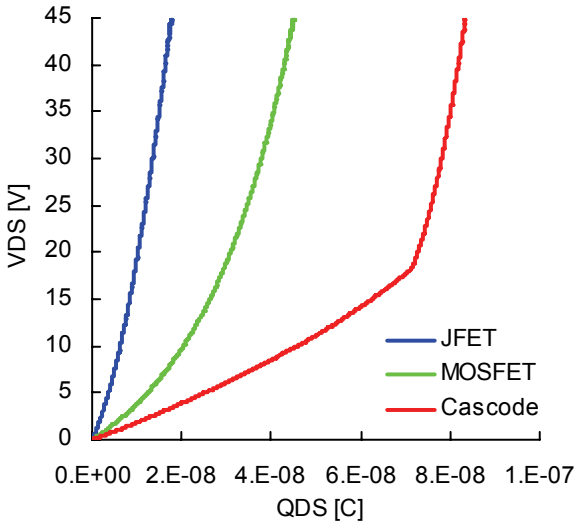

Fig. 9: Gate-drain-charge at a constant current of 1mA (device in off-state)

must be carefully chosen to find an optimum between conduction losses and switching losses of the cascode.
Second, the cascode switching speed must be limited to control the maximum di/dt and dv/dt. As shown before in the controllability analysis, this is mainly reached by relatively large gate resistors of the MOSFET and also the JFET. Unfortunately, this also significantly lowers the switching speed and therefore causes larger switching losses as in the case of a stand-alone JFET.
A better solution is shown in Fig. 11. In this "Cascode Light" a second driver for the MOSFET guarantees that the MOSFET is always turned-on as long as the driver power supply is present [5,6]. In normal operation the cascode now acts like a stand-alone JFET and avoids the limitations of a real cascode circuit.

CONCLUSION

A cascode arrangement offers the chance to realize normally-off power devices using SiC JFETs. In this work, the stability and performance of such a cascode approach formed by a normally-on SiC JFET having a high blocking voltage and a normally-off silicon MOSFET having a low blocking voltage is analyzed. Conditions are derived that guarantee full controllability of the cascode switch and to attenuate possible oscillations. Although such a cascode arrangement outperforms available silicon power devices the performance suffers from additional losses introduced by the MOSFET. An alternative solution is presented offering the full performance of a SiC JFET device.

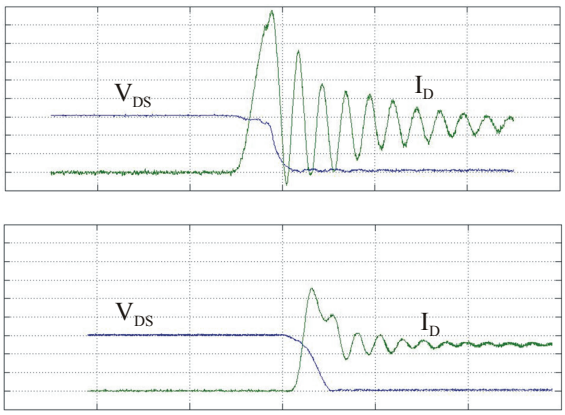

Fig. 10: Turn-on waveforms of a cascode switch (top) and a stand-alone JFET (bottom) in the same inverter circuit (I_D: 4A/div, V_{DS}: 200V/div, time: 100ns/div)

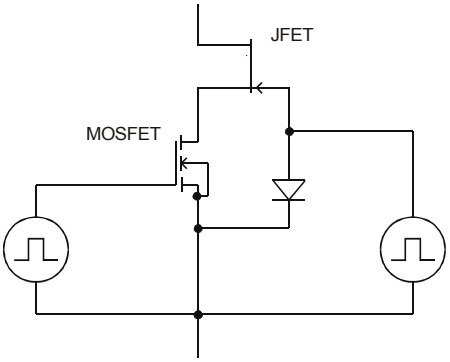

Fig. 11: Modified cascode circuit with separate driver units for MOSFET and JFET

REFERENCES

[1] Kaminski, N.: State-of-the-art and Future of Wide Band-gap devices, Proc. EPE (Barcelona 2009)

[2] Treu, M., Rupp, R., Blaschitz, P., Rüschenschmidt, K., Sekinger, T., Friedrichs, P., Elpelt, R. and Peters, D.: Strategic considerations for unipolar SiC switch options: JFET vs. MOSFET, Proc. IAS (New Orleans 2007)

[3] Rashid, M.H.: *Power Electronics – Circuits, Devices and Applications*, Pearson Education Inc., 2004

[4] Baliga, B.J. and Adler, M.S.: Composite Circuit for Power Semiconductor Switching. European Patent EP 0 063 749 B1, 1982

[5] Melkonyan, A.: *High Efficiency Power Supply using new SiC Devices*, PhD thesis, University of Kassel, 2006

[6] Domes, D. and Zhang, Xi.: CASCODE LIGHT – normally-on JFET stand alone performance in a normally-off Cascode circuit. Proc. PCIM (Nuernberg 2010)

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