Impact of synchronous rectification MOSFET capacitance on the overall efficiency of LLC converters

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Abstract

Low-voltage power MOSFETs based on charge-compensation using a field-plate combine a significant reduction of the area-specific on-resistance with excellent switching properties being attractive for a wide range of applications. The use of such devices in the synchronous rectification stage of power supplies employing a resonant topology on the primary side enables a further improvement of the overall converter efficiency. Besides a low on-resistance also the output charge and the shape of the output capacitance of the power MOSFET impact the losses in the synchronous rectifier. This work discusses how the structure of the power semiconductor component used affects these properties and the mechanism behind its impact on the overall efficiency of the whole converter.

Keywords: Power MOSFET, device capacitance, LLC converter, synchronous rectification, device performance.

INTRODUCTION

Low-voltage power MOSFETs based on charge-compensation using an isolated field-plate offer a significant reduction of the area-specific on-resistance [1] – [9]. Thanks to their overall excellent performance, this class of devices has become established as the standard device of choice for applications requiring fast-switching power devices. Potential target applications include primary side switches and synchronous rectification stages of switch-mode power supplies, low-voltage motor drives or solar power optimizers. Consequently these devices are used both in hard- and soft-switching topologies.

Soft-switching techniques as employed in LLC resonant topologies allow a further improvement of the efficiency in power supplies used for telecom rectifiers or servers [10] - [12]. However, these techniques reduce losses on the primary side while leaving the secondary-side rectification-related losses to be addressed. This is why the diodes were replaced by power MOSFETs acting as synchronous rectifiers (SR) as illustrated in the basic schematic shown in Fig. 1. This measure dramatically reduced the rectification conduction losses and enabled a further increase of the converter efficiency and the power density [13]. As for any switched power device, losses related to the switching of the SR MOSFETs also contribute to the overall losses. This means that especially the output capacitance and the linked charge of the used power device will have a significant impact. Consequently the device structure may play an important role as it not only defines the overall amount of charge but also causes a different shape of the capacitance, which will vary more or less non-linearly with the voltage applied over the

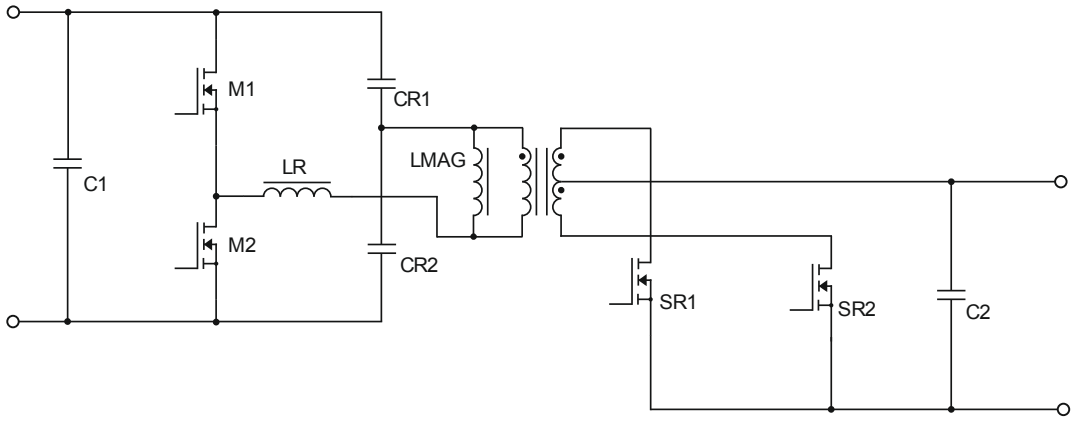

Fig. 1: Basic schematic of a LLC converter with synchronous rectification on the secondary side

power semiconductor device.
In previous work we discussed two options on how to extend the blocking capability of these devices towards higher breakdown voltages in order to address the so-called medium-voltage range of 150 V – 300 V. The performance of both design concepts was evaluated using devices with a blocking voltage of 150 V in different applications [14].
This work focuses on the impact of the device properties on the performance and efficiency of the LLC synchronous rectifier stage. The investigation is done using the example of three different devices structures. The comparison includes a standard trench power MOSFET and two alternative charge-compensated field-plate trench power MOSFETs in the 150 V class.

THE LLC CONVERTER

General introduction to the LLC topology

The soft switching techniques typically used in LLC resonant converters enable the improvement of the efficiency in Telecom or server power supplies. These applications, due to fierce competition, demand high efficiency energy conversion (impact felt in the electricity bill) and high power density (impact felt in the real estate cost) in order to reduce the total cost of ownership of such installations.
The LLC converter had a rapid increase in adoption not only because it helps to meet the above-mentioned requirements, but also because the semiconductor industry introduced integrated-circuit controllers such as in [15]. These controllers simplify the task of designing such a complex topology (see Fig. 1). A detailed explanation of the operation modes of the LLC converter, which cannot be given here, can also be found in [15].
Simply put, the LLC converter attains zero-voltage switching in the primary-side switches M1 and M2 for a wide range of output load (see Fig. 1). This is realized through LMAG, representing the transformer magnetizing inductance. Its value depends on the primary-side switches used, as the magnetizing current must charge and discharge the primary-side MOSFETs' output capacitances regardless of the level of the output load. Both MOSFETs are switched at a 50 % duty cycle ratio. The transformer T1 is usually regarded as an ideal transformer. The inductor LR resonates with the capacitors CR1 and CR2, generating a sinusoidal current which is fed to the output to power the load. The output voltage is regulated by variation of the switching frequency around the resonant frequency defined by LR, CR1 and CR2. Switching frequencies lower than the resonant frequency give a boost to the converter output voltage while switching frequencies higher than the resonant frequency lower the converter output voltage. Details on the determination of the required values for LMAG, LR, CR1 and CR2 can be found in [15].
Inherently, a transfer of charge occurs on the primary side between the output capacitances of M1 and M2. This process is driven by the transformer magnetizing current and needs a certain amount of time depending on the output charge of the primary-side switches. Consequently, this charge-transfer time imposes a limit on the maximum switching frequency since part of the switching period is needed for the charge-transfer mechanism.

Secondary side rectification

Fig. 1 also shows the synchronous rectifying (SR) MOSFETs on the secondary side. These MOSFETs replace the formerly used secondary-side rectifying diodes. Despite the added complexity and cost they clearly increase the gain in the overall converter efficiency [16]. This improvement in efficiency pays back for the added circuitry cost by the savings obtained in the energy costs throughout the system's lifetime.
Synchronous rectification can be implemented in the LLC converter either by full-bridge or by center-tapped configurations as shown schematically in Fig. 2. The full-bridge configuration has the advantage of a simple transformer design (single secondary winding) and a bathtub-shaped effective node capacitance. This capacitance shape has the advantage of eliminating the overshoots in the SR MOSFETs as the capacitance increases with voltage. The downside of the full-bridge

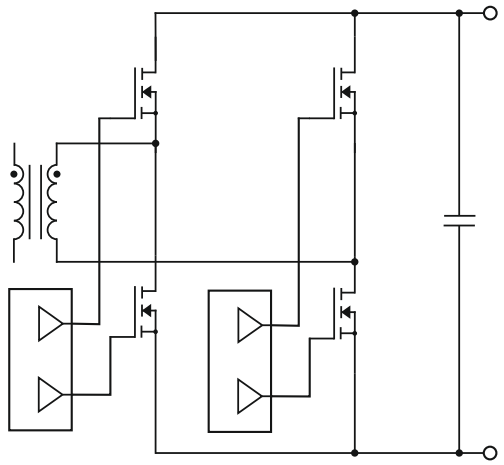

Fig. 2: Full-bridge SR configuration

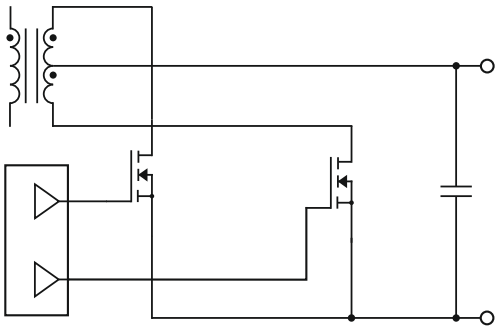

Fig. 3: Center-tapped SR configuration

configuration is its complexity and the higher cost when compared with the center-tapped approach as now two SR MOSFETs are connected in series during rectification and two half-bridge drivers are required.
In contrast the center-tapped SR configuration as shown in Fig. 3 offers the advantage of a lower circuit complexity and lower costs compared to the full-bridge configuration. As a downside it should be mentioned that a more complex transformer design consisting of two secondary windings is needed. Further there is no bathtub-shaped effective capacitance, leaving the circuit more prone to overshoots.

Requirements for the Synchronous Rectification MOSFET

The increase in power density yields more compact systems. This lowers the cost of ownership by a reduction of the real estate required by installations, especially in urban areas. The soft-switched LLC converter greatly contributes to achieving this goal. It has virtually no primary-side switching losses and the switching frequency can be increased as much as necessary in order to reduce the size of the reactive elements (magnetics and capacitors). This enables a clear reduction of the converter volume.
However, aside from increased losses in the magnetics, which are not covered here, there are also potentially higher losses contributed by the SR MOSFET. These losses are linked to the MOSFET output capacitance and consequently will increase with the operating frequency. The mechanism behind this loss contribution lies in the transfer of the output charge from one SR MOSFET to the other during the switching phase (i.e. SR1 is turned-off while SR2 is going to be turned-on and vice versa). The transition of the charge that is stored in the output capacitance of the MOSFET needs some time, and within this transition no energy is transferred to the output. In order to maintain the DC output current level, the rectifier current peak needs to rise to compensate. However, this higher current through the SR MOSFET will lead to higher conduction losses. As such a minimized output capacitance for the SR MOSFET not only affects the height of voltage overshoots [18] but may also limit the efficiency at higher operation frequencies.

POWER MOSFET DEVICE STRUCTURES

Charge-compensation using a field-plate

Trench power MOSFETs emerged about 20 years ago and were quickly established as one of the world's most ubiquitous semiconductor devices [19]. Field-plate trench power MOSFETs entered the market about one decade later and developed into a kind of standard technology for fast-switching devices.
Fig. 4 indicates the main difference between the two device structures. In a field-plate type device, the isolated field-plate provides mobile charges which serve to compensate the drift region donors under blocking conditions. Compared to a device using a simple planar pn-junction, the electric field now also has a component in the lateral direction. The application of a field-plate leads to an almost constant field distribution in the vertical direction since the ionized dopants in the drift region are laterally compensated by mobile carriers in the field-plate.
By this measure the necessary drift region length is reduced and the allowed drift region doping for a given breakdown voltage can be increased. Both effects contribute to the significantly reduced area-specific on-resistance. Since the field-plate electrode is connected to the source electrode of the MOSFET and the gate is formed by a separate electrode, such a device also offers a low gate-charge at the same time.

Overview of investigated device structures

To improve the overall efficiency, in most applications both the conduction and the switching losses need to be minimized at the same time in order to meet the efficiency targets at low and medium load conditions. Within a given technology this imposes a contradictory

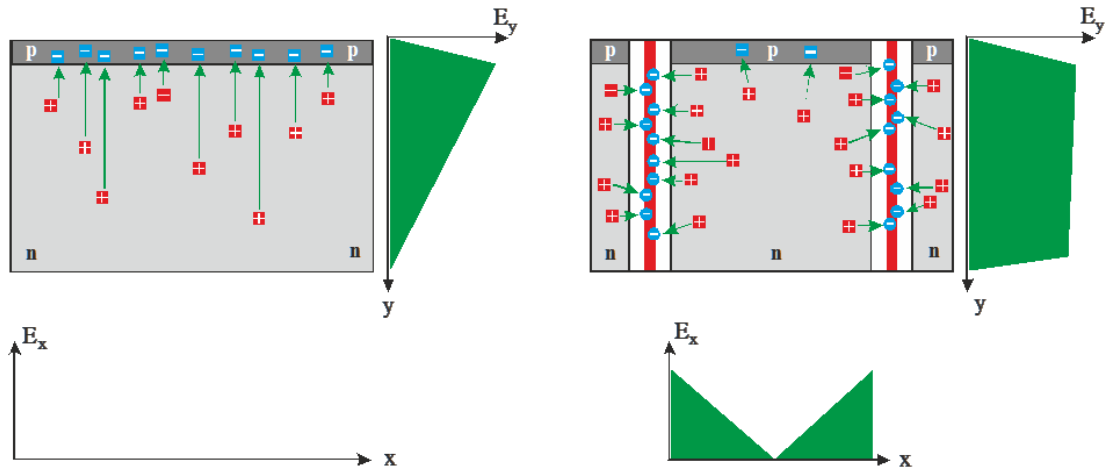

Fig. 4: Comparison of the electric field distribution for a simple pn-junction and for field-plate structure

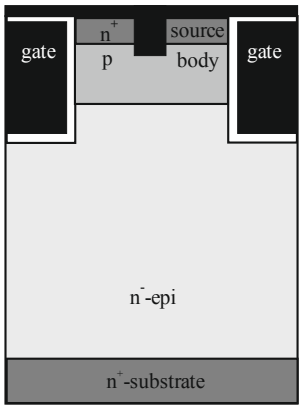

Fig. 5: Schematic cross section of a vertical trench power MOSFET

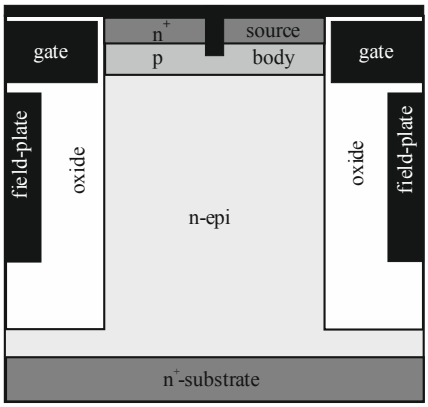

Fig. 7: Schematic cross section of a charge-compensated device designed for a higher blocking voltage

requirement and is one of the key drivers for new device generations.

The introduction of the trench power MOSFET as depicted in Fig. 5 enabled a noteworthy pitch reduction linked to clear reduction of the on-resistance. This was mainly realized by the elimination of the parasitic JFET formed by the p-well body regions. It is worthmentioning that the general Figure of Merit $FOM_G = R_{DS(on)} \bullet Q_G$ and the Switching Figure of Merit $FOM_{GD} = R_{DS(on)} \bullet Q_{GD}$ were also improved.

The arrival of charge-compensated trench power MOSFETs based on an insulated field-plate marked a further milestone. However, the device design became more challenging in order to avoid an unintended increase of the Figure of Merit with respect to output charge $FOM_{OSS} = R_{DS(on)} \bullet Q_{OSS}$ without compromising the ruggedness of the device [18].

Also the extension of the breakdown voltage range into the medium-voltage range of 150 V and beyond imposed a number of challenges related to manufacturability issues such as a too high wafer bow or stress-induced cracks [14]. Therefore, in a first step, the required increase of the blocking capability was realized by an additional second lower-doped drift region below the actual compensation structure as illustrated in Fig. 6. One advantage of this approach is the option to reutilize an existing cell, however the expected area-specific on-resistance will be higher as only a part of the structure is charge-compensated.

The second option to gain a higher blocking capability is found in a complete appropriate redesign of the device. Among other measures, the trench depth as well as the thickness of the field oxide layer inside the trench must be increased which imposes the need to address the already mentioned manufacturability issues. The outcome is a device which offers the best area-specific on-resistance as the full drift-region length is compensated. Furthermore, this concept enables the best options to target the optimization of the device with respect to different application requirements. Fig. 7 gives a schematic representation of this device structure.

Properties of the different device structures

For the further discussion it is important to evaluate the realized device performance at the product level. This includes the package contribution to the overall on-resistance of the device. The comparison presented in this work is done for fully processed devices with a nominal blocking voltage of 150 V.

Fig. 8 compares the on-resistance in different package types. All devices are best-in-class devices. This means

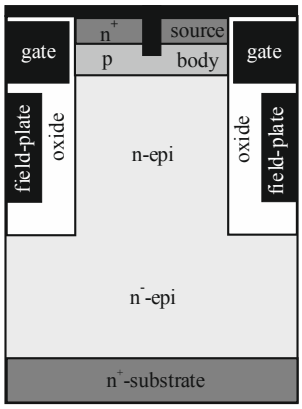

Fig. 6: Schematic cross section of a charge-compensated device with an additional drift layer

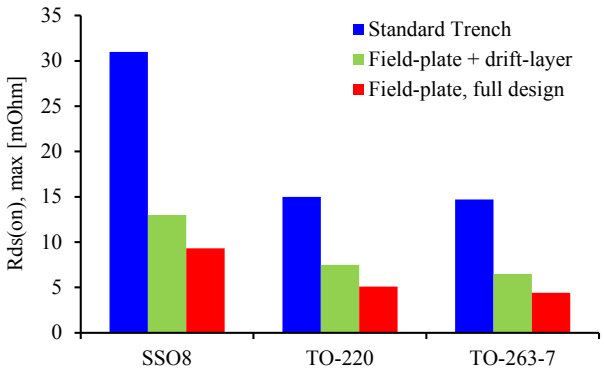

Fig. 8: Comparison of the product on-resistance of the 150 V devices with respect to the discussed concept approaches

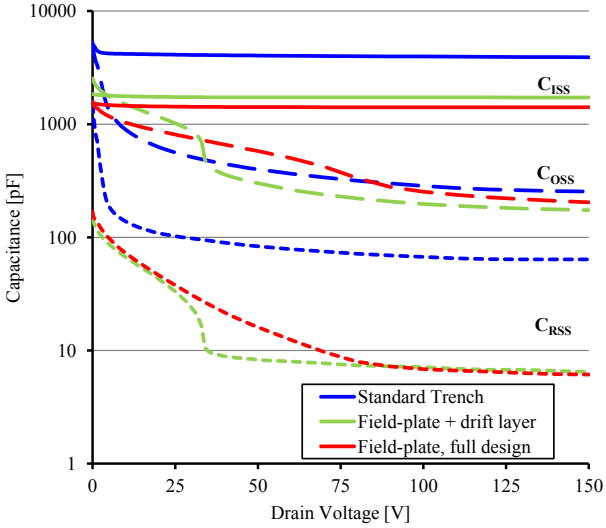

Fig. 9: Comparison of the input, output and reverse transfer capacitance for an equivalent on-resistance of ca. 14 mΩ

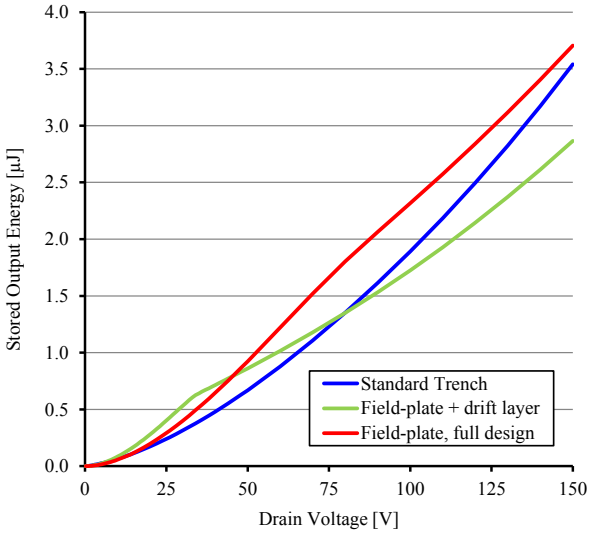

Fig. 11: Comparison of the stored output energy dependencies for an equivalent on-resistance of ca. 14 mΩ

that for each package type the largest possible chip area which fits into it is used. As is to be expected the device based on a field-plate and a full redesign shows the lowest on-resistance for the product. This figure also confirms the impressive reduction in the conduction losses that is realized by the application of the charge-compensation principle.

With respect to the device performance in the discussed application the capacitances are of interest. For a fair comparison in the test board, the on-resistance of the power MOSFET must be comparable. Due to layout constraints, the test board requires a MOSFET with an overall on-resistance of approximately 14 mΩ. To realize this value as closely as possible, two devices are paralleled in the case of the standard trench device as well as in the case of the MOSFET employing a field-plate with additional drift layer. In the case of the fully redesigned field-plate device, only one MOSFET is needed. Unfortunately it was not possible to realize an exact match due to the chip sizes available. This translates into a 7 % lower on-resistance for the standard trench device and a 14 % higher on-resistance for the field-plate device with additional drift layer.

Fig. 9 compares the dependencies of the capacitances on the drain-source-voltage. Obviously, the standard trench device shows a higher input and reverse-transfer capacitance. This can translate into a slower switching speed. In case of the output capacitance, the shape of the dependence is specific to the device structure. The standard trench device has a much higher capacitance value at low drain voltage while both of the charge-compensated devices show some non-linearity in the dependence. This is especially evident in the case of the structure using the additional drift-layer approach; here the step in the capacitance-dependence is also present in the reverse-transfer characteristic.

Fig. 10 shows how the output capacitance characteristics translate into the output charge Q_{OSS} dependency while Fig. 11 reflects the corresponding dependency for the stored output energy E_{OSS}. Most obviously, the kink in the output capacitance shape of the field-plate device with additional drift layer also impacts the shape of the Q_{OSS} and E_{OSS} dependencies.

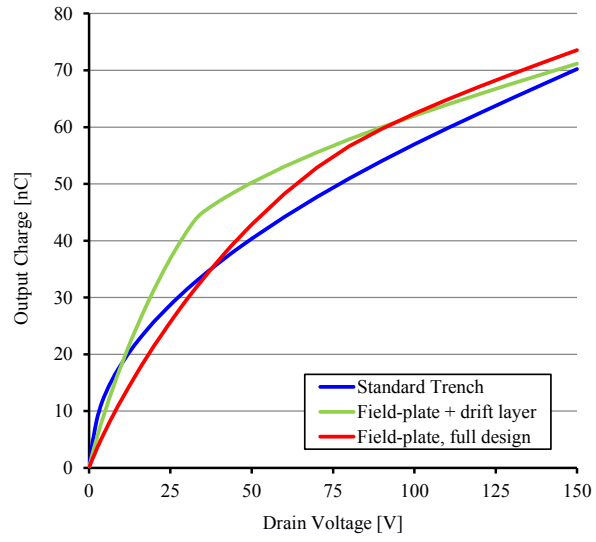

Fig. 10: Comparison of the output charge dependencies for an equivalent on-resistance of ca. 14 mΩ

RESULTS

Circuit simulation results

Simulation setup. A SPICE simulation circuit has been set up for evaluation purposes as shown in Fig. 12. A simple basic control loop has been implemented to keep the steady-state output voltage constant regardless of the device technology being tested. The control loop compensation has been implemented following the equation set presented in [20].

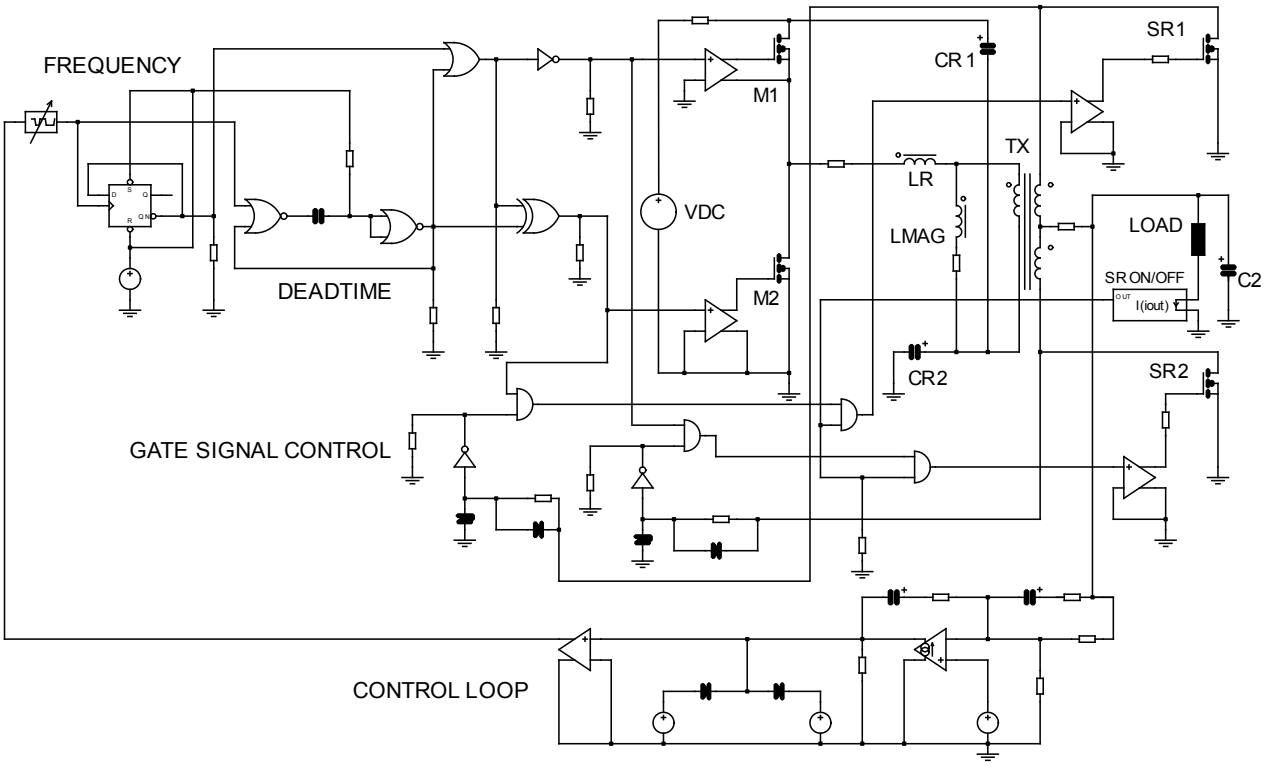

Fig. 12: Basic circuit simulation schematic representing the investigated LLC converter

Simulation results. Fig. 13 shows the simulated drain-source voltages of the SR MOSFET SR1 and SR2 as well as the current that flows from the transformer center-tap into the output capacitor C2 and the load.
Fig. 13 indicates that the rectified current has twice the frequency (270 kHz) than the drain-source voltage of the SR MOSFET.
Fig. 14 zooms into the waveforms during the drain-source voltage transition phase. It can be seen that the transfer of the output charges from one SR MOSFET to the other takes about 150 ns. As already discussed before there is no energy transfer to the output during this time.
The converter currently used has switching frequency of 135 kHz, translating into the period of the rectified current being 3.85 µs long. Accordingly, the charge-transition time lasts only 3.9 % of this period and the impact of the output-capacitance charge-transfer related losses might be still negligible. However, assume one wants to take more advantage of the benefits offered by the used soft-switching topology. If, for example, the switching frequency increases to 1 MHz, then these charge-transition time will extend over a longer fraction of the period.
To maintain the same DC output current level the rectified current peak must now become higher in order to compensate for the lost time in the transition phase. This will increase the rectified current RMS value and also the linked conduction losses in this phase of operation.

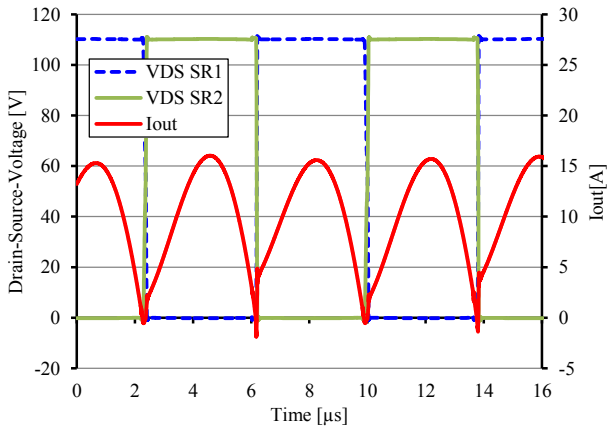

Fig. 13: Simulated waveforms for the drain-source voltage of the SR MOSFET and the rectified load current

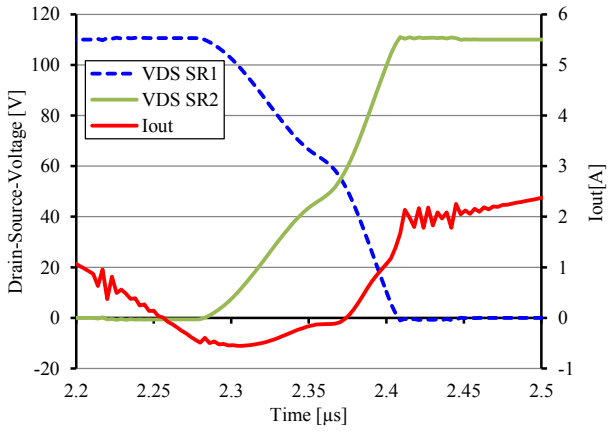

Fig. 14: Zoomed view into the drain-source voltage transition phase and the rectified load current

Experimental results

Test setup. The benefits of the combination of soft-switching techniques with synchronous rectification with respect to their use in either Telecom rectifiers or server power supplies can be best experienced in a 3 kW interleaved LLC converter with an output voltage of 54.5 V [17]. This output voltage requires the use of MOSFET with a blocking capability of 150 V in the synchronous rectifier stage.
Such a converter is used for the experimental investigations. The test board, as shown in Fig. 15, is composed of two 1.5 kW LLC converters, each with an isolated center-tapped secondary-side transformer configuration. To address the on-resistance of the available test devices as well as possible and in order to be able to compare the device sets of approximately equivalent on-resistance, only one LLC converter has been kept active. This selection can be easily performed in the evaluation board graphical user interface. In addition, the output power has been limited to 545 W (10 A) for the same reason. The point at which the synchronous rectification is going to be activated (~5.7 A) has been kept unchanged. As a result it is also possible to study the difference in efficiency due to operation in synchronous rectification mode.

Application test results. The test setup just described allows the following tests to be performed:

- efficiency measurement
- drain-to-source voltage measurement for the synchronous rectifier MOSFET
- gate-to-source voltage measurement for the synchronous rectifier MOSFET

The tests are run using the three previously discussed device sets:

1. two standard trench power MOSFET per transformer secondary branch
2. two field-plate trench power MOSFET employing an additional drift layer per transformer secondary branch
3. one field-plate trench power MOSFET based on a full redesign per transformer secondary branch

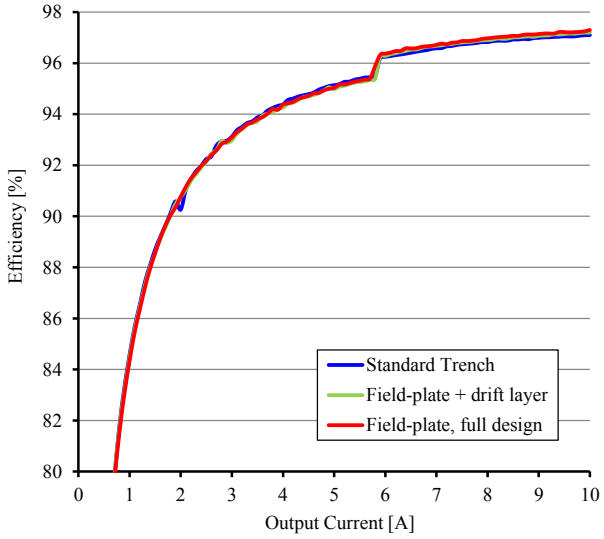

Fig. 16: Absolute converter efficiency comparison with respect to the different device technologies

Figs. 16 and 17 illustrate the efficiency comparison for the different devices. Fig. 16 shows the absolute efficiency values.
It can be seen that the efficiency difference, depending on whether synchronous rectification is used or not, already amounts to 1 % even at a fairly low output current of 5.7 A. The difference becomes even greater at higher output current levels. Furthermore, while synchronous rectification is active, second order differences in efficiency can still be seen which can be related to the different device structure properties.

Fig. 15: The test board being used for the investigations in this work

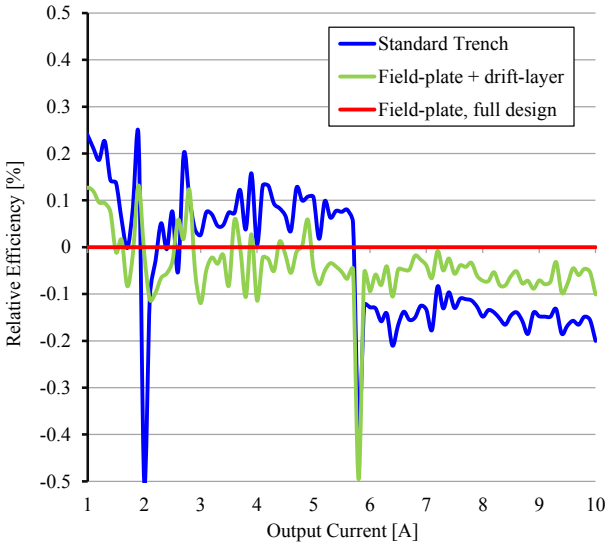

Fig. 17: Relative converter efficiency comparison with respect to the different device technologies

Fig. 17 details the difference in the efficiency for all three devices with respect to the field-plate device technology based on a full design as reference. Also here the activation of synchronous rectification can be clearly seen and is additionally indicated by a significantly reduced variation in the derived values. Due to the relatively large fluctuation of the values it is difficult to evaluate the efficiency differences at lower output currents where the body diode of the MOSFET is used. One may suggest that the standard trench device gives a slightly better efficiency in this range. An explanation could be that the forward voltage of the body diode is lowest for this device as it clearly uses the largest semiconductor area due to the higher area-specific on-resistance. In the case of activated synchronous rectification the efficiency is best for the field-plate device with full redesign. However, the differences are small and approaching the resolution limits of the test setup.

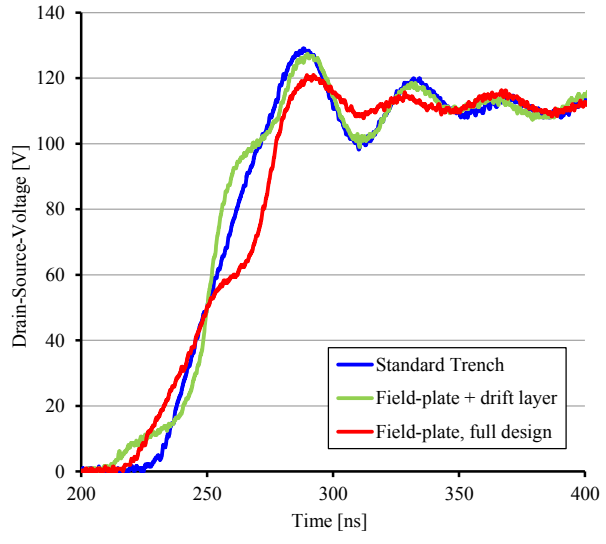

Fig. 18: Comparison of the SR-MOSFETs drain-to-source voltages during drain voltage upswing

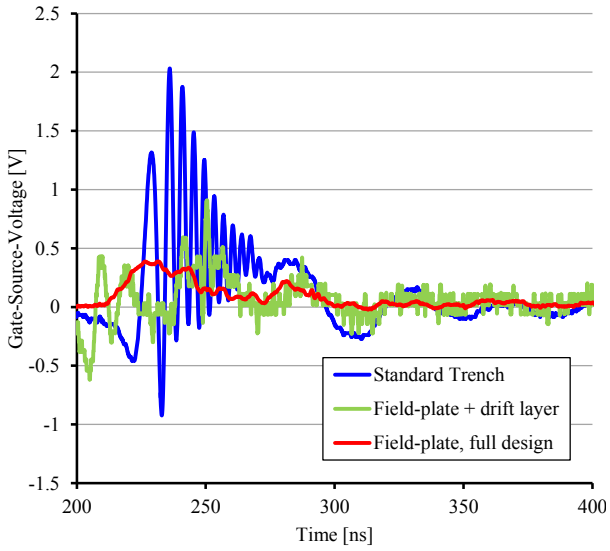

Fig. 19: Comparison of the SR-MOSFETs gate-to-source voltages during drain voltage upswing

The fact that the efficiency is best for the field-plate device with full redesign is a good indication that the stored output energy E_{OSS} is not dissipated at every switching cycle and therefore does not impact the efficiency. Otherwise the efficiency for this device should be slightly below the other two devices as the measured E_{OSS} is somewhat higher in this case (see Fig. 11). Instead, the energy keeps swinging from one SR MOSFET to the other and the losses generated during switching only relate to the losses in the connecting copper traces or in the secondary transformer windings.

Figs. 18 and 19 show the comparison of the SR-MOSFETs drain-to-source (V_{DS}) and gate-to-source (V_{GS}) voltages for the transition into the blocking condition (turn-off). The most advanced technology using a field-plate with full design yields 10 V less voltage overshoot compared to the two other technologies. The standard trench MOSFET causes the highest overshoot. As depicted in Fig. 19 it is also the standard trench device technology that generates a higher induced gate-to-source voltage ringing during the drain voltage upswing. This is a consequence of the higher feedback due to the clearly larger reverse transfer capacitance. Still, the induced gate voltage is not high enough to cause an unwanted turn-on event which would have a negative impact on the efficiency.

CONCLUSION

In this work the impact of the synchronous rectification stage on the overall efficiency of a resonant LLC converter is investigated. The study is based on both experimental measurements and circuit simulations and includes the use of different device structures in the secondary-side rectifier stage. All three device structures are introduced and the resulting properties are discussed.

Due to the resonant nature of the LLC topology, typical switching losses are eliminated to a large degree. Especially the losses due to the stored-charge in the output capacitance of the power semiconductors are avoided as this charge swings from one synchronous rectifier MOSFET to the other one instead of being dissipated during a hard turn-on of the device. During the charge transition, no energy transfer to the rectifier output is possible. This is compensated by a higher rectifier current peak in order to maintain the output current level, and it is this higher current peak that generates additional conduction losses. In consequence it is not the energy stored in the output capacitance that contributes to the losses. This is confirmed by the measurement results that do not reveal an impact of the output charge on the overall efficiency.
Still, the aforementioned additional conduction losses are related to the output charge as its value defines the charge-transition time needed. It is expected that this loss contributor will become significant if higher switching frequencies are going to be used. In the available test setup, the operation frequency is limited by the output charge of the primary-side switches where the same loss mechanism applies as described before. To further study the described effect and its dependencies, a new test bench needs to be developed that offers the required degree of freedom.
For the time being, the different properties of the investigated MOSFET structures are mainly seen in the gate ringing and in overvoltage peaks in the drain-source voltage, meaning that the EMI behavior is affected rather than the converter efficiency.

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