

650 V SiC Trench MOSFET for high-efficiency power supplies

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Keywords

Power semiconductor device, Silicon Carbide (SiC), MOSFET, Reliability, Power Supply

Abstract

This work introduces a new SiC Trench MOSFET technology with 650 V nominal blocking voltage. The technology is tailored to address the needs of power supplies in the power range from several hundred watts to some tens of kilowatts including server and telecom switch-mode power supply (SMPS), solar inverters and electric-vehicle charging. These applications benefit strongly from power semiconductors that serve high switching frequencies, enable fast switching under hard-switching conditions, and provide low conduction losses as well as a small output and reverse-recovery charge. The MOSFET technology introduced enables new, highly efficient topologies such as the full-bridge totem-pole in the power-factor correction (PFC) stage. The paper further presents long-term reliability data and performance evaluations indicating a possible absolute PFC stage efficiency of 99 %. Such an efficiency is essential to gain an overall system efficiency of 98 %.

1. Introduction

Power supplies for target applications covering a wide range from telecom rectifiers through servers to solar inverters or electric vehicle chargers share the need for high efficiencies in order to minimize the overall energy consumption and the total cost of ownership. For example, soft-switching techniques as typically employed in LLC resonant topologies allowed for a significant improvement of the efficiency in power supplies used for telecom rectifiers or servers [1-3]. However, these techniques reduced losses only on the primary side. Secondary-side rectification-related losses remained to be addressed. The replacement of the traditionally used diode rectifiers by power MOSFETs acting as synchronous rectifiers (SR) dramatically reduced the rectification conduction losses and enabled a further increase of the converter efficiency and the power density [4]. In this way the DC-DC conversion efficiency has been significantly improved, moving attention again to the AC-DC conversion of the PFC stage.

Power factor correction is one of the most important parts of an SMPS especially for the power range of 100 W and higher. In the past years, the worldwide power consumption has increased dramatically with power supplies for server and telecom applications being a substantial contributor to this increase. SMPS of highest efficiency are easily achievable by the use of wide bandgap power semiconductors in combination with different topologies than presently used. Now one needs to

understand the limiting factors for achieving 98 % system efficiency with the present PFC designs. Here, especially the traditional input bridge rectifier comes into focus as it represents the biggest loss contributor.

2. The full-bridge totem-pole topology

2.1. State of the art power supplies

Commonly used power supplies consist of the main building blocks as depicted in Fig. 1. The AC-DC part typically consists of an input bridge rectifier combined with a boost PFC stage with an output voltage of typically 400 V. The DC-DC part typically employs an LLC resonant stage and a center-tapped synchronous rectifier on the secondary side but alternative DC-DC topologies are possible.

Such power supplies are usually designed for a universal input voltage range of 85 - 265 VAC. As the input voltage covers a range of larger than 3:1, the RMS input current varies accordingly. Consequently, the I^2R conduction losses vary over a 10:1 range for just a single load condition, imposing a serious challenge for the optimization and selection of both the MOSFET P1 and the Schottky rectifier D1. The typical operating frequency is limited to 70 kHz to keep the fundamental and 2nd harmonic below 150 kHz due to EMI reasons. A higher operating frequency also clearly increases the switching losses. The typical control mode is the Continuous Conduction Mode (CCM) as here the ripple current losses and switching losses are well balanced. The PFC stage may also be operated in Discontinuous Conduction Mode (DCM) or Critical Conduction Mode (CrCM) at the cost of a much higher ripple current while at the same time enabling quasi Zero Voltage Switching (ZVS) for reduced switching losses. However, the input bridge rectifier is in all cases the most dominant source of losses, causing an efficiency loss between 1 and 2 %. Obviously, even a perfect zero loss MOSFET P1 would not be able to compensate for these losses. This is also clearly visible from the loss breakdown for the boost PFC stage shown in Fig. 2. For a further increase in the absolute efficiency of the complete power supply it is therefore necessary to move to other topologies.

2.2. Topology options for the power factor correction stage

2.2.1. Dual Boost PFC and H4 PFC

Several topologies exist that can achieve higher efficiency and make use of superjunction MOSFETs, namely the Dual Boost PFC and the H4 PFC. The basic schematics of both topologies are depicted in

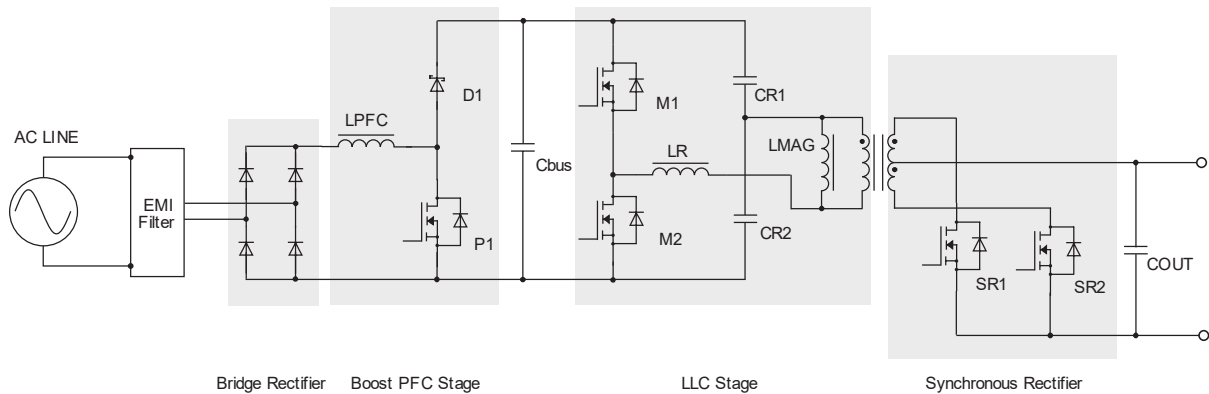


Fig. 1: Basic schematic of a commonly used power supply with input bridge rectifier and boost PFC stage

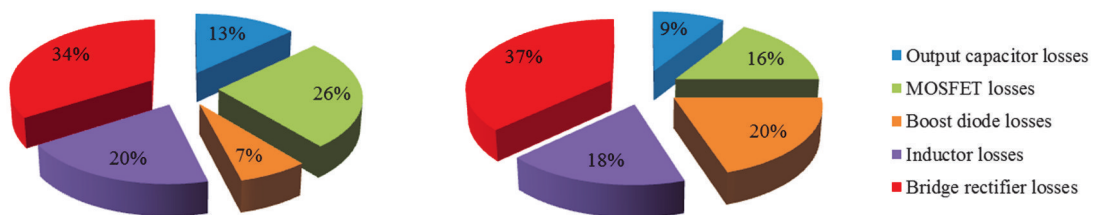


Fig. 2: Loss breakdown for a Boost PFC stage at low input voltage 85 V (left) and at standard input voltage 230 V (right)

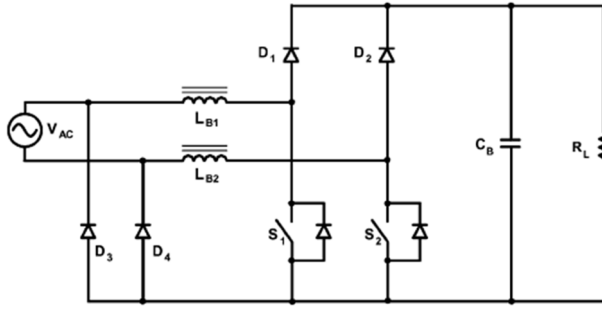


Fig. 3: Schematic of a Dual Boost PFC [5]

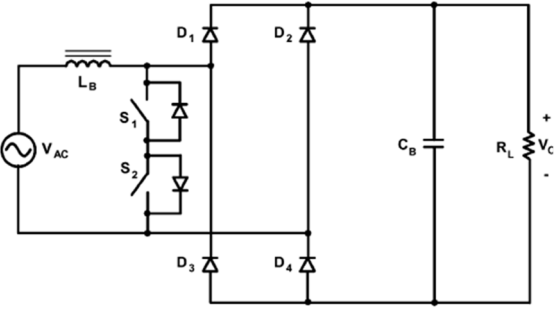


Fig. 4: Schematic of an H4 PFC [5]

Fig. 3 and Fig. 4. The functional principle of these topologies are very well described in the literature [5,6]. Based on extensive simulation work it is possible to derive the peak efficiency for both topologies.

As indicated in Fig. 5, a peak efficiency of 98.8 % can be expected for both the Dual Boost PFC and the H4 PFC. This translates into a realistic expectation for the overall system efficiency level of 97.5 %, assuming synchronous operation is used. It is not possible, and due to cost reasons, not feasible, to use these topologies to target PFC stage efficiencies of 99 % or higher.

2.2.2. Totem-Pole PFC

One promising topology is the full-bridge totem-pole topology as shown in Fig. 6. This topology works bridgeless and completely eliminates any diode-related losses [7]. It is a rather simple topology which can be operated in many different control modes [8] including CCM, DCM, CrCM etc. and is intrinsically capable of providing a bi-directional power flow. Beside its simplicity this topology provides the highest practically achievable efficiency. However, the full-bridge totem-pole configuration imposes some serious challenges at least to a part of the power semiconductors.

Fig. 6 indicates the usage of two SiC MOSFETs in the first half-bridge of the PFC stage. This half-bridge must be operated at high switching frequencies between 45 kHz and 100 kHz with one transistor working as a boost switch and the other as a synchronous rectifier. Operation in Continuous Conduction Mode requires switches with the lowest-possible reverse-recovery charge Q_{RR} and an output capacitance dependency on the drain voltage that does not exhibit sharp drops typically seen for superjunction (SJ) devices. It is also beneficial to have a much lower output charge Q_{OSS} . Wide-bandgap power transistors like SiC MOSFETs act as enablers for this high performance topology. Note that the second half-bridge runs only at low frequency for half-cycle commutation, e.g. at the power grid frequency of 50 Hz. Here, SJ devices are a perfect choice as they can easily provide the required low on-resistance.

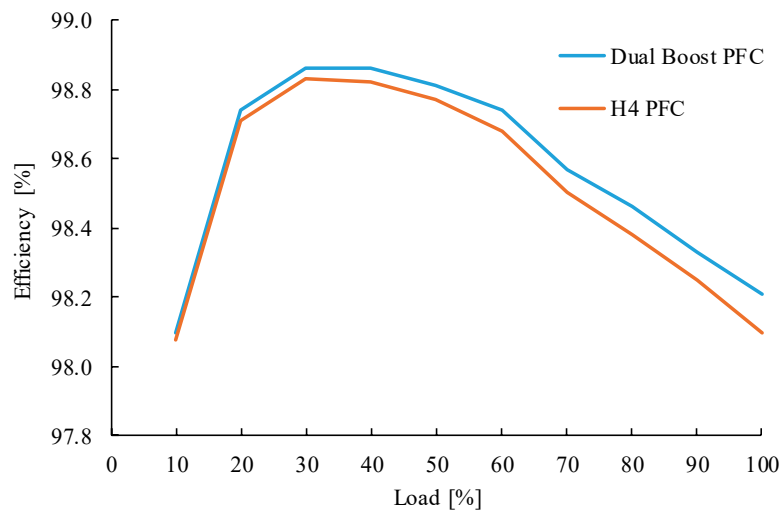


Fig. 5: Efficiency of Dual Boost PFC and H4-PFC stage ($V_{in} = 230$ VAC, $P_{out} = 3$ kW, $f_{sw} = 45 - 65$ kHz, $V_{out} = 400$ VDC)

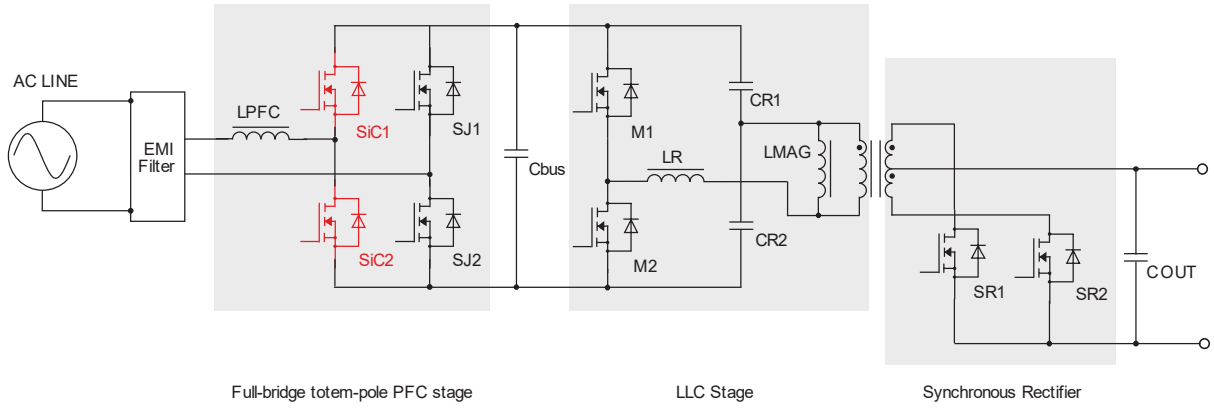


Fig. 6: Basic schematic of an advanced, highly-efficient power supply with full-bridge totem-pole PFC stage eliminating the standard input-bridge rectifier

2.3. Operation principle of the CCM Totem Pole PFC

The CCM Totem Pole PFC is in principle divided into four phases over one AC cycle and two phases per positive and negative cycle of the input voltage. Fig. 7 illustrates the different phases of the operation.

2.3.1. Positive AC cycle

The low ohmic SJ MOSFET S2 is continuously conducting. During the magnetizing phase the SiC MOSFET Q2 is turned on and operates like in a standard PFC and is needed in order to magnetize the PFC choke. After Q2 is turned off, the body diode of Q1 is conducting and finally actively turning on Q1 the demagnetizing phase starts. During this time Q1 acts as a synchronous boost.

Exactly during the time when the synchronous boost turns off, there is a short period in which the body diode of Q1 is conducting again and Q2 is actively turned on which leads to a hard commutation on the conducting body diode. This means this hard commutation is present in every switching cycle on one of the SiC MOSFETs, therefore the switching energy and the losses increase during this turn on based on the Q_{RR} and the Q_{OSS} .

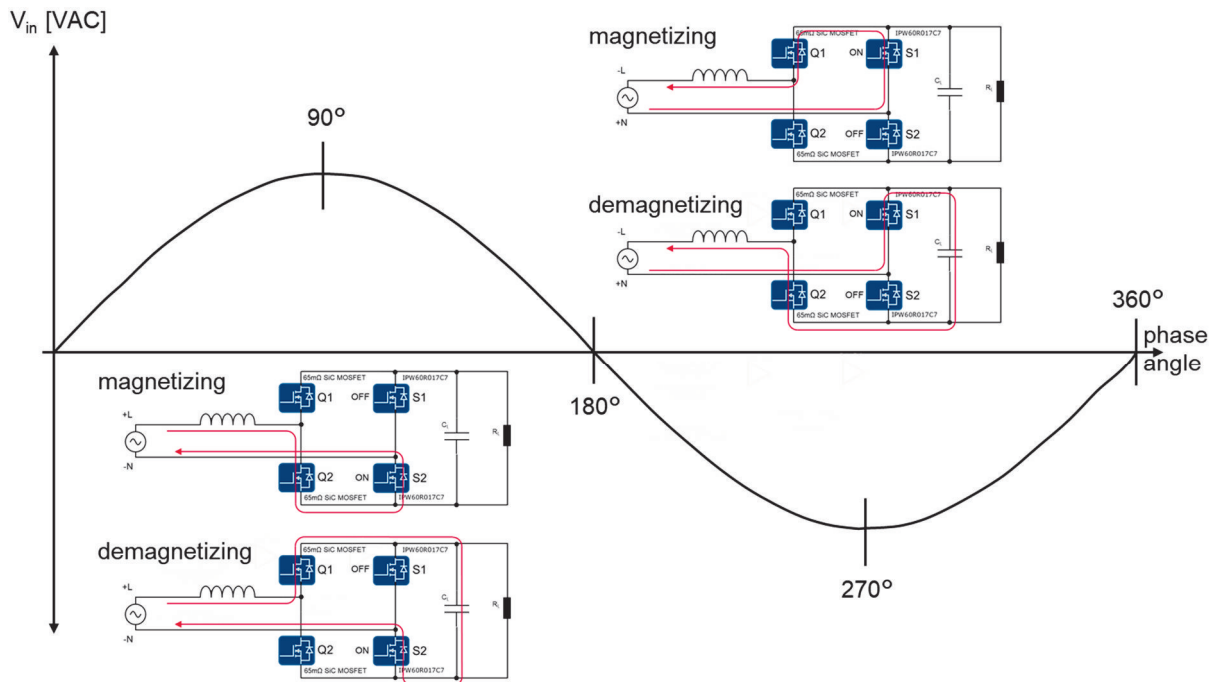


Fig. 7: CCM Totem Pole PFC principle of operation depending on the AC phase

2.3.2. Negative AC cycle:

The negative AC cycle operation is completely the same as the inverted positive AC cycle. In this case the low ohmic SJ MOSFET S1 is continuously conducting. During the magnetizing phase the SiC MOSFET Q1 is turned on and operates like in a standard PFC and is needed in order to magnetize the PFC choke. After Q1 is turned off, the body diode of Q2 is conducting and finally actively turning on Q2 the demagnetizing phase starts. During this time Q2 acts as a synchronous boost.

As can be seen in this topology, the already mentioned lowest possible Q_{RR} and Q_{OSS} are required as during every switching cycle there is a hard commutation on the conducting body diode. For this reason the SiC MOSFET and its related technology parameters are the optimum choice for achieving 99 % efficiency. Therefore, the next chapter is going to describe the SiC MOSFET technology before stepping in to the results in the application testing.

3. Device Concept and Reliability

3.1. SiC MOSFET design

Wide band-gap semiconductors based on silicon-carbide are most attractive for power devices due to their low losses, improved temperature capability and high thermal conductivity. However, while the use of silicon carbide promises many advantages thanks to being a wide-bandgap material, there are also some noteworthy differences to silicon leading to a number of challenges when doing a SiC MOSFET based on the 4H-SiC polytype as the most prominent silicon-carbide polymorph used for power semiconductor devices:

- SiC has a higher surface density of atoms per unit area compared to Si, resulting in a higher density of dangling Si- and C- bonds and carbon clusters at the interface, defects located in the gate oxide layer near to the interface may appear in the energy gap and act as traps for electrons [9]
- The thickness of thermally grown oxides strongly depends on the crystal plane and doping level
- SiC devices allow much higher drain-induced electric fields in the blocking mode compared to their Si counterparts that require a limitation of the electric field in the gate oxide to maintain reliability [10]
- SiC devices show a higher Fowler-Nordheim current injection compared to Si devices due to a smaller barrier height, consequently the electric field on the SiC side of the interface must be limited [11,12]

Consequently, one challenge of SiC MOSFETs is the low electron mobility at the SiO_2/SiC interface due to carbon related interface defects. Due to electron scattering and trapping at such point defects at the interface, the channel mobility being in the range of 5 – 50 cm^2/Vs is typically only a fraction of the bulk mobility of ca. 400 cm^2/Vs (the value at a bulk doping level equal to the channel doping) [13]. Another challenge of today's SiC devices is the 4° off-axis tilt of commercially available SiC substrates. It is a consequence of the need for epitaxial layer growth, and thus cannot be avoided. Due to the tilt, the wafer surface does not perfectly coincide with the (0001) crystal c-plane, causing

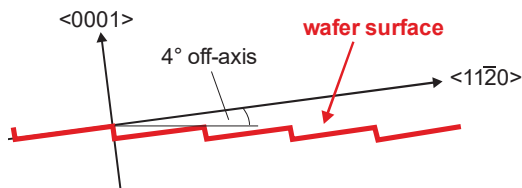


Fig. 8: Schematic illustration of the 4° off-axis cut of 4H-SiC wafers

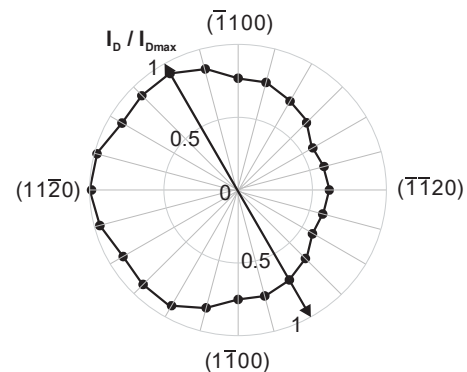


Fig. 9: Relative channel mobility for various trench planes of 4H-SiC on-axis substrate [14]

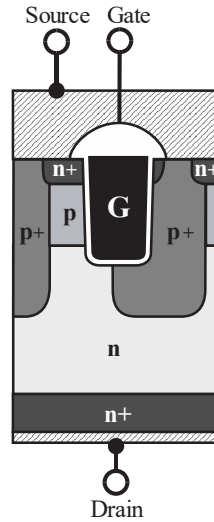


Fig. 10: SiC Trench MOSFET concept with an asymmetric channel

increased surface roughness and steps when fabricating a MOS structure at the wafer surface. This situation is illustrated in Fig. 8. However, this off-axis cut is not only a problem of devices using a lateral channel but also affects trench MOSFET technologies, as a vertically etched trench will generally have side walls with different roughness, performance and reliability. It was experimentally shown that the vertical channel mobility strongly depends on the crystal plane, and a factor of almost two between worst and best channel mobility must be expected, as indicated in Fig. 9 [14]. A suitable post-oxidation annealing step like a nitric oxide annealing can reduce the interface state density significantly [15]. The conditions of the post oxidation anneal (POA) also affect the stability of the threshold voltage. An optimized POA provides high channel mobility and high threshold voltage stability at the same time. In general, the optimal passivation process conditions are different for each 4H-SiC crystal face.

The limitation of the electric field strength in blocking state must be realized by appropriate device design measures like a buried shielding region.

Fig. 10 gives a schematic cross section of the cell concept that is used for the proposed 650 V device. The active channel is fabricated in a way that it is exactly oriented along the a-plane $\langle 11\bar{2}0 \rangle$ which gives the best channel mobility and lowest interface trap density. Hence the 2nd trench sidewall does not coincide with a crystal plane and thus is not used as an active channel. The gate oxide is protected by deep p-wells that are connected to the source electrode at the semiconductor surface. This leads to a very compact cell design and in combination with the high channel mobility of the a-plane to a low area-specific on-resistance. This allows the device to be easily driven by the commonly used gate-source voltage of $V_{GS} = +15$ V.

The 650 V MOSFET cell is widely identical to the 1200 V device as introduced previously [16]. Differences in the device design represent only those changes necessary to meet the desired breakdown voltage and include adaptations to the drift region and to the edge termination structure. The trench design and the gate oxide process remained untouched. Therefore the 650 V device offers the same high reliability as the 1200 V device, as discussed in more detail in the following chapter.

3.2. Gate oxide reliability

This chapter discusses gate oxide breakdown as a failure mechanism in SiC power devices. The fundamentals are essentially the same for Si and SiC, however some details differ. In the following we will highlight the differences and demonstrate that the resulting reliability challenges for SiC MOSFETs can be managed if proper design and screening measures are put in place.

The challenge of the gate oxide reliability of SiC MOS devices is to guarantee a maximum failure rate of less than 1 FIT under given operation conditions in industrial applications. Since the intrinsic quality and properties of SiO₂ on SiC and on Si are almost identical, Si MOSFETs and SiC MOSFETs of the same area and oxide thickness can withstand roughly the same oxide field for the same time. Of course this is only valid if the devices do not contain defect-related impurities, i.e. extrinsic defects.

3.2.1. Definition of critical extrinsics

In contrast to Si MOSFETs, SiC MOSFETs exhibit a much higher extrinsic defect density in the gate oxide. One reason for this is the higher defect density of the SiC substrate [17]. Extrinsic defects as depicted in Fig. 11 behave like small spots with a locally thinner oxide. Therefore the oxide experiences a higher stress field at the same applied gate voltage. Devices with extrinsic defects breakdown earlier in comparison to devices that are free of defects. Defect free devices will fail much later due to intrinsic wear out. Typically, intrinsic failure times are far out of reach under normal application conditions if the bulk oxide thickness is sufficient. As a consequence, the oxide FIT rate within the typical chip lifetime is exclusively determined by extrinsic defects, the so-called “critical extrinsics”. A critical extrinsic can be defined as a defective spot in an active device which reveals breakdown at one point in time during the required product lifetime of a certain application. In this context the assessment whether an extrinsic is critical or not is not only determined by the physical nature of the defect itself, e.g. its electrical oxide thickness. It is also determined by the mission profile of the application, e.g. the gate use voltage $V_{G,use}$, the junction temperature T_J and/or the targeted lifetime of the product.

Consequently, one specific extrinsic may be critical for one application that is running at $V_{G,use1}$ but may be uncritical for another application which is running at $V_{G,use2}$, provided $V_{G,use2} < V_{G,use1}$.

The challenge to make the gate oxide of silicon carbide MOSFETs reliable is to reduce the number of critical extrinsics from an initially high number at the end of process (e.g. 1 %) to an acceptable low number when the products are shipped to the customer (e.g. 10 ppm). One well-established way to achieve this is to apply an electrical screening [10].

3.2.2. Electrical screening of critical oxide extrinsics

During electrical screening, each device is subjected to a gate stress pulse with defined amplitude and time. The stress pulse voltage is selected to destroy devices with critical extrinsics while devices without extrinsics or with only non-critical extrinsics survive. Devices that do not pass the screening test are removed from the distribution. In this way a potential reliability risk is converted to yield loss. The efficiency of the electrical screening (i.e. the reduction of the field-failure rate due to screening) depends on the ratio of screening voltage $V_{G,scr}$ to use voltage $V_{G,use}$. The relation is derived from the linear E-model [18-20] (also called thermochemical or Eyring model). Fig. 12 shows an exemplary correlation plot. The higher the screening voltage with respect to the use voltage, the fewer devices with critical extrinsics remain after screening. One may define the field-failure probability after screening F_{SCR} as the product of original failure probability without electrical screening F_0 times the screening efficiency scr_eff :

$$F_{SCR} = F_0 \cdot scr_eff \quad (1)$$

To reduce the number of critical extrinsics, and thus the field-failure probability, by more than three orders of magnitude, e.g. from 1 % to less than 10 ppm, one has to screen devices with approximately three times the use voltage. In this way Si-like gate oxide FIT rates can be achieved [21]. To be able to stress devices with equal to or more than three times the use voltage, the bulk gate oxide needs to have a certain minimum thickness. In case the gate oxide thickness is too low, devices either fail intrinsically during screening because of wear-out or show a degraded threshold voltage and channel

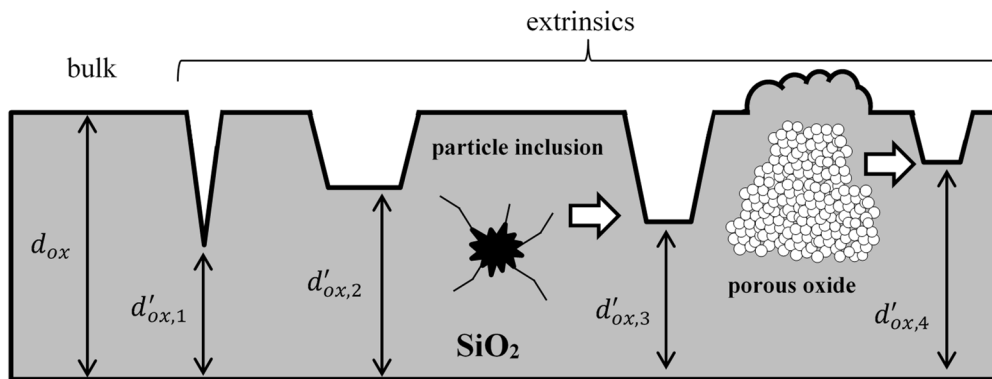


Fig. 11: Schematic representation of extrinsic defects in SiO₂ [10]

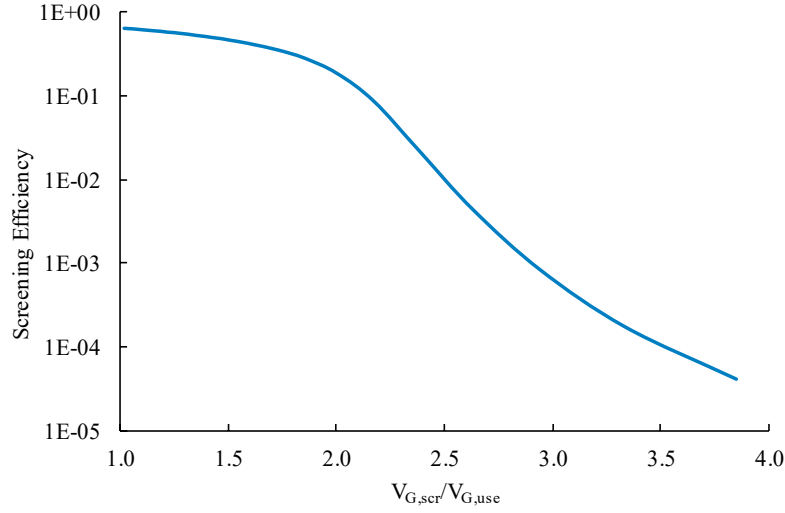


Fig. 12: Screening efficiency as a function of screening voltage to use voltage ratio

mobility after screening. Screening with a value of “only” twice the use voltage is less efficient by more than two orders of magnitude! As a consequence, the enabler for an efficient gate oxide screening is a bulk oxide thickness that is much higher than is typically needed to fulfill the intrinsic lifetime targets. Unfortunately a thicker bulk oxide increases the threshold voltage and decreases the channel conductance at a given $V_{GS(on)}$. The trade-off between gate oxide FIT rate and device performance is illustrated in Fig. 13 and was also discussed in [22]. Ultimately, the price for excellent gate oxide reliability is a higher on-state resistance.

3.2.3. Experimental verification of on-state reliability and data sheet consequences

We have tested the on-state reliability of electrically screened SiC MOSFETs for 100 days at 150°C and three different combinations of gate oxide process and screening conditions using three individual stress runs at different positive and negative gate stress biases. Each sample group consisted of 1000 pieces. Fig. 14 indicates the results for different gate oxide generations available at different phases of the device development. For twice the recommended gate bias of 30 V, fewer than 10 out of 1000 devices failed. The resulting improvement of both gate oxide process and screening procedures reduced this number to only one fail at 30 V and zero fails at 25 V and -15 V. While this one remaining failure is still an extrinsic fail, it is uncritical as it will occur far beyond the specified product lifetime under the nominal gate bias use conditions. Please note that there is virtually no chance to directly prove field-failure probabilities in the ppm range using a reliability test which runs under nominal gate bias conditions, e.g. at $V_{GS} = 15$ V. This is because one would need either millions

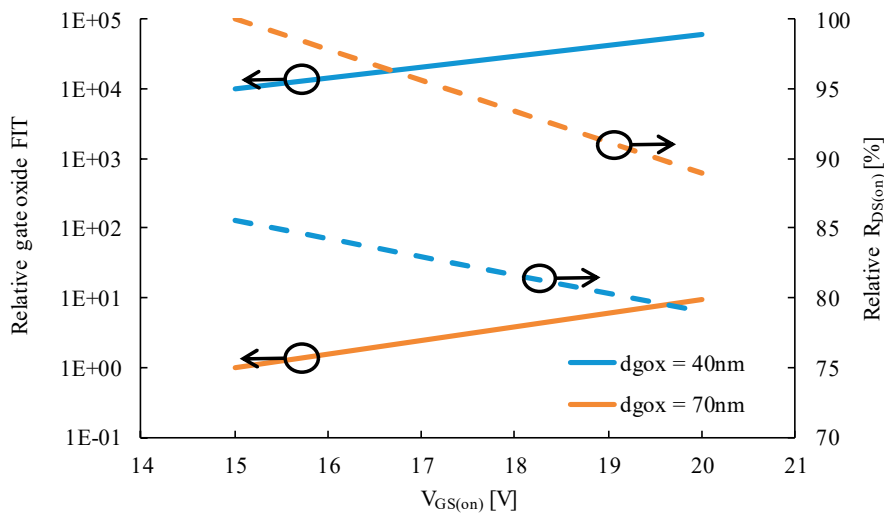


Fig. 13: Impact of gate oxide thickness and gate voltage on failure probability and on-state properties

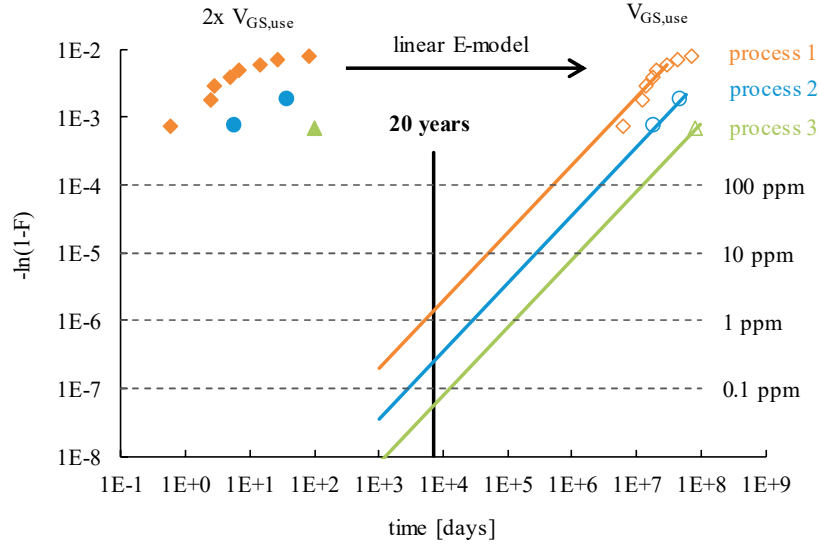


Fig. 14: Evaluation of on-state failure rate

of samples and/or testing times in the range of decades. Mathematically, one may use the linear E-model to extrapolate the result of an accelerated stress test and extract the failure probabilities for typical use conditions, e.g. 20 years and $V_{GS} = +15$ V, c.f. Fig. 14. Of course, the extrapolation is better the closer the test conditions match with the use conditions and the larger the sample size. This is particularly important when aiming to detect defect density driven (extrinsic) failure modes. These are expected to be found in a single digit percent range, most likely even lower. This is why we used a sample size of 1000 pieces each and gate stress conditions as close as possible to typical use conditions (150°C, 25 V / 30 V).

After converting the observed failure probabilities at accelerated stress conditions to $V_{GS} = +15$ V, we yield a benchmark low ppm failure rate for 20 y. This low number even enables the use of larger on-state gate voltages than 15 V, e.g. $V_{GS} = +18$ V, especially for applications which do not require such low ppm rates or which do not run in on-state for the full 20 y. The use of a higher on-state gate voltage is of course beneficial for the specific on-resistance and the overall performance of the device.

3.2.4. Experimental verification of off-state reliability

Since SiC devices allow much higher drain induced electric fields in the blocking mode compared to their Si counterparts, a limitation of the electric field in the gate oxide in the blocking mode is also needed to maintain an overall excellent reliability. The best on-state reliability is worth nothing if devices fail with a much higher probability in the off-state. The efficiency of the shielding is again a trade-off against the on-resistance. Gate oxide shielding in the blocking mode is typically achieved by providing buried p-regions which form JFET-like structures below the accumulation zone of the MOSFET [23]. This JFET adds an additional component to the on-resistance that mainly depends on the distance and the doping between the buried p-regions. This shielding structure design feature is crucial to avoid gate oxide degradation or even gate oxide breakdown in the off-state.

To verify the off-state reliability of our hardware, we have stressed more than 5000 pieces of 1.2 kV SiC MOSFETs for 100 days at 150°C at $V_{GS} = -5$ V and $V_{DS} = 1000$ V. The condition corresponds to the most critical point of the mission profile for industrial applications. A further acceleration is very difficult due to restrictions in the applied drain voltage with respect to the breakdown voltage of the device. Running this test at even higher drain voltages will falsify the results as other failure mechanisms like cosmic-ray induced failures become more likely. The result was that none of the tested devices failed during this off-state reliability test. As the 650 V device follows the same design criteria as the 1200 V device, the same reliability is expected.

3.3. Cosmic ray ruggedness

As any other high-power device SiC MOSFETs are also susceptible to single-event burnout (SEB) due to cosmic radiation. There is a certain chance that a power device gets destroyed under blocking conditions if it is hit by a highly-energetic particle which is produced by cosmic ray interactions in our

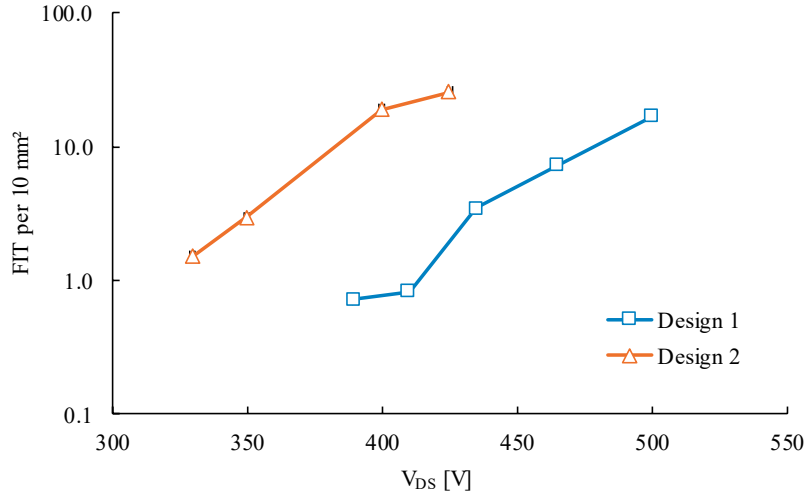


Fig. 15: Cosmic ray robustness comparison

atmosphere. The probability of a failure mainly depends on the device breakdown voltage, the applied blocking voltage, the time in operation, the operation temperature, and the altitude [24]. As such cosmic ray robustness is a design parameter which can be adjusted for any FIT rate depending on the application specification. Fig. 15 shows the test results for differently designed 650 V devices. The FIT rates shown correspond to operation at sea level and room temperature. Design 1 is capable of fulfilling a typical industrial requirement profile with a failure probability of ≤ 1 FIT at $V_{DS} \leq 420$ V while this is not the case for design 2. However, design 2 would offer a clearly lower on-resistance. A careful optimization of the device design helps to minimize the on-resistance increase while, at the same time, allowing the required cosmic ray robustness to be met.

4. Device performance in the target application

4.1. Introduction of the test board

First, the test environment will be briefly introduced before discussing the test and efficiency results. The 3.3 kW CCM totem-pole PFC test board that was designed by Infineon has a power density of 73.2 W/inch³. It is fully compliant with server power supplies with an input voltage range of 176 VAC

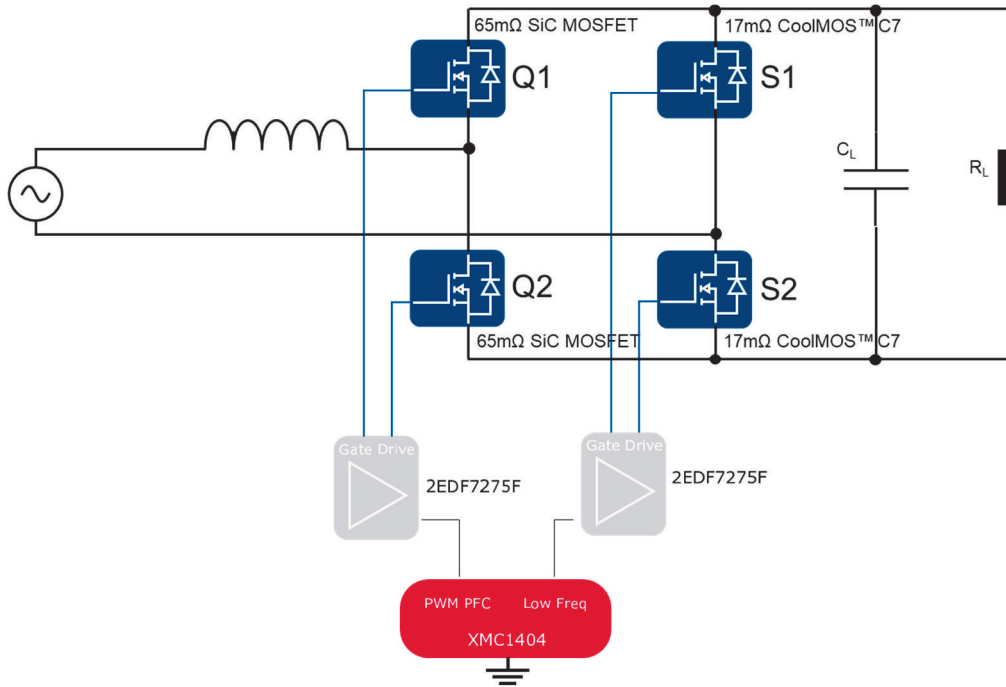


Fig. 16: Simplified schematic of the totem-pole test board

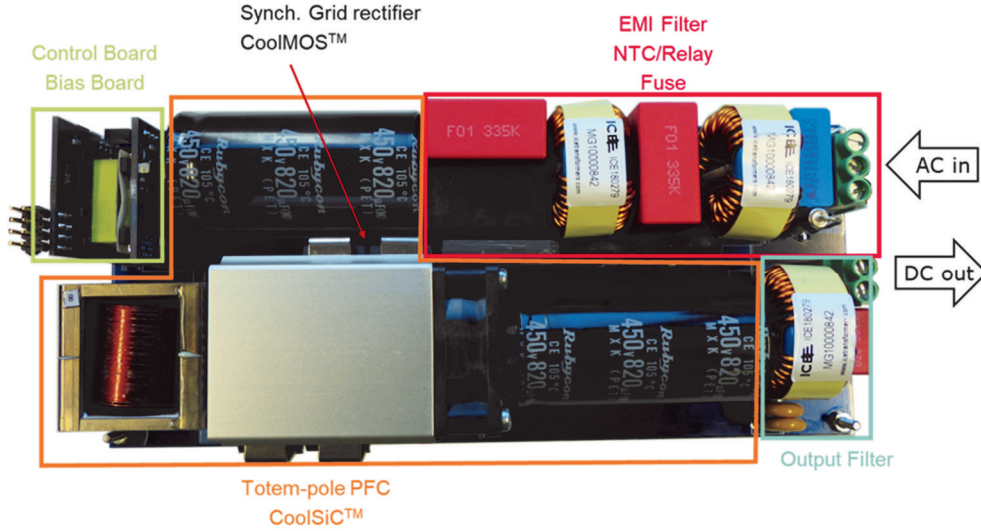


Fig. 17: The totem-pole PFC test board

to 264 VAC. The output voltage is 380 VDC and the PFC operates up to an output current of 8.7 A. In this topology, the PWM (pulse width modulation) for the boost stage of the PFC, equipped with the 650 V SiC MOSFET introduced in this work, is operating at a switching frequency of 65 kHz. In contrast, the grid rectifier and the return path are operating at the mains grid frequency of 50 / 60 Hz. This means the main requirement for these semiconductors is a low on-resistance, therefore the latest CoolMOS™ devices are a good choice here.

Fig. 16 gives the simplified schematic of the test board and Fig. 17 shows the test board.

4.2. 650 V SiC MOSFET Properties

Chips with on-resistances of 26 mΩ, 49 mΩ, 72 mΩ and 109 mΩ were assembled in either TO-247-3pin or TO-247-4pin packages for device characterization and initial performance evaluation in the target application. Note that the on-resistance was measured at room temperature at $V_{GS} = 18$ V.

Fig. 18 compares the temperature dependence of the on-resistance of a super-junction device technology with that of the 650 V SiC MOSFET technology introduced in this work. In contrast to the silicon device, the on-state resistance value of the SiC MOSFET increases only by ca. 30 % as the temperature rises from room temperature to 150 °C. From an application point of view, this behavior can be seen as an additional benefit that the current SiC MOSFET technology offers. It means that if both devices come with an identical $R_{DS(on)}$ at the datasheet condition of 25 °C, the real on-state resistance of the silicon device is more than 45 % higher for the typical operation junction temperature of ca. 100 °C.

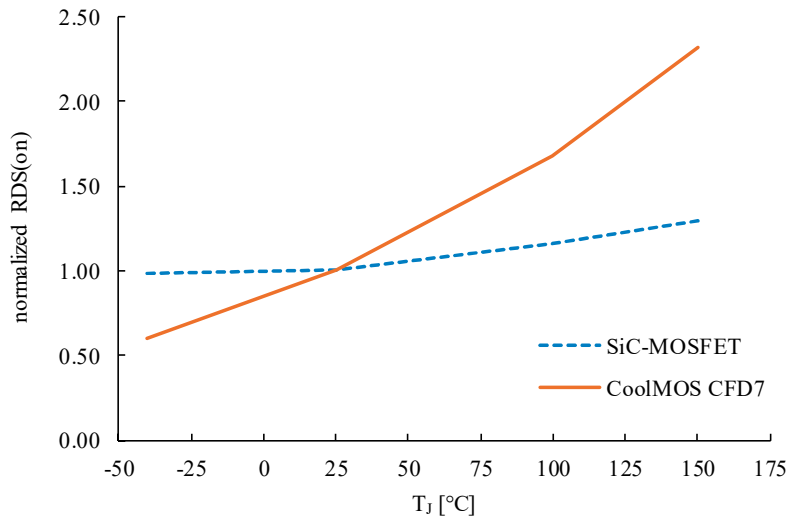


Fig. 18: Comparison of the temperature dependence of normalized $R_{DS(on)}$ for a SiC-MOSFET and for a SJ MOSFET (CoolMOS™ CFD7)

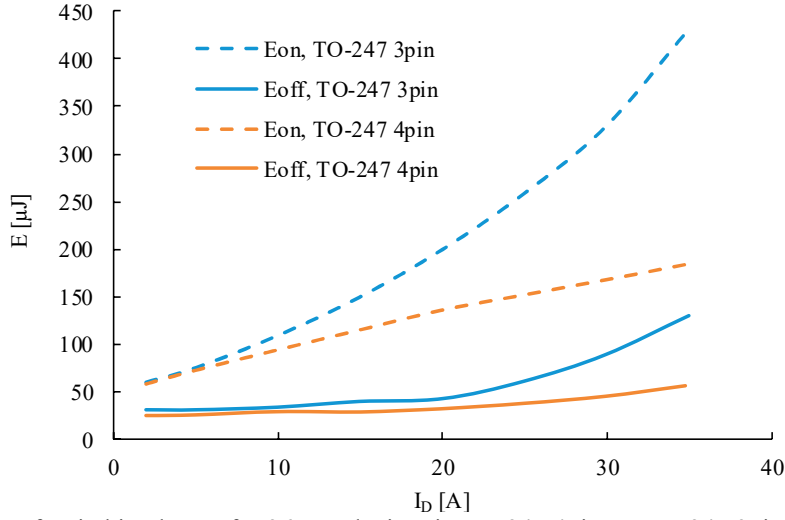


Fig. 19: Comparison of switching losses for 26 mΩ devices in TO-247 4pin vs. TO-247 3pin [$V_{DC} = 400$ V, $T = 25$ °C, $V_{GS} = 0/18$ V, $R_{G,on/off} = 5.6/0$ Ω]

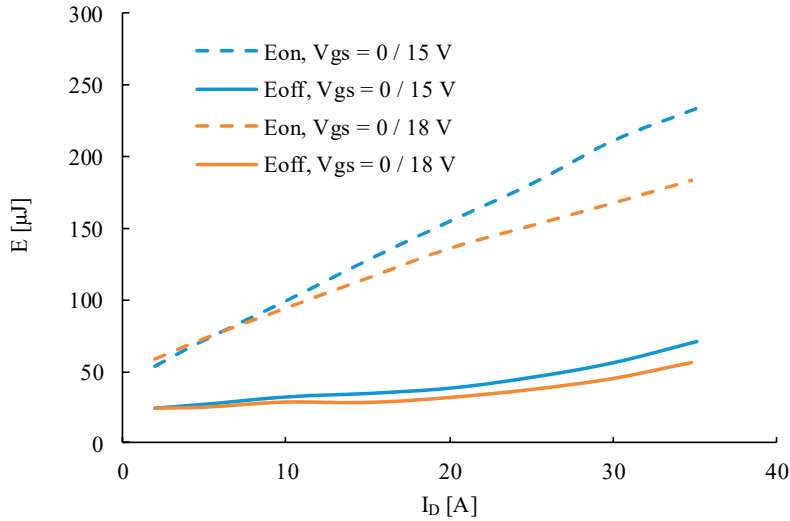


Fig. 20: Comparison of switching losses for 26 mΩ devices using $V_{GS} = 0/15$ V vs. $V_{GS} = 0/18$ V [$V_{DC} = 400$ V, $T = 25$ °C, $R_{Gon/off} = 5.6/0$ Ω, TO-247 4pin]

Turn-on and turn-off losses were measured under different conditions. Fig. 19 indicates that the use of a 4pin-package enables a significant reduction of the switching losses thanks to the elimination of feedback from the source inductance on the gate drive. Fig. 20 and Fig. 21 reveal the impact of the gate drive voltage being used for the on-state or off-state, respectively. The impact of either using 18 V for the on-state or -5 V for the off-state on the measured switching losses is almost identical. However, while a higher on-state gate voltage offers the clear benefit of a reduced on-resistance, the use of a negative gate voltage will just significantly increase the system complexity and cost. Therefore the use of a negative gate voltage is not recommended.

4.3. Device performance of the totem-pole PFC

Fig. 22 compares the difference in the efficiency as measured in the Totem-Pole PFC test board for the cases of using a negative gate voltage and zero gate voltage at off-state. The measurements indicate a very small difference that is in the range of the precision limit of the measurement equipment. From these results one can easily conclude that it hardly makes sense to turn-off the device with a negative gate voltage.

Based on the characterization results one can already calculate the expected efficiency in the target application. For a 26 mΩ device, the calculation shows that one can achieve a peak efficiency of 99 % in the target application. However, beside efficiency one also needs to care about the overall system

costs. In order to create competitive products it is necessary to optimize every SMPS design for the highest efficiency at the lowest system cost. The SiC MOSFET may have a significant impact on the system costs. Therefore all efficiency measurements were repeated for 49 m Ω , 72 m Ω and 109 m Ω devices. Fig. 23 compares the measured efficiency dependencies for these devices. The 49 m Ω device achieves a peak efficiency of 99.1 %. However, one can still obtain a peak efficiency of 99 % using the 72 m Ω device. This offers a good option for SMPS designers to reduce system costs while maintaining a high efficiency.

The cost-down option is a benefit of the temperature dependency of the on-resistance shown in Fig. 18. As already mentioned, this characteristic is an important additional advantage of the current SiC MOSFET generation over its silicon-based counterparts.

With respect to Fig. 23, it is also possible to use the 109 m Ω part in the same design at 230 VAC input voltage and a power rating of 3.3 kW. However in this case the peak efficiency will be less than 99 %. Additionally, one needs to de-rate the output power at lower input voltages due to the thermal power dissipation limits according to Fig. 24. The de-rating is obtained from the maximum allowed junction temperature T_J of 150 °C. As it is not possible to measure the junction temperature directly, simulations were needed to determine the temperature difference between the surface temperature of the mold compound and the junction temperature. The simulation yields a temperature difference of around 20 K for the 109 m Ω chip in a TO-247 4pin, a thermal interface material with a thermal

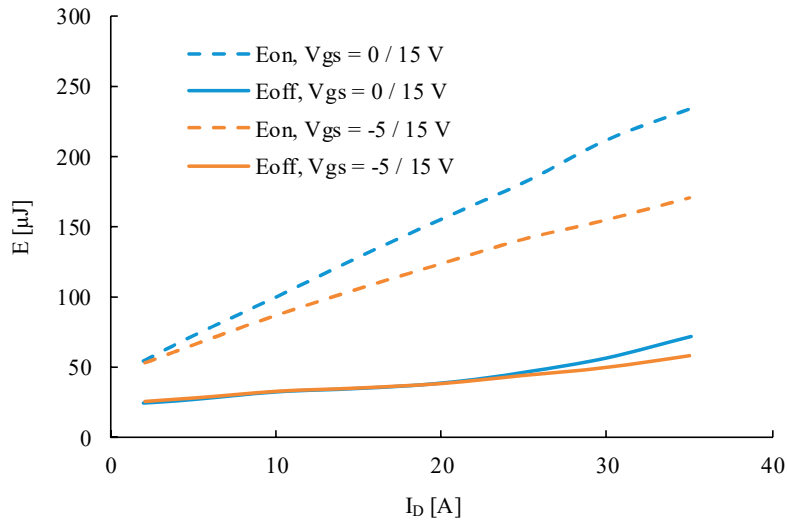


Fig. 21: Comparison of switching losses for 26 m Ω devices using $V_{GS} = 0/15$ V vs. $V_{GS} = -5/15$ V [$V_{DC} = 400$ V, $T = 25$ °C, $R_{G,on/off} = 5.6/0$ Ω , TO-247 4pin]

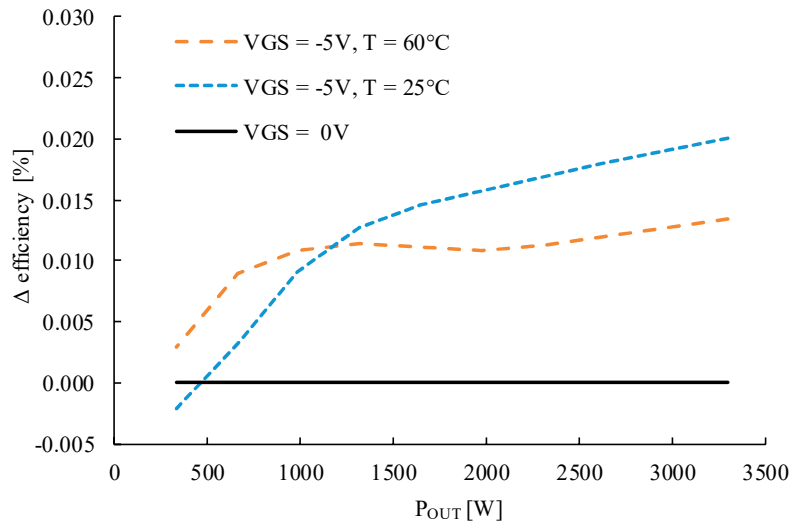


Fig. 22: Difference in efficiency in CCM Totem Pole PFC for 26 m Ω devices using $V_{GS} = -5/15$ V vs. $V_{GS} = 0/15$ V [$V_{AC} = 230$ V, $R_{G,on/off} = 5.6/0$ Ω , TO-247 4pin]

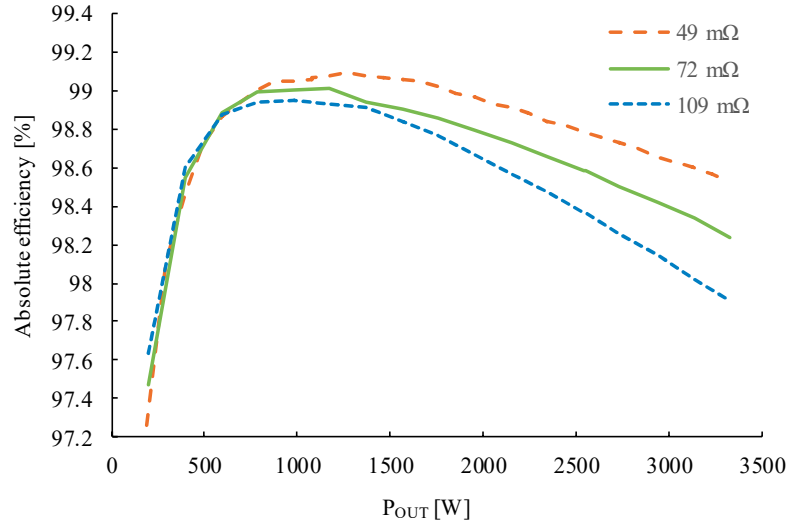


Fig. 23: Absolute efficiency of SiC MOSFET with different on-resistance in CCM Totem Pole PFC

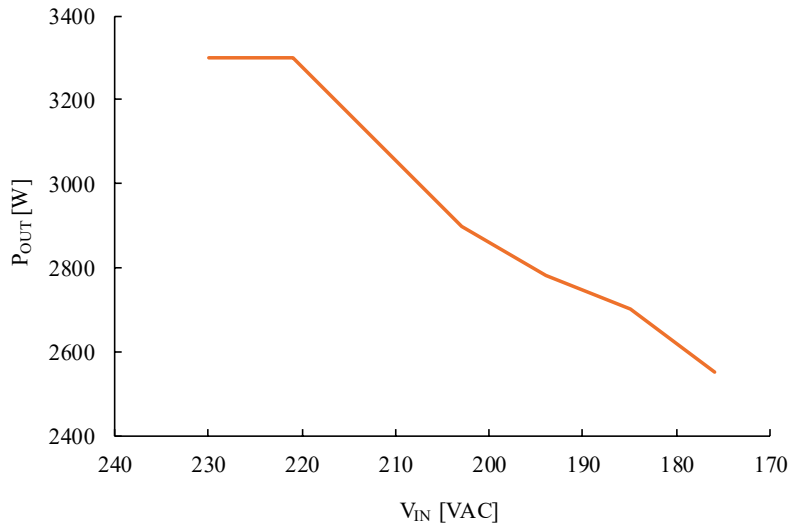


Fig. 24: Required power de-rating for 109 mΩ SiC MOSFET part at lower input voltages

conductivity of 1.8 W/mK, a thermal resistance of the heat sink of 2 K/W and an ambient temperature of 60 °C. This means that the surface temperature of the mold compound must remain below 80 °C at room temperature (25 °C), maintaining a safety margin of 15 K to the maximum allowed junction temperature.

Overall the 49 mΩ part is the best option for use in the investigated 3.3 kW CCM Totem Pole PFC. One could also decide to use parts with a larger on-resistance to address cost-down requirements.

5. Summary

This work introduces a 650 V SiC MOSFET technology that addresses the needs of switch-mode power supplies targeting a wide range of applications from telecom rectifiers through servers to solar inverters or electric vehicle chargers.

The device extends the CoolSiC™ MOSFET family based on an asymmetric trench cell concept that combines excellent reliability features with attractive low on-resistance and good ruggedness. The reliability of the developed gate oxide is proven by long-term tests using large device populations. While offering the use of a standard gate drive voltage of 15 V, the gate oxide quality also gives the option to drive the device with 18 V. In this way the on-resistance is further reduced. The gate oxide reliability and cosmic ray ruggedness fulfill the requirements for industrial applications.

These devices enable the use of new topologies in the AC-DC conversion part of switch-mode power supplies that yield a higher efficiency. To verify this improved performance, a 3.3 kW totem-pole PFC

test board design was equipped with the new SiC MOSFET devices. Efficiency measurements yield a peak efficiency of 99.1 %. Additionally, it is shown that the lower increase of on-resistance with temperature of the current SiC MOSFET device technology enables cost-efficient designs as designers can also choose parts with a higher on-resistance at room temperature.

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