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Design considerations for charge-compensated fast-switching power MOSFET in the medium-voltage range

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Abstract: Low-voltage power metal–oxide–semiconductor field-effect transistors (MOSFETs) based on charge compensation using a field plate offer a significant reduction of the area-specific on-resistance. The extension of their blocking capability into the so-called medium-voltage range of 150–300 V promises devices with excellent properties being attractive for a wide range of applications. There are two approaches how this voltage-range extension can be realised. Both concepts are linked to different device performance and different development effort. This study discusses both concepts using the example of the 150 V device class and compares the performance gained at the device and application level.

1 Introduction

The general trend in the industry goes towards power systems with a reduced total cost of ownership. Telecom equipment represents a good example of an end application where the consumption of electricity is a substantial cost burden. Therefore, high-efficiency power supplies are highly sought after. Power supply losses contribute twofold for electricity consumption: first by the converter efficiency loss itself and second by increasing the thermal load on the cooling system, which has to remove the heat generated by the efficiency loss. In addition to electricity, real estate is another big contributor to the cost of ownership especially in the urban areas. Power systems shall then have components, such as power converters, which ought to be small in volume, light weight, energy efficient, low cost and yet easy to be maintained. All these requirements impose challenges from the system down to the semiconductor level.

The advances in power semiconductor technologies enable the power designer to fulfil the above-mentioned requirements by reducing losses in power converters, both conduction and switching losses. This reduction in losses also allows for a general size reduction by various means ranging from the use of smaller magnetic components due to the use of higher switching frequencies, up to the possibility of either reducing the size of, or even eliminating, the heatsinks.

This increase in power density translates into more and more challenging conditions for the power devices. Not only should the on-resistance of the devices be reduced, but also the general figure of merit ($FOM_G = R_{DS(on)} \cdot Q_G$), the switching figure of merit ($FOM_{GD} = R_{DS(on)} \cdot Q_{GD}$) and the figure of merit with respect to output charge ($FOM_{OSS} = R_{DS(on)} \cdot Q_{OSS}$) should be minimised. In many applications this results in large improvements in the switching speed, however this is usually linked to higher current and/or voltage slew rates (di/dt and dv/dt). At the same time the current density in the devices increases (see Fig. 1) which all calls for maintaining a high ruggedness of the devices.

Low-voltage power metal–oxide–semiconductor field-effect transistors (MOSFETs) experienced dramatic improvements over the past decade thanks to the application of the charge-compensation principle to this device class. Stepping forward in the wafer manufacturing technology the breakdown voltage was extended over the years towards the so-called medium-voltage class (MVC), with a voltage range between 150 and 300 V.

While in the lower voltage range a large number of these devices are used in just one or two main application fields, this is fundamentally different in the higher voltage range. Here the devices are used in many different topologies targeting a wide range of application fields, and markets are significantly more fragmented between the different types of applications.

2 Application requirements

In the case of the 150 V device class, the largest market segments are formed by applications such as synchronous rectification in telecom rectifiers (Fig. 2), isolated DC/DC brick converters for

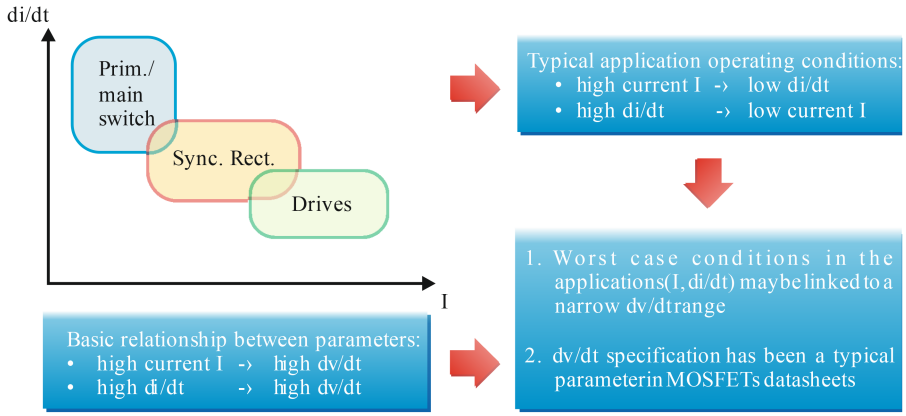

Fig. 1 *Typical relationships between di/dt, dv/dt and current*

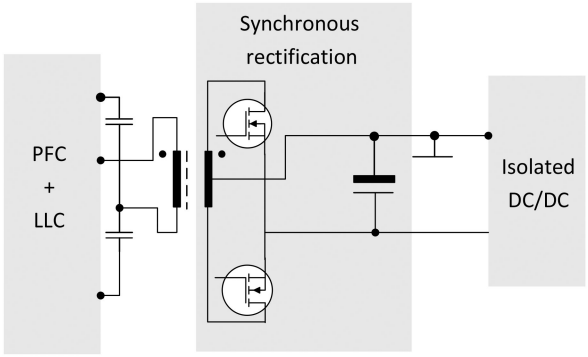

Fig. 2 *Synchronous rectification stage of a power supply unit*

telecom (Fig. 3), inverter switches for low-voltage drives (Fig. 4) and switches for solar power optimisers (Fig. 5).

Telecom rectifiers and brick converters require high power density and efficiency in order to reduce the system total cost of ownership. MVC devices (150 V) are used in both these applications as synchronous rectifiers, and, in the latter, also as an active switch on the primary side. In addition to low conduction losses, devices operating as synchronous rectifiers are further required to show good overshoot behaviour (minimised drain–source voltage spike). This means that the properties of the internal body diode, such as the reverse-recovery charge Q_{RR}, are of increasing importance. Still related to the voltage overshoot, another point to mention is the synchronous rectifier device output charge Q_{OSS} which should be minimised in order to reduce the amount of energy trapped in the stray and transformer leakage inductances.

Low-voltage drives running at battery voltages of 72 and 80 V represent a second application field. Such devices are mainly used in forklifts and light electric vehicles (LEV), for example battery driven vehicles at airports and the like. Such vehicles demand high power from the relatively low voltage delivered by the batteries. Consequently, the rated current turns out to be high, requiring that a large number of devices must be paralleled in order to be able to cope with it. Devices with competitive price, high ruggedness and designs that offer good thermal management options are of paramount importance to this application. Usually, the low-voltage drives inverter is hard switched.

The main requirements for solar power optimisers are good reliability, high efficiency, high power density and competitive pricing. Depending on the customer, either hard- or soft-switching strategies are employed.

In addition to those mentioned above, a large number of other industrial applications for medium-voltage devices can be found – each with different requirements, which makes it difficult to summarise them here.

Due to all these differences in requirements, a methodology is needed which helps to identify the device properties beneficial for all applications in order to focus on the improvement of the right device features. Such a methodology also needs to account for conflicting optimisation requirements, in case devices, which are used in different applications, need to be optimised in opposing directions and thereby indicating needs for technology derivatives.

Established methodologies for such an analysis are offered in general by the quality function deployment [1, 2]. The house-of-quality matrix as one part of it can be employed as an aid in determining how products live up to customer needs [3]. Fig. 6 illustrates the basic worksheet used in this process for analysing the relationship between customer wishes and product capabilities and their interactions, identifying development priorities and including a benchmarking of the new concepts against predecessor and competitor products. As the required inputs are delivered from different functional units such as marketing, engineering and manufacturing, the methodology also increases the cross-functional integration within the organisation.

An example for the application of this procedure to analyse the application requirements with respect to power MOSFET development can be found in earlier work [4].

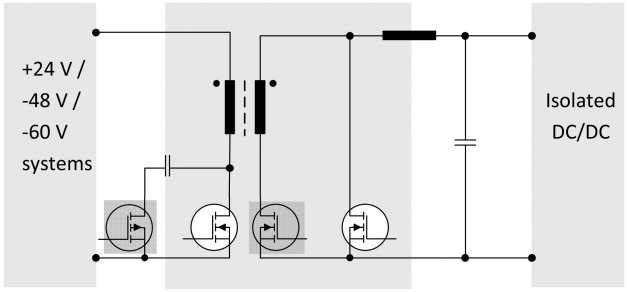

Fig. 3 *Isolated DC/DC brick converter*

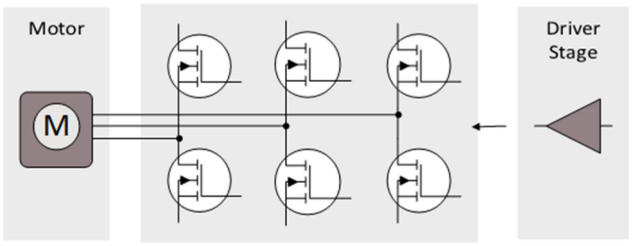

Fig. 4 *Low-voltage drives for forklift and LEV*

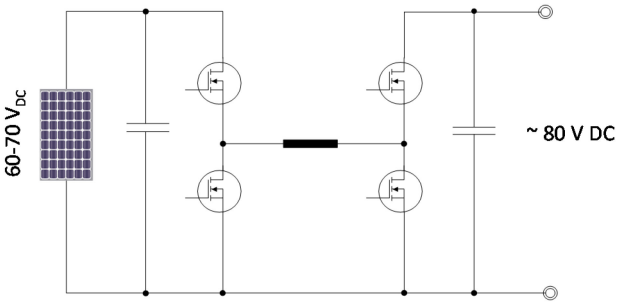

Fig. 5 *Solar power optimiser*

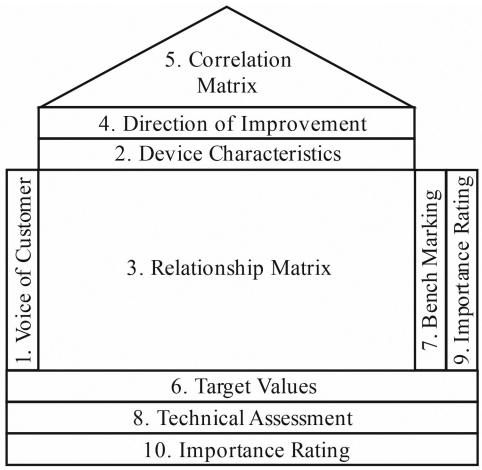

Fig. 6 *House-of-quality matrix*

With the help of the briefly described application requirement analysis, the optimisation criteria for a 150 V MOSFET device intended to be used in the previously discussed application fields are derived. As such a suitable power MOSFET device should fulfil the following requirements:

- low on-resistance $R_{DS(on)}$,
- low output charge Q_{OSS},
- low gate–drain charge Q_{GD},
- low reverse-recovery charge Q_{RR},
- high avalanche ruggedness,
- wide package portfolio including SMD.

3 Device concept

3.1 Basics of charge compensation using a field plate

Low-voltage power MOSFETs based on charge compensation using an isolated field plate offer a significant reduction of the area-specific on-resistance. Such devices entered the market more than 10 years ago and developed into a kind of standard technology for fast-switching devices. The basics and properties of these devices have been discussed in various details in many publications over the years, e.g. [5–13]. Fig. 7 gives a schematic cross-section of such a device.

In field-plate type devices, the isolated field plate provides the mobile charges required to compensate the drift region donors under blocking conditions as indicated in Fig. 8. Compared with a device using a simple planar pn-junction, the electric field now also has a component in the lateral direction. Fig. 9 explains the basic differences in the electric field for a simple pn-junction and for the case where a field plate compensates the donors in the drift region.

The application of a field plate leads to an almost constant field distribution in the vertical direction since the ionised dopants in the drift region are laterally compensated by mobile carriers in the field plate, thereby reducing the necessary drift region length and increasing the allowed drift region doping for a given breakdown voltage. Both effects contribute to the significantly reduced area-specific on-resistance. Since the field-plate electrode is connected to the source electrode of the MOSFET and the gate is formed by a separate electrode, such a device offers an outstanding area-specific on-resistance and a low gate-charge at the same time.

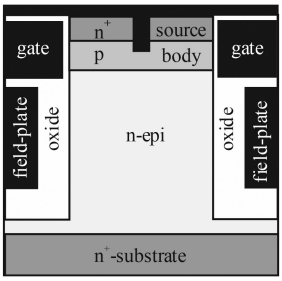

Fig. 7 *Schematic cross-section of a charge-compensated device using a field plate*

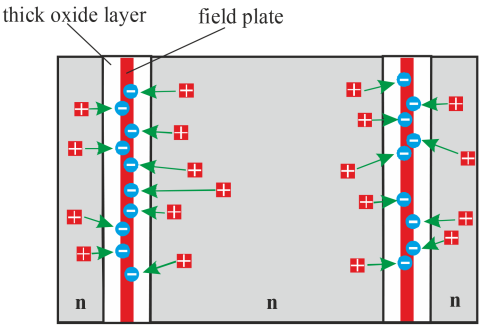

Fig. 8 *Principle of charge compensation by a field plate*

3.2 Options for further device improvements

To improve the overall efficiency, in most applications both the on-resistance and the switching losses need to be minimised at the same time in order to meet the efficiency targets at low and medium load conditions. It was shown that those targets can be reached by the use of improved manufacturing setups linked to better process control capabilities in combination with an optimised cell structure. These measures lead to an increase in the overall efficiency level without compromising the ruggedness of the device [14]. The extension of the breakdown voltage range of devices based on the charge-compensation principle by using an isolated field plate is without doubt very attractive, however a number of problems related to manufacturability and device characteristics impose a number of challenges as described in the following sections.

3.3 Design approach 1 – additional epi layer

The targeted additional blocking capability can be realised by a second lower-doped drift region under the actual compensation structure as schematically shown in Fig. 10. This allows the reutilisation of an existing cell, but the expected area-specific on-resistance will be higher as only a part of the structure is charge-compensated. Additionally, such an approach may also help to avoid wafer bow issues. Fig. 11 indicates the rising wafer bow with increasing blocking voltage within a given device manufacturing technology using the field-plate approach. The wafer bow is a critical issue as above a certain limit the wafers cannot be processed anymore. The main reasons for the rise of the bow are given by the increasing trench depth and the increasing field-oxide thickness. So if the wafer bow is close to the limit, the additional lower-doped drift region is an easy way to circumvent related problems while targeting higher blocking voltages.

However, there is still the need for some additional development effort as an appropriate edge-termination structure is needed. Once this issue is addressed such an approach allows a comparatively fast development of different voltage classes at the cost of performance, especially at cost of area-specific on-resistance.

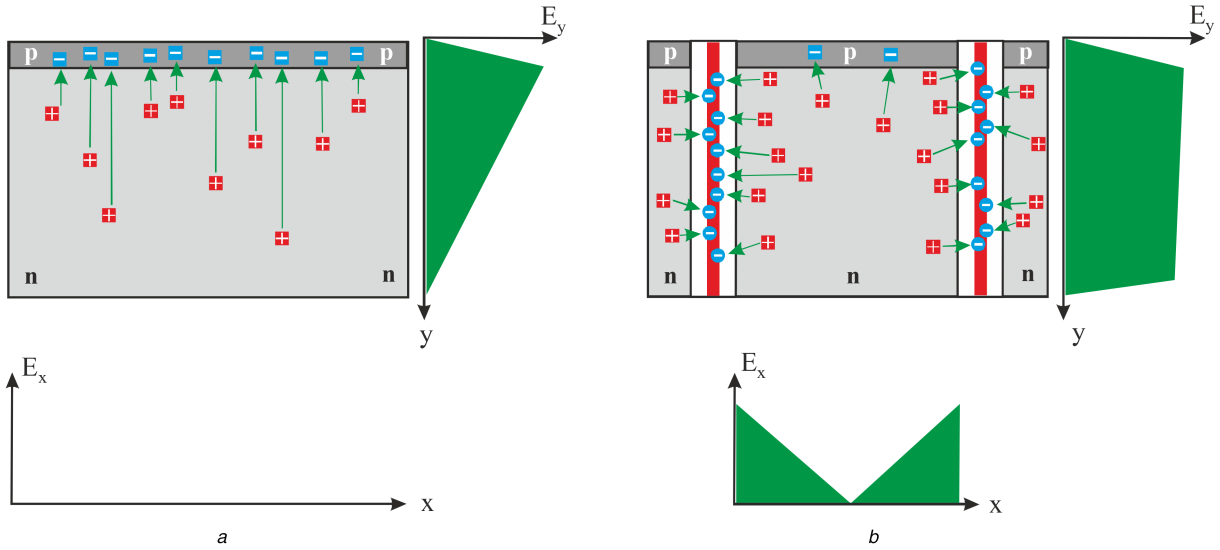

Fig. 9 *Basic differences in the electric field for a simple pn-junction and for the case where a field plate compensates the donors in the drift region*
(a) Electric field for a pn-junction, ***(b)*** Electric field for a field-plate structure

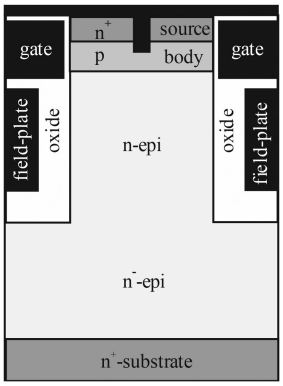

Fig. 10 *Schematic cross-section of a charge-compensated device with an additional drift layer*

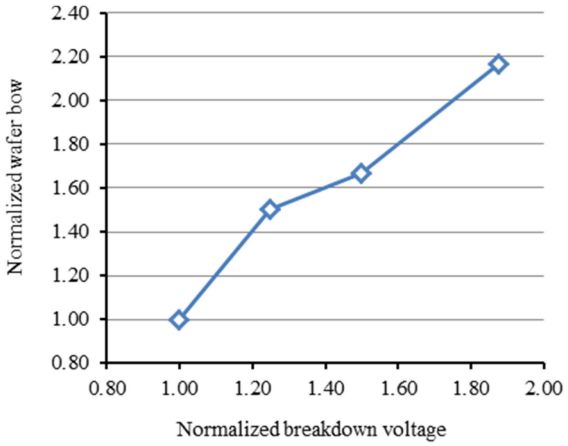

Fig. 11 *Increase of wafer bow with breakdown voltage for charge-compensated devices using a field plate*

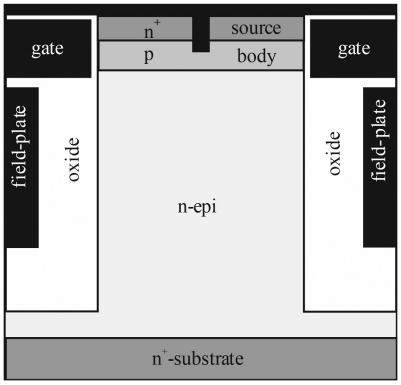

Fig. 12 *Schematic cross-section of a charge-compensated device designed for a higher blocking voltage*

3.4 Design approach 2 – full redesign of device

The required higher blocking capability can be achieved by an appropriate design of the device as depicted in Fig. 12. Among other measures, the trench depth as well as the thickness of the field oxide layer inside the trench must be increased. Without countermeasures, this might be linked, to one or all of the following problems:

- the wafer bow will become too large for the wafers to be handled in the production facilities as already discussed
- the induced stress by the mismatch of oxide and silicon in the trench exceeds the material limits and leads to cracks as shown in Fig. 13,
- the control of the trench depth which is important for an acceptable parameter tolerance either becomes more difficult or leads to long process times linked to higher costs.

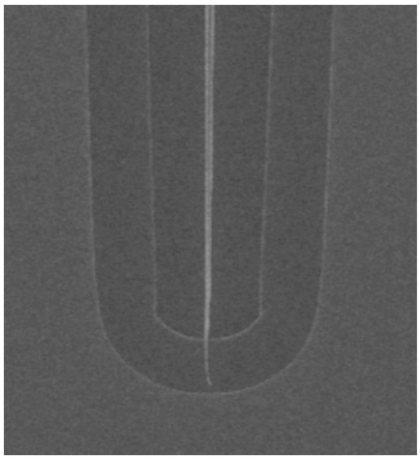

Fig. 13 *Stress-induced crack through a thick oxide in the field-plate trench*

On the other hand, this device will offer the best area-specific on-resistance as the full drift-region length is compensated. As such the concept enables the best possible optimisation of the device with respect to different application requirements. Obviously, any effort which was spent before to gain better control over process parameters to improve the device parameters [15] will be helpful here as well. The aforementioned problems related to wafer bow and cracks may be solved by a careful optimisation of process parameters, appropriate selection of the materials used or even a reordering of process steps.

4 Comparison of device properties

In order to select the right approach it is interesting to evaluate the realised device performance at the product level, which includes the package contribution to the overall on-resistance of the device. The comparison presented in this work is done for fully processed devices with a nominal blocking voltage of 150 V.

Fig. 14 compares the on-resistance in different packages. All devices are so-called best-in-class devices. This means that for each package type the largest possible chip area which fits into the package is used. As is to be expected the devices based on a full redesign with respect to the targeted nominal blocking voltage (approach 2) show a clearly reduced on-resistance for the product.

This improvement is gained by the changed device design. Fig. 15 indicates the percentage of the contribution of the power MOSFETs different structural elements to the overall on-resistance of each of the devices. Here, ‘channel’ represents the contribution of the body and the source region, ‘trench’ represents the contribution of the charge-compensated region, ‘socket’ stands for the part related to the drift layer below the trench bottom while ‘substrate’ embodies the resistance of the base material. As the on-resistance of the device following the design approach 2 is smaller than that of the design approach 1, it can be concluded that by far the largest part of the obtained improvement is gained by the elimination of the additional lower-doped drift layer.

Fig. 16 compares the important figures of merit in order to evaluate the dynamic device properties. This comparison is important as the devices are widely used in applications where fast switching is required and high switching frequencies are demanded. As such the better on-resistance of the device need not be compromised by a high gate charge, a large Miller capacitance or an increased output charge. The presented comparison is done for best-in-class devices in a SSO8 package. Regarding dynamic properties the device based on a full redesign yields improved device parameters. Moreover, it also shows a more linear output capacitance with less accumulated charge as can be seen in Fig. 17. This capacitance linearity, along with its reduced stored charge, is highly appreciated in applications such as synchronous rectification as it is linked to reduced voltage overshoots.

Since excellent avalanche ruggedness is required by many applications it is of interest to see if there is a difference in the behaviour for the two different approaches. For this investigation, devices with different active areas were characterised. In the

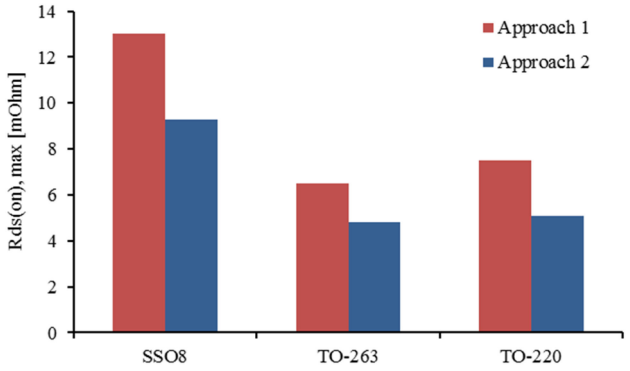

Fig. 14 *Comparison of the product on-resistance of 150 V devices with respect to the discussed concept approaches*

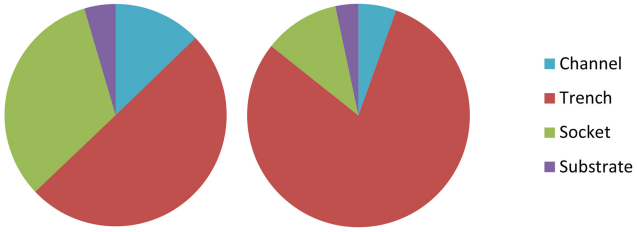

Fig. 15 *$R_{DS(on)}$ composition for a 150 V device designed according to approach 1 (left) and approach 2 (right)*

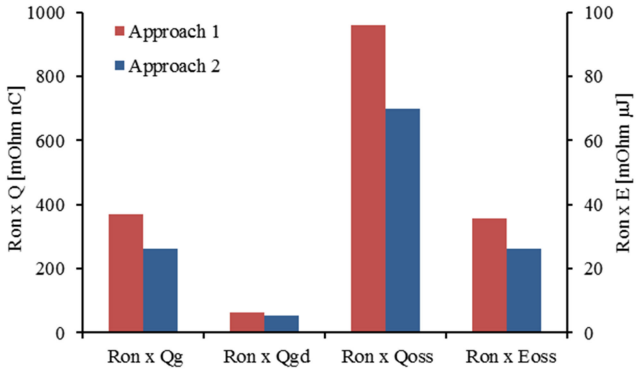

Fig. 16 *Comparison of the most important FOM of best-in-class 150 V devices in a SSO8 package*

unclamped inductive switching test, different values of the avalanche inductor were used to cover a large range of current densities and test conditions. Fig. 18 gives the comparison between both device concepts and does not reveal a significantly different avalanche ruggedness. This can be easily understood since the avalanche capability is limited by the amount of dissipated energy which heats-up the device up to the intrinsic temperature of the semiconductor material. Once this point is reached, thermally generated carriers exceed the extrinsic dopant concentration and the device begins to behave as an intrinsic semiconductor material with conduction properties entirely governed by temperature and not by doping [16]. If the current continues to flow, the device will be destroyed. The avalanche capability in this case is in first order governed by the device area as a single-pulse avalanche event is usually short and the heat front yet not reaches the leadframe of the device. Consequently a device with the same area owns approximately the same intrinsic avalanche capability. A deviation would point to an extrinsic destruction mechanism like the activation of the parasitic bipolar junction transistor (BJT) which must be avoided by an appropriate device design.

Based on the presented numbers it can be concluded that the additional technological development effort spent on a dedicated device design for the respective voltage class is paid-off by significantly better overall device properties.

5 Device performance in application

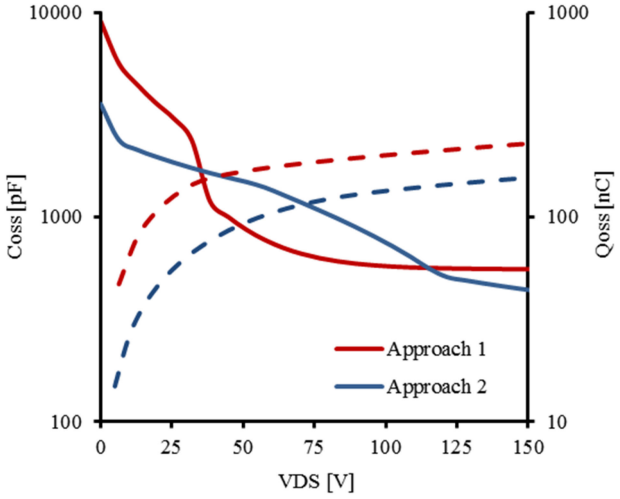

Fig. 17 *Comparison of MOSFET output capacitance C_{OSS} (solid lines) and output charge Q_{OSS} (dashed lines) for the design approaches 1 and 2 (R_{DSon} = 7.5 mΩ)*

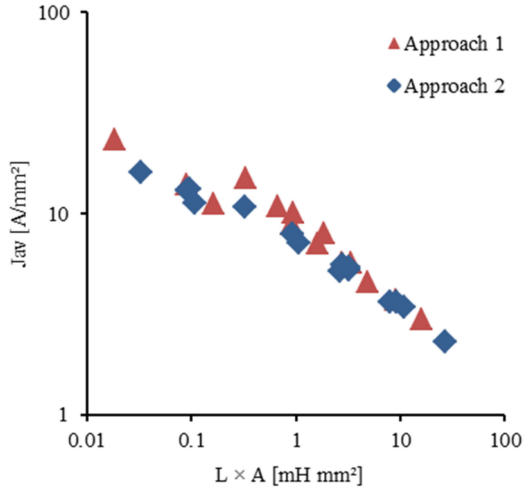

Fig. 18 *Comparison of avalanche destruction current densities for the two different devices*

The improvement of the device parameters gives a clear indication that the use of the design approach 2 is advantageous, as can be seen next for synchronous rectification in both soft-switching and hard-switching topologies. Although devices with low on-resistance can help to reduce the number of parts in a given design, a reduced voltage overshoot behaviour is also an important feature of the device. It reduces design-in efforts by either reducing, or even eliminating, the complexity of snubber circuits and saves bill-of-material costs and design-in time and effort. Moreover, it also improves efficiency yielding a simpler cooling concept, which again contributes to additional savings here.

5.1 Synchronous rectification in soft-switching applications

Telecom rectifiers and server power supplies have strongly benefited from the use of soft-switching techniques to improve the efficiency [17, 18]. These techniques reduce losses on the primary side only, still leaving the secondary-side rectification-related losses to be addressed. The latter are tackled by synchronous rectification (SR) which replaces diode rectifiers with MOSFETs, thus dramatically reducing rectification conduction losses and increasing the converter efficiency and the power density [19].

The benefits of the combination of soft-switching techniques with synchronous rectification can be best experienced in a 3 kW interleaved LLC converter with an output voltage of 54 V [20]. High-power low output-voltage LLC converters must deliver a very high DC output current which represents the DC component of the rectified sinusoidal resonant current. The high-resonant AC

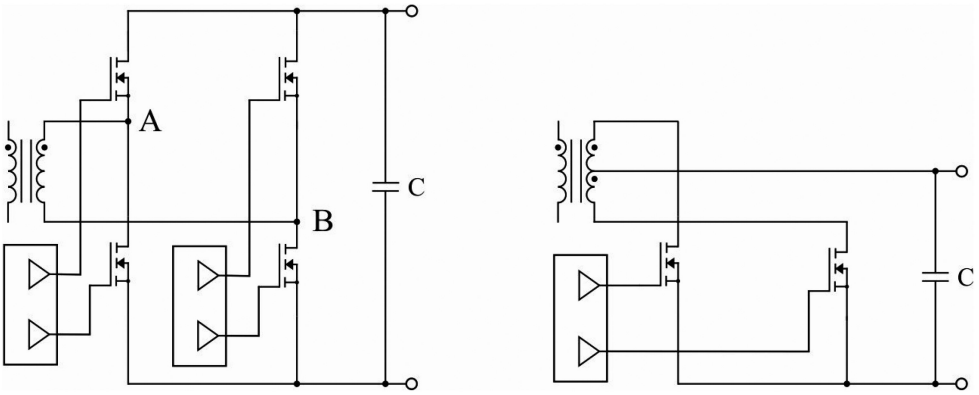

Fig. 19 *Full-bridge SR configuration (left) and centre-tapped SR configuration (right)*

current component must then be filtered out by the LLC converter output capacitors.

Such capacitors have their size determined by the converter output voltage ripple requirement along with its switching frequency and output current level. If the current level is high, a relatively large output capacitance is required. Therefore, aluminium electrolytic capacitors are the preferred choice. However, since these capacitors have a larger dissipation factor than that of other types of capacitors, they produce more internal heat when a ripple current flows through them. The temperature rise linked to this heat may significantly affect their lifetime [21]. In order to avoid this, several electrolytic capacitors might have to be placed in parallel in order to cope with the inherently high ripple current which in turn increases the converter size.

Interleaving converters represent a technique of paralleling converters that avoids both the direct paralleling of high-voltage switches on the converter primary side and the high-ripple current in the output capacitors due to the cancellation of such ripple currents [22].

Synchronous rectification can be implemented in LLC converters either by full-bridge or by centre-tapped configurations as shown schematically in Fig. 19. The full-bridge configuration has the advantage of a simple transformer design (single secondary winding) and a bathtub-shaped effective node capacitance as depicted in Fig. 20. This capacitance shape has the advantage of eliminating the overshoots in the SR MOSFETs as the capacitance increases with voltage. The downside of the SR full-bridge configuration is its complexity and the higher cost when compared with the centre-tapped approach, as two SR MOSFETs are connected in series during rectification and two half-bridge drivers are required.

In contrast, the centre-tapped SR configuration as shown in Fig. 19 offers the advantage of a lower circuit complexity and lower costs compared with the full-bridge configuration. As a downside it should be mentioned that a more complex transformer design consisting of two secondary windings is needed and that there is no bathtub-shaped effective capacitance, leaving the circuit more prone to overshoots.

SR MOSFETs that follow approach 2 help the designer to overcome the latter disadvantage by reducing the overshoot voltage due to its lower output capacitance value and its more linear shape (higher capacitance at moderate-to-high voltage range). This absorbs the energy trapped in the commutation-loop stray inductance and transformer leakage inductance, rendering lower overshoot voltage compared with SR MOSFETs which follow approach 1.

The 3 kW interleaved half-bridge LLC DC/DC converter [20] with a centre-tapped secondary-side synchronous rectification is used as a soft-switched test platform. Fig. 21 illustrates the basic schematic of the secondary side of this LLC converter. This converter steps the nominal input voltage of 380 V DC, which is usually generated by a front-end power factor correction (PFC) converter (not presented here), down to the output voltage of 54 V DC. The output current capability covers a range up to 55.55 A. The interleaved stages are digitally controlled and the asynchronous switching frequencies are in the range of 100 kHz.

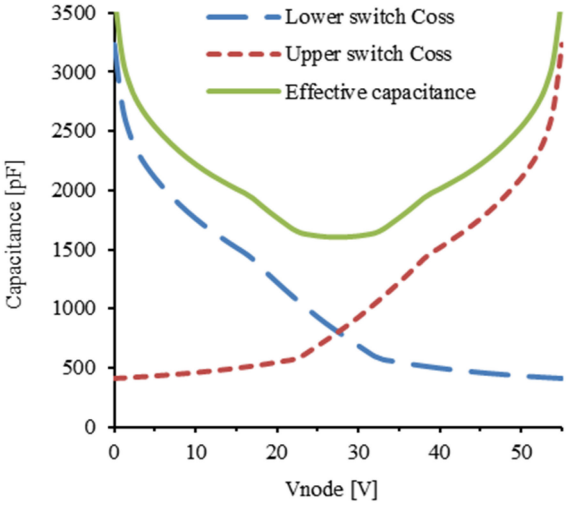

Fig. 20 *Effective capacitance at node A or B (see Fig. 19) in the full-bridge SR configuration*

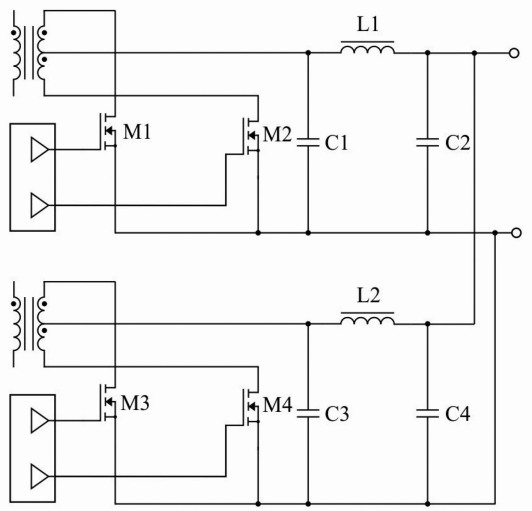

Fig. 21 *Basic schematic of the secondary side of the two interleaved LLC stages*

Therefore, both output voltages are regulated and the current sharing between the stages is well controlled.

Fig. 22 shows the efficiency measurement results for each of the two MOSFET design approaches. The efficiency curves show some kinks which are related to the operation of the LLC converter with its two stages:

- the first kink shows up when the second LLC stage gets activated,

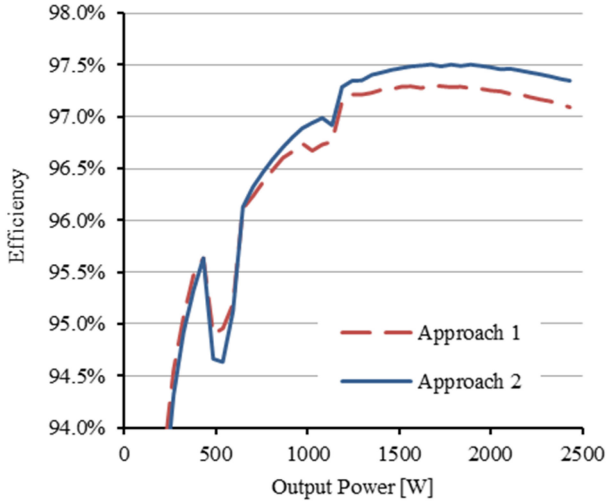

Fig. 22 *Comparison of the efficiency of the AC/DC converter stage using 150 V devices of app. identical area with different design approaches*

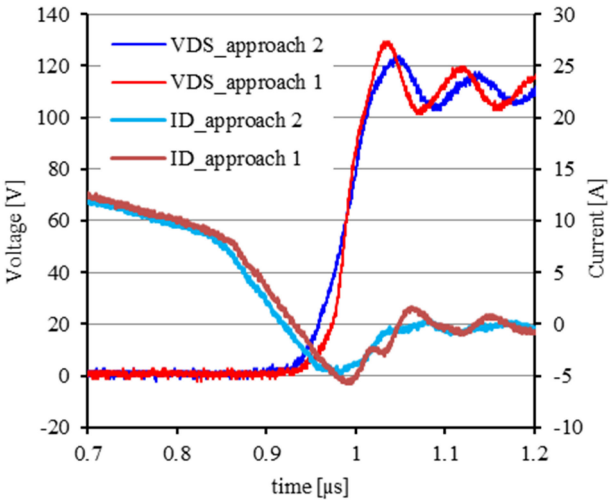

Fig. 23 *Comparison of voltage overshoot due to body diode commutation using 150 V devices of identical on-resistance with different design approaches (V_{IN} = 390 V, I_{OUT} = 20 A)*

- the second kink is caused by the activation of synchronous rectification in the first LLC stage,
- the third kink is due to the activation of synchronous rectification in the second LLC stage.

The higher effort to realise the device in approach 2 gives a clear benefit in this application: the peak efficiency is increased by 0.2% while the efficiency at full load increases by as much as 0.25%. This gain in efficiency is directly related to the reduction of the on-resistance R_{DSon} with design approach 2.

Fig. 23 illustrates the voltage overshoot linked to the body diode commutation and to the output charge Q_{OSS} as well as the stored-charge Q_{RR} of the synchronous rectification MOSFET. For the device following the design approach 2 the voltage overshoot is reduced by 5 V while at the same time the reverse-recovery current peak shows a smaller amplitude as both charges are reduced.

5.2 Synchronous rectification in hard-switching applications

Solar power optimisers usually use a non-isolated buck–boost converter topology as seen in Fig. 5 due to its simplicity, low cost and yet good efficiency yield, even if operated in hard-switching pulse-width modulation, which makes the design easier from a control perspective. This topology also benefits from using devices that follow approach 2, especially when these devices are used as synchronous rectifiers. Their more linear output capacitance should

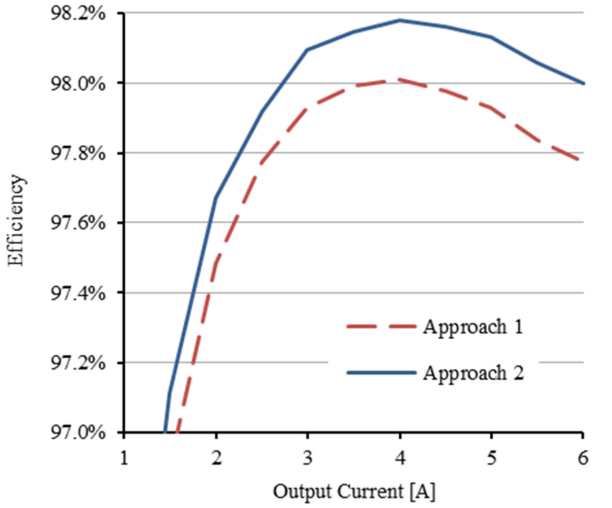

Fig. 24 *Comparison of the efficiency of the buck converter using 150 V devices of app. identical area with different design approaches*

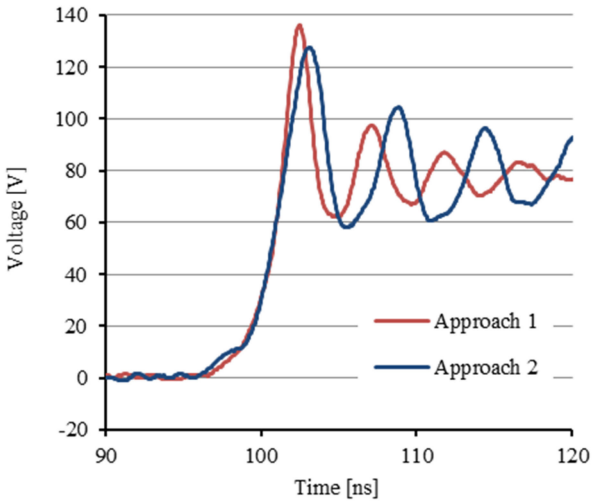

Fig. 25 *Comparison of the half-bridge phase node voltage overshoot due to the body diode commutation using 150 V devices of identical on-resistance (V_{IN} = 75 V, I_{OUT} = 4 A)*

yield a lower phase-node voltage overshoot compared with devices which follow approach 1.

Experimental results were collected using a 250 W hard-switched buck converter board operated at 200 kHz as the test platform. This board reproduces the operation of a solar power optimiser when operated in buck mode, an approach being discussed in more details elsewhere [23, 24]. The input voltage is kept at 75 V and the output voltage is regulated down to 42 V. All switches have an identical on-resistance. Fig. 24 compares the efficiency measurement results for each of the two MOSFET design approaches. Once again, approach 2 gives a better performance: the peak efficiency is increased by almost 0.2% while the efficiency at full load increases slightly above this value. Fig. 25 shows the voltage overshoot linked to the body diode commutation. For the device following approach 2 the voltage overshoot is reduced by 8 V.

6 Conclusion

This work discusses two different device design approaches for extending the blocking voltage capability of low-voltage power MOSFETs based on the charge-compensation principle using an isolated field plate. The devices discussed are intended to address the so-called medium-voltage range of 150–300 V. Potential target applications include primary side switches and synchronous rectification stages of switch-mode power supplies, low-voltage

motor drives or solar power optimisers. These devices are used both in hard- and soft-switching topologies.

The first and simpler approach achieves the required additional blocking capability by having a second lower-doped drift region added under its actual compensation structure. Although this allows the reutilisation of existing cells at the expense of increased area-specific on-resistance, it still requires the development of a suitable edge termination structure.

The second approach is based on an appropriate design of the device with, among other measures, an increased trench depth and an adapted field oxide layer thickness, which has been shown to meet the required blocking capability. This approach offers the best area-specific on-resistance as the full drift-region length is compensated. As such, it is expected that this second design concept enables the best possible optimisation of the device performance with respect to a wide range of different application requirements.

The performance of both design concepts has been evaluated using devices with a blocking voltage of 150 V. As confirmed by the experimental results presented for synchronous rectification, employed in both hard- and soft-switched applications, the second approach based on a specific design for a given voltage class delivers a better overall performance. Consequently, the higher development effort required for this approach is clearly justified by the better properties and behaviour of the realised power MOSFET.

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