A SiC Trench MOSFET concept offering improved channel mobility and high reliability

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Abstract

This work discusses the challenges in the design of a SiC Power MOSFET compared to their silicon-based relatives and describes a novel SiC Trench MOSFET concept. The most prominent difficulties being identified are related to the properties of the channel and the gate dielectric as well as their interface. Different approaches to realize a SiC MOSFET are briefly discussed and the CoolSiC™ MOSFET concept is introduced which balances low conduction losses with an IGBT-like reliability. Long term gate oxide tests reveal that the extrinsic failure rate can be confidently predicted to be less than 1 FIT per die in 20 years under specified use conditions for industrial applications.

Acknowledgements

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1. Introduction

Wide band-gap semiconductors based on silicon-carbide are most attractive for power devices due to low losses, improved temperature capability and high thermal conductivity. Although silicon-carbide Schottky diodes have been commercially available for more than a decade, active switches are only just arriving in the market. The last few years have seen the market introduction of a number of active silicon carbide power devices based on different device concepts such as the BJT [1], normally-off vertical JFET [2], normally-on quasi-vertical JFET [3] and several MOSFETs [4-6], with some of them already vanishing. For the time being the MOSFET seems to have become the device of choice, as it is a voltage-controlled, normally-off device which makes it user-friendly. This trend is supported by an inversion-channel mobility being significantly improved over time, e.g. by nitridation techniques using nitric oxide or by the use of nonplanar structures [7,8]. In addition, significant progress was achieved in improving the extrinsic failure rate of the gate oxide. Finally, assets of a frontend fabrication process in 6-inch regarding reproducibility, stability, precision and efficiency are utilized effectively.

2. Device Concept

2.1 SiC MOSFET design challenges

While the use of silicon carbide promises many advantages thanks to being a wide bandgap material, there are also some noteworthy differences to silicon leading to a number of challenges when making a SiC MOSFET based on the 4H-SiC poly type, the most prominent silicon-carbide polymorph used for power semiconductor devices.

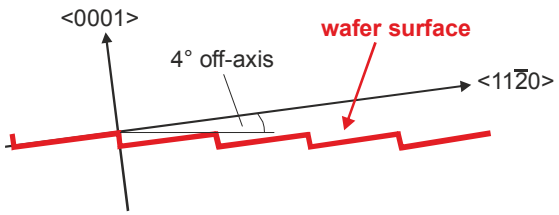

Fig. 1: Schematic illustration of the 4° off-axis cut of 4H-SiC wafers

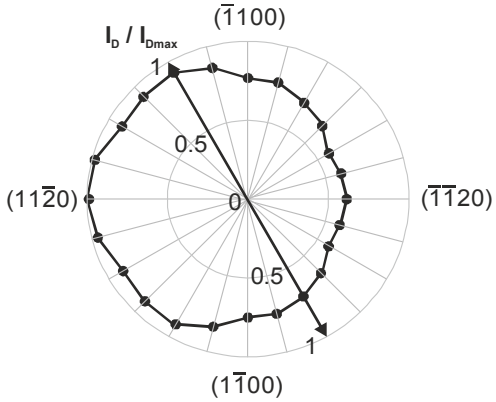

Fig. 2: Relative channel mobility for various trench planes of 4H-SiC on-axis substrate [12]

A first challenge for SiC MOSFETs is the low electron mobility at the SiO_2/SiC interface due to carbon-related interface defects resulting from thermal oxidation. Due to electron scattering at such charged point defects at the interface and because of charge trapping effects, the channel mobility is in the range of 5 – 70 cm²/Vs, which is typically only a fraction of the bulk mobility of ca. 400 cm²/Vs (the value at a bulk doping level equal to the channel doping) [9]. The defects with energy levels somewhere within the larger bandgap of SiC can interact over a larger span of time constants by trapping or emitting electrons. This effect causes a hysteresis in the threshold voltage [10]. The trapping and emission of inversion and accumulation charge at these near interface traps (NIT) causes more complex threshold voltage variations depending on the applied gate voltage profile and temperature [11]. Although most of the observed variations are fully reversible, more sophisticated gate oxide processes are needed to limit the more permanent component of the threshold voltage instability.

Another issue to be addressed for today's SiC devices is the 4° off-axis tilt of commercially available SiC substrates. This is a consequence of the need for epitaxial layer growth and thus cannot be avoided. Due to the tilt the wafer surface does not perfectly coincide with the (0001) crystal c-plane, causing a rough surface and steps as depicted in Fig. 1. It has been shown experimentally that the channel mobility strongly depends on the chosen crystal plane, and a factor of almost 2 between the worst and best channel mobility must be expected, as indicated in Fig. 2 [12].

Improvements to the dielectric and interface properties can reduce the interface state density using a suitable post-oxidation annealing step like a nitric oxide annealing [8]. Any improvement here will usually also increase the channel mobility due to the reduced impact of Coulomb scattering and charge trapping. In addition, the amount of threshold voltage shift with temperature and time becomes less.

As SiC devices allow roughly 10 times higher electric fields than their Si counterparts, the electric field in the gate oxide has to be limited in order to maintain the required reliability of the device. This reduction or limitation of the electric field strength must be realized by appropriate device design measures as discussed in the next section.

2.2 Cell concept

The first and still most widely used approach to realize a SiC MOSFET is the one using a planar gate and a quasi-vertical structure as shown in Fig. 3 [4]. As it is necessary to limit the electric field reaching the SiO_2/SiC interface, the parasitic JFET represented by the p-wells of the structure is not as disadvantageous as for the silicon counterparts. However, the lateral channel structure limits the scalability of the structure, and as such the area-specific on-resistance that can be achieved. Another disadvantage arises from the lateral channel orientation, which is linked to low channel mobility and a comparably high interface trap density, as discussed before.

Fig. 4 shows another approach using a double trench structure [5,6]. The use of a trench gate results in an increased channel width and, even despite using off-axis material, still provides a higher channel mobility. However, as the channel is oriented along different sidewalls, which correspond to different crystal planes, the properties of each channel will differ from one another. The second trench is

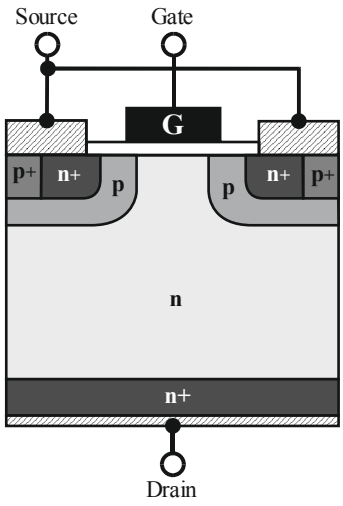

Fig. 3: SiC MOSFET with planar gate structure [4]

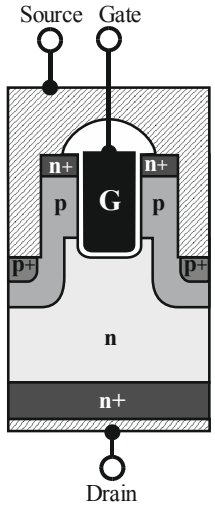

Fig. 4: A trench SiC MOSFET with double trench structure [5]

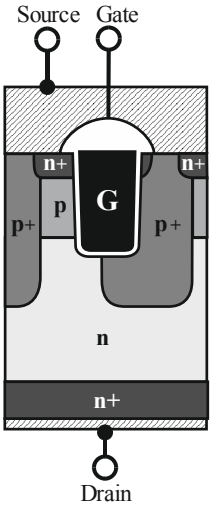

Fig. 5: Proposed trench SiC MOSFET with asymmetric channel

connected to a deep p-well, ensuring the required limitation of the electric field at the SiO_2/SiC interface and at the same time providing a large enough area for body diode conduction. On the other hand the need for a second trench negatively affects the cell pitch, and as such limits the channel width which can be realized.

Our approach is depicted in Fig. 5. The main channel is exactly oriented along the a-plane $<11\bar{2}0>$ which gives the best channel mobility and lowest interface trap density. Hence the best channel properties are realized at the expense of the 2nd trench sidewall as an active channel. The SiO_2/SiC interface is again shielded by deep p-wells. The deep p-type regions also serve as emitters of the body diode, which can be used for freewheeling operation. In all, this allows a very compact cell design and compensates for the missing channel at the 2nd sidewall, and as such realizes a low area-specific on-resistance which is about half the value of typical DMOS cells. Thanks to the improved channel properties the device can be easily driven by commonly used gate-source voltages of V_{GS} = + 15 V. The cell construction inherently has a favorable small ratio of the Miller charge Q_{GD} relative to the gate-source charge Q_{GS}. Q_{GS} is comparably large since a large part of the trench contributes to it, i.e. the n^+-type areas and all p-type areas which are connected via a well to the source. In all, this allows for a well-controlled switching with very low dynamic losses [13]. In particular, this feature is essential to suppress undesirable additional losses caused by a parasitic turn-on in topologies using half bridges.

3. Gate oxide reliability

3.1. Intrinsic and extrinsic oxide breakdown mechanisms

Tests of commercial MOSFET products revealed that there are still concerns about the SiC MOSFET gate oxide reliability [14], in particular with respect to the high failure rate as a consequence of high gate oxide stress fields [15]. Linked to this is a debate in the literature as to whether the high number of early failures in SiC MOS structures is due to an intrinsic (built-in) weakness of SiO_2 when grown on SiC or due to some macroscopic defects or imperfections at the SiC/SiO_2 interface or inside the bulk of the SiO_2, so-called extrinsics or extrinsic defects [16-18]. A more detailed overview on this topic than can be presented here will be published in [19] including the appropriate mathematical framework.

If the first model of an intrinsic oxide weakness applies, it would mean that an oxide on SiC can never be of the same reliability as an oxide of the same thickness on Si. When stressed by the same electric field, any oxide on SiC would intrinsically break down earlier even if it is free of extrinsic defects. It has been suggested that trap-assisted tunneling via an intrinsic defect band inside the SiO_2 could cause the broad failure distribution in SiC MOS time-dependent breakdown (TDDB) data [16]. Also,

fundamentally different intrinsic properties of oxides grown on SiC could limit the applicability of established know-how from Si and may lead to wrong interpretation of accelerated reliability tests.
If on the other hand the second model of extrinsic defects applies, the reason for the higher number of initially defective parts at the end of SiC MOSFET processing is rather defect driven (e.g. substrate defects, oxide defects etc.) [18,20]. As a consequence the gate oxide reliability can be improved by growing less defective substrates, providing cleaner oxides or eliminating defects during fabrication. Furthermore, assuming that the SiC MOS structure has the same intrinsic reliability as a Si MOS structure, a lot of know-how from Si can be directly applied to SiC, which allows a SiC MOSFET to be treated basically as a Si MOSFET. The only remaining difference as of today would be the higher extrinsic defect density at the end of processing.
Most experimental studies favor the second defect-related explanation of early gate oxide failures in SiC MOS structures. For example, it has been demonstrated on small scale MOS capacitors, which exhibit a negligible probability of hosting an extrinsic defect, that the intrinsic oxide properties of SiO_2 on SiC are very similar or even identical to the intrinsic properties of SiO_2 on Si [21]. Still it is important to consider the following reasonable arguments which could cause an intrinsic weakness:

- The larger bandgap of 4H-SiC reduces the conduction and valence band offsets between the SiC semiconductor and the gate dielectric (see Fig. 6). This causes for the same oxide field a higher Fowler-Nordheim tunneling current than in silicon devices [17]. If the tunneling current and not the electric field controls the oxide wear-out it would be reasonable to assume that SiO_2 on SiC cannot withstand the same oxide field as SiO_2 on Si
- During thermal oxidation of SiC a certain fraction of the semiconductor is consumed. This process releases carbon-containing molecules which need to be removed. If carbon gets trapped within the bulk of the SiO_2, it could have an impact on the intrinsic breakdown properties of the oxide and could act as a percolation path promotor [16]

The first point can be omitted for devices with an oxide thickness in the range of several tens of nanometers, as is typical for high power MOSFETs. In such devices, even for SiC, the gate tunneling current is negligible at the use conditions ($E_{Ox} < 3 – 5$ MV/cm). In this field-driven regime the commonly used linear E-model can explain voltage and temperature acceleration of oxide breakdown [22].
The second point can be eliminated by comparing the breakdown properties of thick SiO_2/SiC stacks where the oxide was either grown fully thermally or has been deposited and later densified. If trapped carbon species in the oxide were to have a significant impact on the breakdown characteristics, a fully thermally-grown oxide must show a lower breakdown field because much more carbon is released during its fabrication process. However, there is no experimental evidence for such a difference. Also SIMS or HR TEM studies could not find significant amounts of carbon in the bulk of thermally-grown oxides on SiC [23].
Based on these arguments, and due to overwhelming experimental evidence, it is concluded that the higher number of early failures in SiC based MOS structures is with a very high probability related to

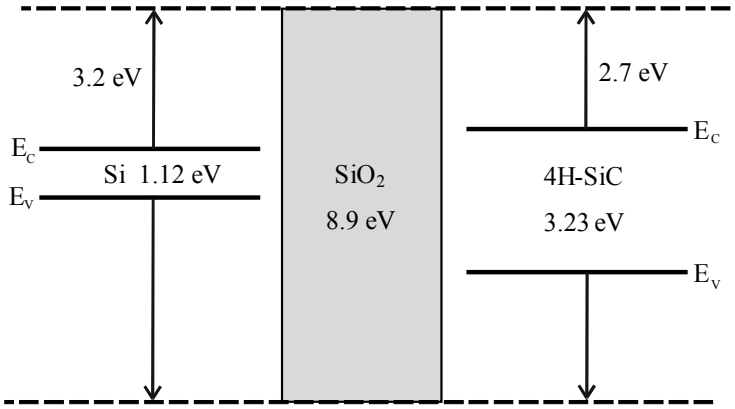

Fig. 6: Illustration of the band offsets between Si/SiO_2 and 4H-SiC/SiO_2

the higher electrical defect density of SiC which is consistent with the observed tendency of gradually improving gate oxide reliability of SiC MOS structures in the last decade. Accordingly the intrinsic quality and properties of SiO_2 on SiC and Si seem to be almost identical, and Si MOSFETs and SiC MOSFETs of the same area and oxide thickness can withstand roughly the same oxide field for the same time, provided the devices under test do not contain any defect-related impurities.

3.2. Oxide-thinning model and reduction of critical extrinsic defects

In the framework of Weibull statistics [24], identical intrinsic oxide properties of SiO_2 on SiC and on Si means that the intrinsic branches of Si and SiC MOSFETs with the same oxide thickness and area coincide (Fig. 7). The only remaining difference, then, is the much higher extrinsic defect density in the SiC MOS devices, which governs the failure rate during the chip lifetime. SiC is known to have a much higher substrate defect density and a much larger variety of defects compared to Si. These distortions may lead to local oxide thinning or small device regions of reduced oxide quality. Distorted regions may have the regular or even a larger physical oxide thickness but break down at a lower electric field compared to a defect free bulk oxide because of reduced dielectric strength. In the oxide-thinning model such a defective region can be treated as an electrically thinner bulk oxide that breaks down at the regular electric field [25].
Since the weakest link determines the lifetime of the chip, the electric field that triggers the break down under use conditions is given as:

$$E_{ox}^{on\prime} \approx \frac{V_{G,use}}{d'_{ox}} \tag{1}$$

where $E_{ox}^{on\prime}$ is the oxide field and d'_{ox} is the electrical oxide thickness of the thinnest extrinsic spot within the device. If there is no extrinsic defect present, d'_{ox} equals the bulk oxide thickness d_{ox} and the device appears in the intrinsic branch of the Weibull distribution. The reduced breakdown time t' of an extrinsic defect can be approximated using the linear E-model [22]:

$$t' = t_{intr} exp\left(\gamma\left[\frac{V_{G,use}}{d_{ox}} - \frac{V_{G,use}}{d'_{ox}}\right]\right) = t_{intr} exp\left(\gamma\left[E_{ox}^{on} - E_{ox}^{on\prime}\right]\right) \tag{2}$$

The constant γ in eq. 2 represents the voltage acceleration factor. The smaller the oxide thickness of the weakest extrinsic spot, the higher is the maximum field at $V_{G,use}$ and the earlier a breakdown occurs. With this model in mind, the extrinsic branch in the Weibull distribution can be understood as an ensemble of devices with extrinsic defects having different electrical oxide thicknesses $d'_{ox,i}$. In Fig. 7, the flat slope of the extrinsic branch is determined by the distribution of the electrical oxide thickness of the extrinsic defects. The slope of the intrinsic branch is much steeper but still finite due to statistical processes involved in the formation of the percolation path and due to slight device-to-device variations in bulk oxide thickness.
Assuming today's typical electrical defect density in SiC of 0.1 to 1 defects/cm^2, one would expect roughly 1 – 10 % extrinsics in an ensemble of SiC MOSFETs with an active gate oxide area of

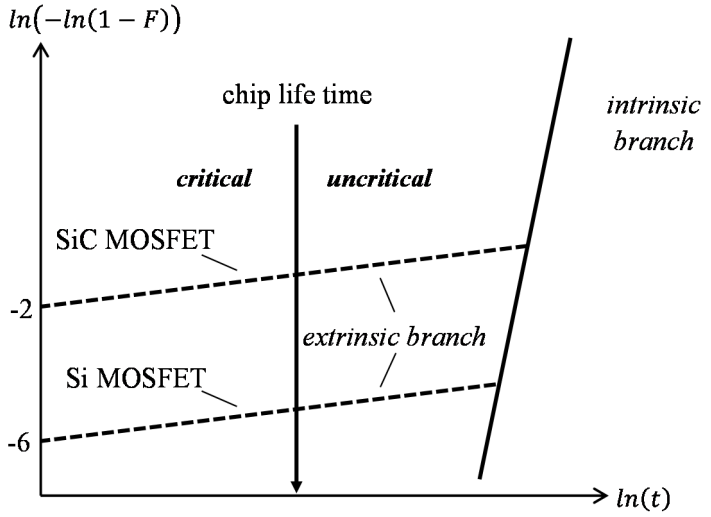

Fig. 7: Schematic representation of the extrinsic and intrinsic Weibull distribution for SiC MOSFETs and Si MOSFETs having the same oxide thickness and area [19]

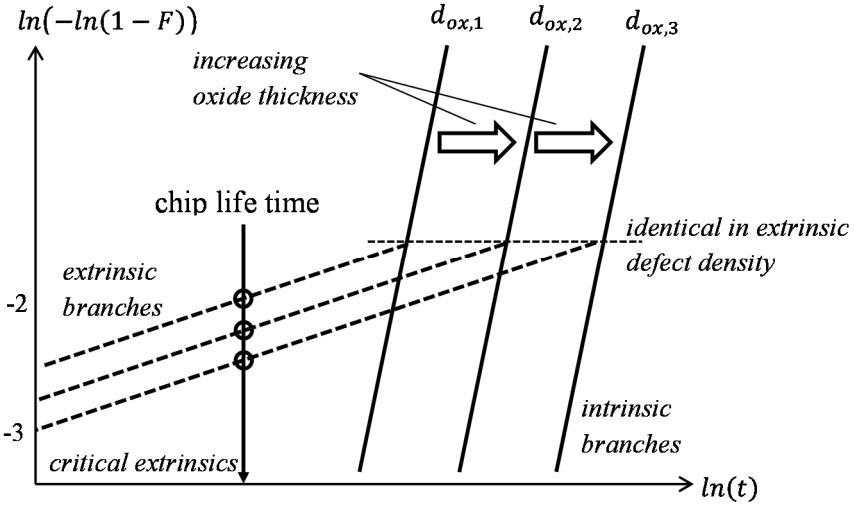

Fig. 8: Illustration of extrinsic and intrinsic branches when increasing the bulk oxide thickness ($d_{ox,1} < d_{ox,2} < d_{ox,3}$) [19]

10 mm^2. This means that 90 – 99 % of all SiC devices are perfectly fine and will show intrinsic gate oxide reliability. However, the remaining fraction of potentially early failures is, in spite of all improvements, still about 3 - 4 orders of magnitudes higher than for Si (see Fig. 7).
Now it is important to realize that not all devices which appear in the extrinsic failure branch of the Weibull distribution are necessarily critical - only devices which fail within the desired product life time are actually a reliability issue. Using the linear E-model [22], one can assign a device which fails extrinsically at time t_i' at a voltage $V_{G,i}$ a certain extrinsic oxide thickness $d'_{ox,i}$.

$$t_i = 3600 \cdot exp\left(\gamma E_{BD}^{1h} - \frac{\gamma}{d'_{ox}} V_{G,i}\right) \tag{3}$$

$$d'_{ox} = \frac{\gamma V_{G,i}}{\gamma E_{BD}^{1h} - ln\left(\frac{t_i}{3600}\right)} \tag{4}$$

In equations 3 and 4 the parameter E_{BD}^{1h} is the intrinsic SiO_2 breakdown field strength. It describes the average oxide field that SiO_2 can withstand for 1h, e.g. 10 MV/cm at 150°C. The thinner the oxide of the extrinsic spot, the higher the local electric field at $V_{G,use}$ and the earlier the device will fail. Assuming a typical chip life time of 20 years, a recommended gate use voltage of +15 V and an acceleration factor of γ = 3.5 cm/MV, equation 4 yields roughly 23 nm as upper oxide thickness limit for critical extrinsics. If the device will be operated at +20 V, this effective oxide thickness increases to 31 nm. By increasing the bulk oxide thickness the intrinsic life time is shifted into the future (Fig. 8). The same number of extrinsics is then distributed over a wider period of time and oxide thickness range, and the number of critical extrinsics is reduced.

3.3. Investigation of gate oxide failure rate

Long-time tests with a larger number of devices were performed in order to investigate extrinsic gate oxide failure rates in our devices with an asymmetric channel as depicted in Fig. 5. A constant gate bias stress at the elevated temperature of 150 °C was applied for three times 100 days. After each 100 days the gate-source voltage was increased by +5 V. Two groups of 1000 devices each were tested. The results for both groups are presented in Fig. 9. In the case of group 1 (green dots), the test started at a gate source voltage V_{GS} = + 25 V and ended at V_{GS} = +35 V, which is 20 V above the recommended use voltage of V_{GS} = + 15 V. Group 2 (blue dots) started at V_{GS} = +30 V and ended at V_{GS} = +40 V. The statistics of the failure rates of 2.9 % in group 1 and 6.5 % in group 2 fit well to the prediction using the linear E-Model [22]. An acceleration factor of γ = 3.9 cm/MV was determined for the best fit corresponding to the solid lines in Fig. 9. Extrapolation of this result assuming an expected 20 years life time of the device at use conditions, i.e. V_{GS} = 15 V at 150°C, the model predicts a failure rate of less than 1 FIT per die. This gives evidence of a typical gate oxide reliability which practically matches the one of IGBTs as used today in industrial applications [26].

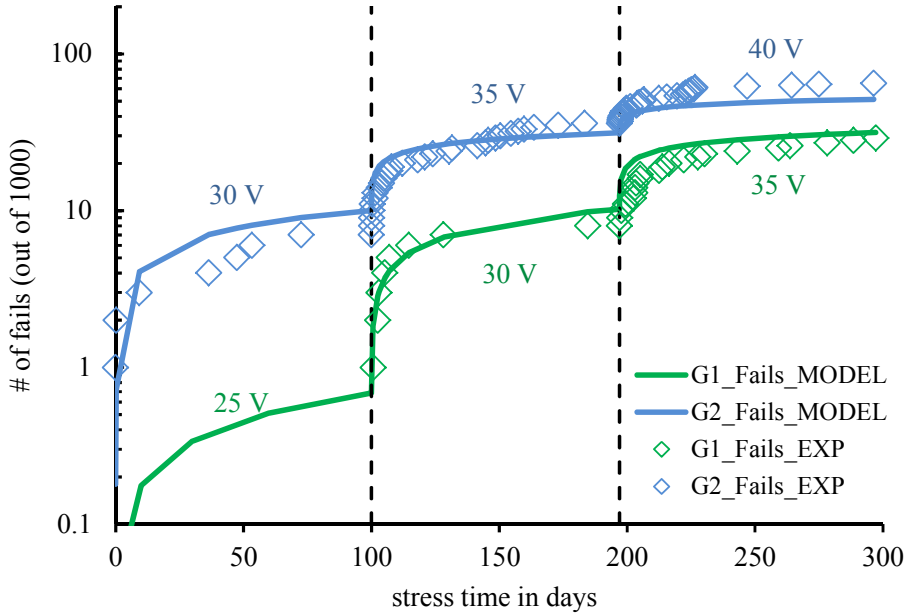

Fig. 9: Constant gate bias stress test results at 150°C. Solid lines represent the prediction by a linear E model.

4. Device characteristics

4.1. Static Performance

The proposed SiC MOSFET device is compatible with common standard gate-driver voltage levels of -5 V ... 0 V in the off-state and +15 V in the on-state, providing a typical on-resistance of $R_{DS(on)}$ = 45 mΩ at a drain current of I_D = 20 A and a temperature of T = 25 °C, and an $R_{DS(on)}$ = 70 mΩ at the elevated temperature of T = 175 °C. The threshold voltage has a typical value of V_{GSTH} = 4.5 V at T = 25 °C and decreases by about 6 mV/K to V_{GSTH} = 3.6 V at T = 175°C (I_D = 10 mA, V_{GS} = V_{DS}).
Fig. 10 gives the output characteristics of the device, while the transfer characteristics are shown in Fig. 11. The on-state current strongly depends on the applied gate voltage, and there is no current saturation visible within the measurement range, a feature which is common for SiC MOSFETs. Note that the slope of the curves is steadily decreasing with V_{DS} but does not fully disappear. At lower gate voltages V_{GS} the drain current I_{DS} is limited by the MOS channel. However, with the channel fully open at a reasonable value of the gate voltage V_{GS}, the drain current is now governed by the JFET region. Increasing the temperature changes the balance between the main contributors (MOS channel, JFET region and drift region) to the on-resistance. As the temperature coefficient of each of these contributors is also different, the share of the JFET to the overall on-resistance decreases. This effect is responsible for the more linear curves in on-state at higher temperatures.
The body diode shows a low forward-voltage drop of less than 4 V (V_{GS} = -5 V, channel off, I_D = 20 A, see Fig. 12). The curves with a gate-source voltage of V_{GS} = -5 V represent pure body diode operation. At zero gate voltage the junction barrier is lowered, which results in a reduced source-drain voltage V_{SD}. However, very low V_{SD} and linear characteristics are found if the channel is fully turned-on by applying +15 V to the gate. Now the on-resistance amounts 33 mΩ at V_{GS} = 15 V and 57 mΩ at 175°C, respectively. These values are lower compared to the 1st quadrant since the JFET resistance is significantly reduced due to the inverse polarity at the pn-junction. In order to keep static losses in the reverse conduction mode low, synchronous rectification is recommended by turning on the channel after an appropriate interlock time.
Fig. 13 shows the temperature dependence of the on-resistance and of the threshold voltage. The on-resistance increases by 70 % from 25°C to 175°C and as such shows the commonly found significant dependence on temperature as expected for MOSFET devices with small defect densities at the gate oxide interface. The measured positive temperature coefficient is also beneficial for the paralleling of devices. The overall temperature behavior is determined by the temperature-dependent properties of the MOS channel, the JFET region and the drift layer. The MOS channel has a negative temperature

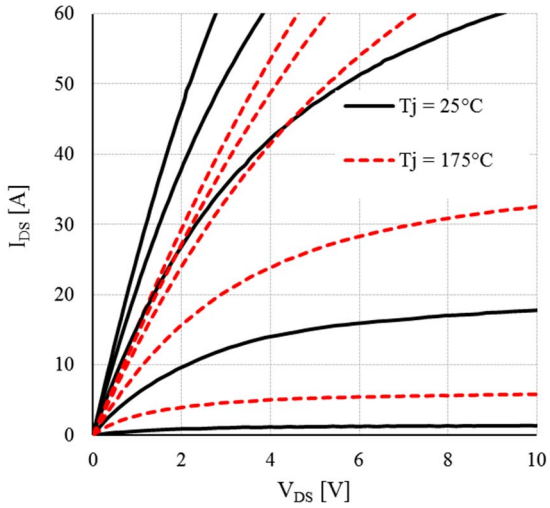

Fig. 10: Output characteristics
(V_{GS} = 7, 10, 13, 15, 17 V)

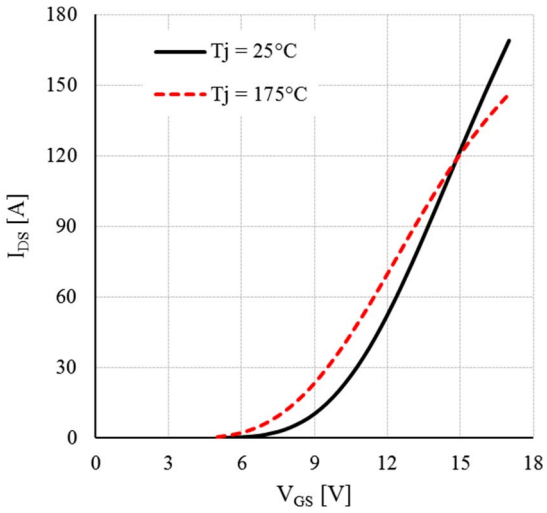

Fig. 11: Transfer characteristics
(V_{DS} = 20 V)

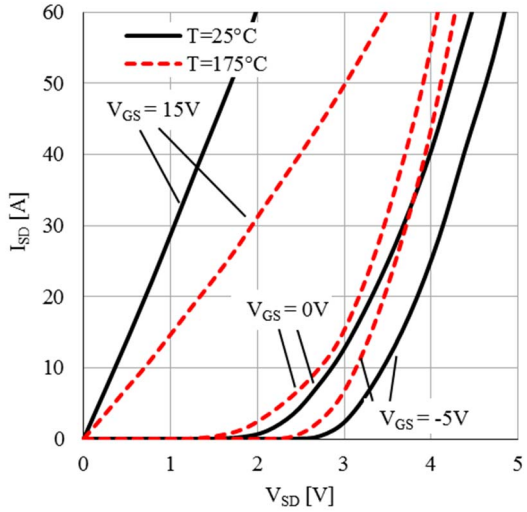

Fig. 12: Typical 3rd quadrant characteristics at 25°C (solid) and 175°C (dashed), V_{GS} = +15V, 0 V and -5V

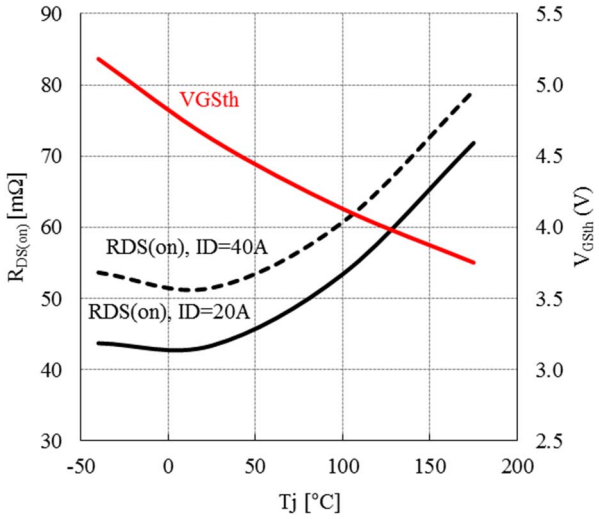

Fig. 13: Typical temperature dependence of $R_{DS(on)}$ at I_D = 20 A, 40 A and of V_{GSth} (V_{GS}=V_{DS}, I_D = 10mA)

characteristic mainly due to the threshold voltage decreasing with temperature whereas the n-type doped drift zone has a positive temperature coefficient. The increase of the resistance with load current is again explainable by the JFET contribution.

4.2. Dynamic behavior

The capacitances and their dependencies on the drain-source voltage give key information about the switching behavior (Fig. 14). The Miller capacitance C_{rss} and the linked Miller charge Q_{GD} are quite small. This makes parasitic re-turn-on easy to suppress and avoids related losses. Turn-on and turn-off energies for different load currents, temperatures and different free-wheeling devices are depicted in Fig. 15 and Fig. 16. The tests were either done in a half-bridge configuration using the internal body diode of the SiC MOSFET, or in a chopper configuration with an external SiC Schottky Barrier Diode (SBD).

The turn-on energies E_{on} dominate the switching losses and can be minimized independent of the temperature if the MOSFET is used in combination with an SBD diode (both curves in Fig. 15 overlap). Compared to the E_{on} of the MOSFET in a half-bridge configuration, 30-50 % of the losses can be saved. In a half-bridge configuration the body diode is active and shows an increasing impact with both a larger load current and a higher temperature. This is a bipolar effect linked to the build-up

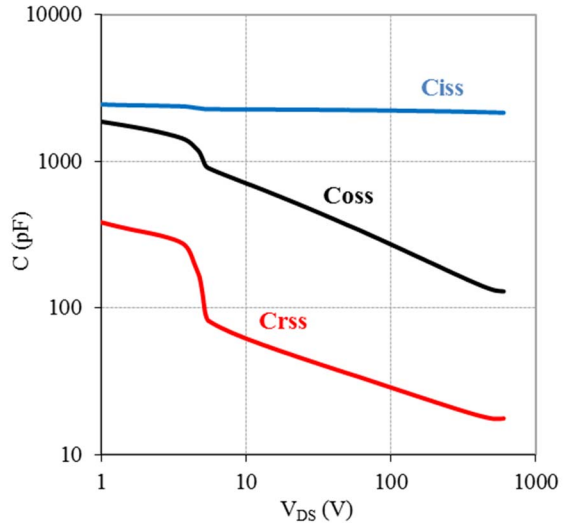

Fig. 14: Small signal capacities C_{iss}, C_{oss}, C_{rss} as function of V_{DS} measured at 1 MHz, V_{GS} = 0 V

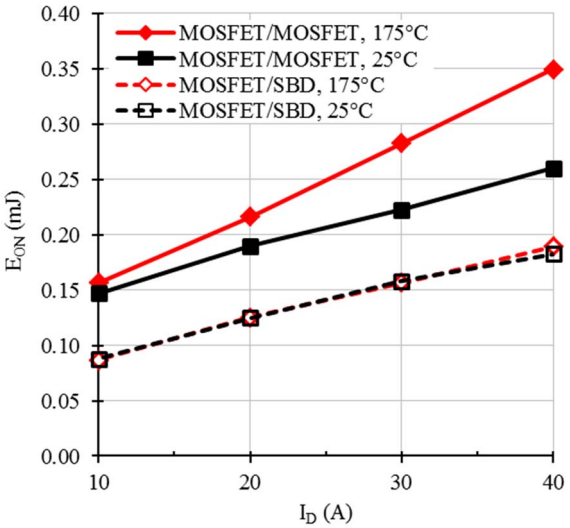

Fig. 15: Turn-on energy as function of drain current, measured in TO-247-4 pin (V_{DS} = 800 V, R_g = 2.2 Ω, V_{GS} = -5 V / +15 V)

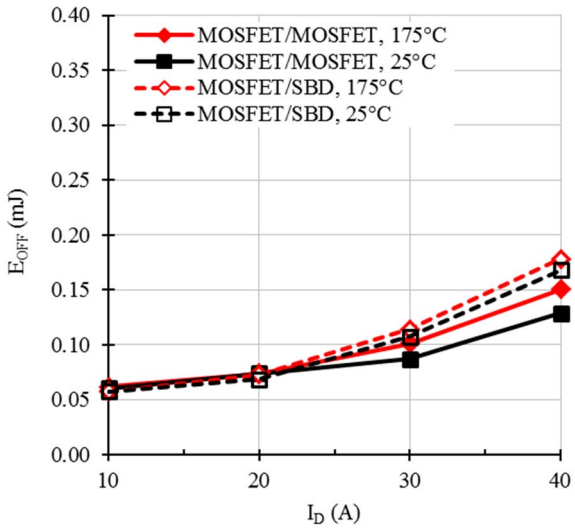

Fig. 16: Turn-off energy as function of drain current, measured in TO-247-4 pin (V_{DS} = 800 V, R_g = 2.2 Ω, V_{GS} = -5 V / +15 V)

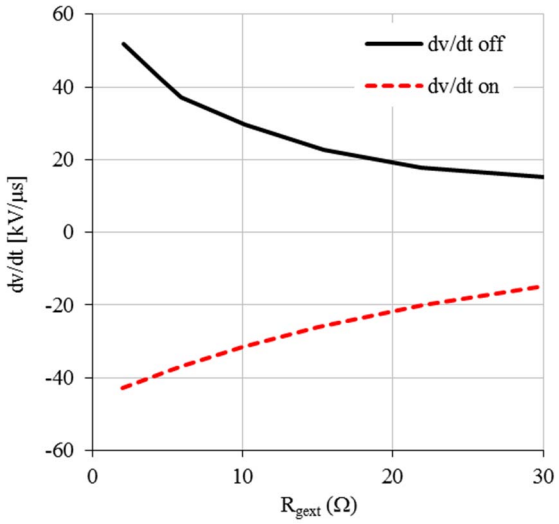

Fig. 17: Max. dv/dt vs. external gate resistor R_{Gext} (V_{DS} = 800 V, I_D = 20 A, T = 175 °C)

of a reverse recovery charge. However, the absolute values at the rated current of 20 A are still very small compared to 1200 V Si IGBTs. In general a reduction of the switching losses is feasible by minimizing the shared parasitic source inductance, e.g. by using the TO-247-4pin which provides an additional Kelvin source lead connected to the driver, a measure also being implemented in power modules, or by replacing through-hole packages with SMD devices in the future.

Fig. 17 presents the corresponding voltage slopes dv/dt, indicating that the dv/dt is fully controllable by the gate resistor value during turn-on and turn-off. This allows addressing any dv/dt limitation set by the power electronic system, however switching losses will increase due to the nature of hard-switching transitions.

Fig. 18 – Fig. 21 show a few measured waveforms in a half-bridge configuration using the internal body diode. Two different values for the gate resistor are used. The waveforms clearly indicate the impact of the gate resistor on the switching speed. In contrast to IGBTs there is no tail current since no bipolar charge is built-up when the MOSFET channel is conducting. As such the dynamic behavior is mainly governed by the capacitances of the MOS structure linked to the extension of the space-charge region.

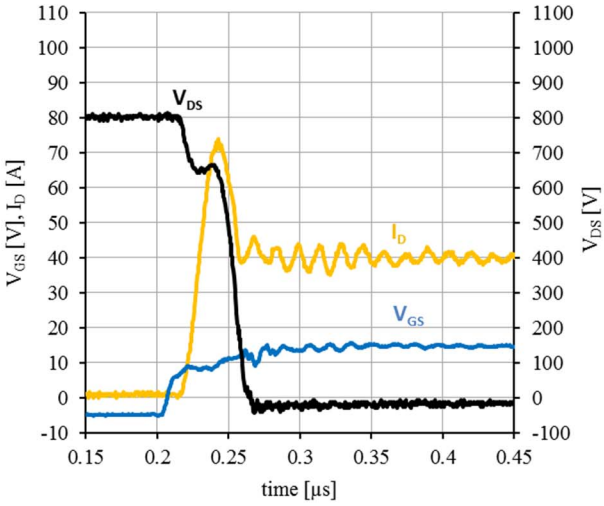

Fig. 18: Turn-on waveform in a half-bridge using the internal body diode, measured in TO-247-3pin (V_{DS} = 800 V, I_D = 40 A, R_G = 6.0 Ω, T_j = 175°C, V_{GS} = -5 V / +15 V)

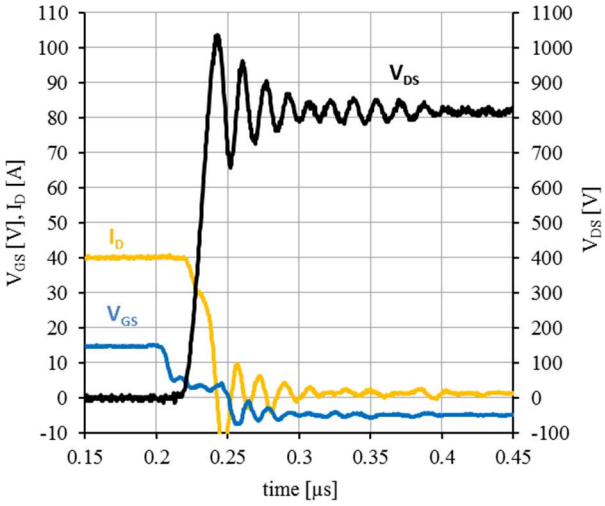

Fig. 19: Turn-off waveform in a half-bridge using the internal body diode, measured in TO-247-3pin (V_{DS} = 800 V, I_D = 40 A, R_G = 6.0 Ω, T_j = 175°C, V_{GS} = -5 V / +15 V)

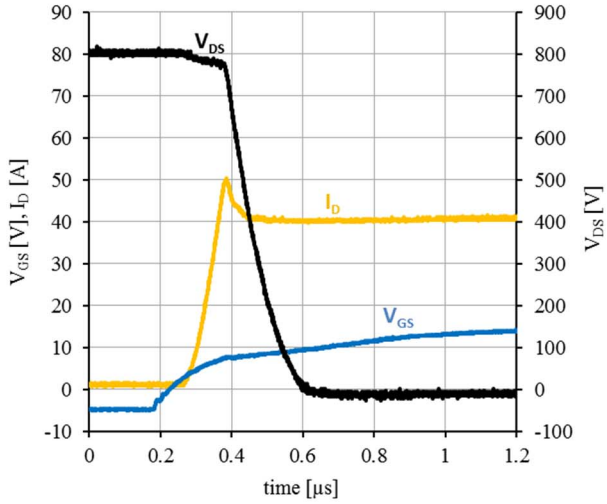

Fig. 20: Turn-on waveform in a half-bridge using the internal body diode, measured in TO-247-3pin (V_{DS} = 800 V, I_D = 40 A, R_G = 30.1 Ω, T_j = 175°C, V_{GS} = -5 V / +15 V)

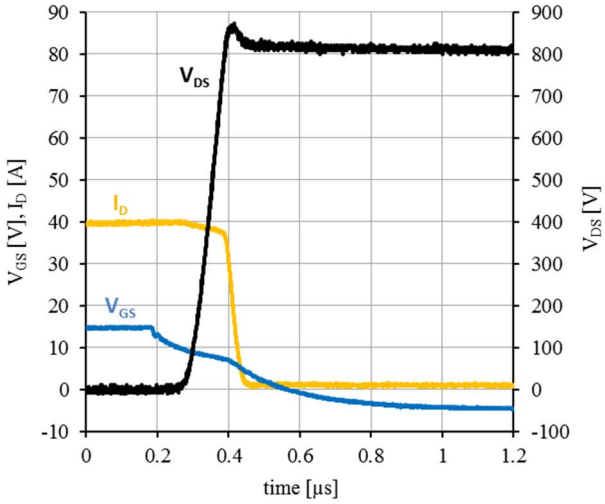

Fig. 21: Turn-off waveform in a half-bridge using the internal body diode, measured in TO-247-3pin (V_{DS} = 800 V, I_D = 40 A, R_G = 30.1 Ω, T_j = 175°C, V_{GS} = -5 V / +15 V)

4.3. Ruggedness

Power devices need to be robust to withstand critical application conditions such as single short-circuit or avalanche events. Fig. 22 shows the waveforms of a typical short-circuit test. The device is turned-on / off between -5 V and +15 V at 800 V bus voltage and a case temperature of 175°C (i.e. short circuit type 1). After 5 µs the device was able to turn-off safely.

Standard UIS (unclamped inductive switching) measurements revealed a good avalanche ruggedness of the device. UIS tests for a given inductance driving the avalanche current are repeated with stepwise increased current value until the device is destroyed. This procedure is rerun for several values of the avalanche inductance. The result of this characterization is presented in Fig. 23, indicating the dependence of single-pulse avalanche destruction current density and energy on the area-normalized value of the avalanche inductance. The measurements do not reveal a weakness with respect to avalanche ruggedness. An activation of the parasitic BJT can be excluded since the built-in voltage of the respective pn-junction of 2.7 V at room temperature is very high. Fig. 24 shows the

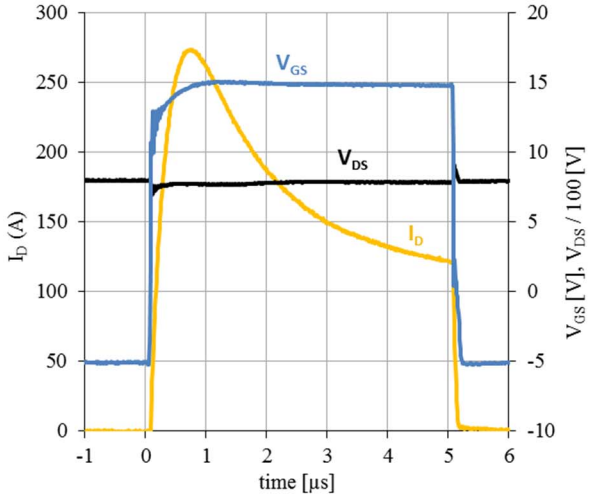

Fig. 22: Typical short circuit waveforms (Tc = 25°C, R_G = 7.9 Ω, V_{DC} = 800 V, V_{GS} = -5 V / +15 V, package TO-247-4 pin)

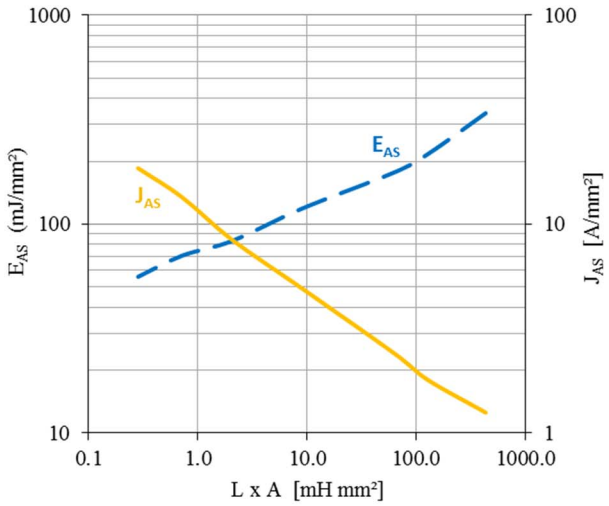

Fig. 23: UIS test single-pulse destruction current density and destruction energy depending on avalanche inductance

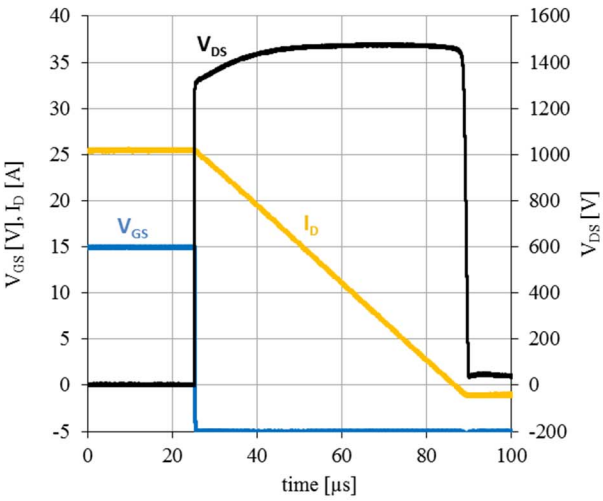

Fig. 24: UIS test waveform (T_C = 25°C, V_{DC} = 50 V, L = 3.5 mH)

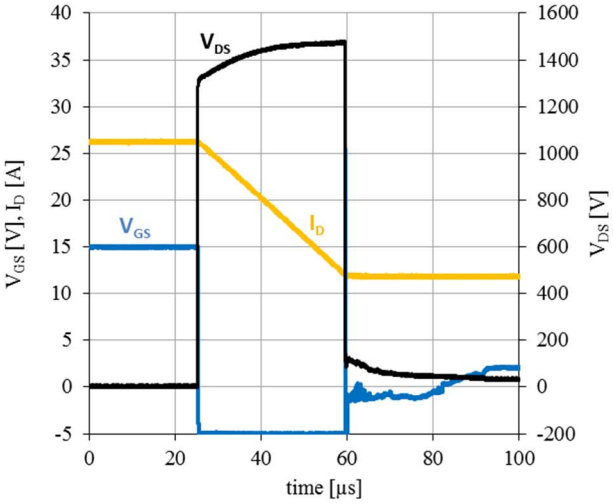

Fig. 25: UIS test waveform at destruction (T_C = 25°C, V_{DC} = 50 V, L = 3.5 mH)

waveform of the last UIS test which did not destroy the device while Fig. 25 gives the measurement of the destructive test using the next higher current level. The presented results and waveforms indicate an energy-related destruction mechanism as the drain-source-voltage increases over time. This is a consequence of the self-heating of the device due to the dissipated energy which is linked to a lower avalanche generation rate, leading to a higher breakdown voltage. The device fails during the destructive test when the drain-source-voltage reaches its maximum. This means that also the device temperature reaches its highest value which triggers the destruction mechanism.

In case of silicon devices, the amount of dissipated energy is usually high enough to meet the intrinsic temperature of the semiconductor material [27]. Once this point is reached, thermally generated carriers exceed the extrinsic dopant concentration. Now the device begins to behave as an intrinsic semiconductor material with conduction properties entirely governed by temperature and not by doping. If the current continues to flow, the device will be destroyed. In case of the SiC MOSFET, an estimation of the temperature increase due to the dissipated electrical energy yields a junction temperature in the range of 600°C … 700°C. This value is much lower than the intrinsic temperature of SiC, consequently it is not the semiconductor material itself imposing the limit with respect to energy-related destruction.

5. Conclusion

The new CoolSiC™ MOSFET based on an asymmetric trench cell concept combines excellent reliability features with attractive low on-resistance, low threshold voltage and good ruggedness while offering the use of a standard gate drive voltage of 15 V. With respect to gate oxide reliability considerations, it was possible to utilize a lot of know-how available from silicon and combine it with SiC specific features. Investigating the reliability of the developed gate oxide by long-term tests using a large population of devices verifies that the device has a Si-IGBT like gate oxide reliability and fulfills typical requirements for industrial applications. Its temperature behavior makes the device easy to operate, in particular for operation in parallel. The switching behavior can be fully controlled by the gate resistor and good device ruggedness is provided.

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