A new Power MOSFET Generation designed for Synchronous Rectification

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Abstract

Low-voltage MOSFETs are widely used in the synchronous rectifying stages of power supplies. To allow a high efficiency in light-load conditions, the power MOSFET not only needs to meet general requirements like low on-resistance, low gate charge and good avalanche capability, but must also have a low output capacitance and low reverse-recovery charge. The paper shows how those requirements were met in our newest generation of power MOSFET starting with the 60 V class.

Introduction

Several years ago the upcoming 80PLUS® requirements for SMPS (switched-mode power supply) forced the designers of power supplies to rethink the concept of the secondary side rectification. At that time conventional diodes with a forward voltage drop of roughly 0.5 V were used. In combination with large output currents these diodes generate high conduction losses, leading to a poor efficiency level of the SMPS at high output power. The change to synchronous rectification by using standard MOSFETs with low $R_{DS(ON)}$ was the solution to increase the efficiency level above 80 % at 20 %, 50 % and 100 % of the output power. Further design steps like improved PCB layout, enhanced snubber networks for better spiking behavior of the MOSFET or going for lower $R_{DS(ON)}$ increased the efficiency level to a peak of around 90 %.
However, the current 80PLUS platinum certification requires much more. The efficiency for single output PSUs (power supply units) with an AC input voltage of 230 V (e.g. server PSU) has to be above 90 %, 94 % and 91 % at respectively 20 %, 50 % and 100 % of the output power. An optimization at full load could be enabled by using the smallest available $R_{DS(ON)}$ for the SR (synchronous rectification) MOSFET, but this approach does not allow the highest performance to be reached at low output power. To reach or exceed the 80PLUS platinum certification in the coming years, it is essential to have MOSFETs for synchronous rectification which have a well balanced ratio between switching losses and conduction losses. At the same time the absolute loss values need to be extremely low.

Application requirements

Basics of Synchronous Rectification

To design a MOSFET which is perfectly suited to synchronous rectification, this application needs to be analyzed in-depth to get an understanding of which parameters are important. In the following a short overview is given, a detailed analysis is presented in a separate paper [1].
Power losses in the SR MOSFET must be separated into load dependent conduction losses and constant switching losses. Conduction losses are determined by the $R_{DS(ON)}$ of the switch. They increase with increasing output load of the power supply. On the other hand the switching losses are constant over the whole output load, and are mainly determined by the gate charge Q_G and the output

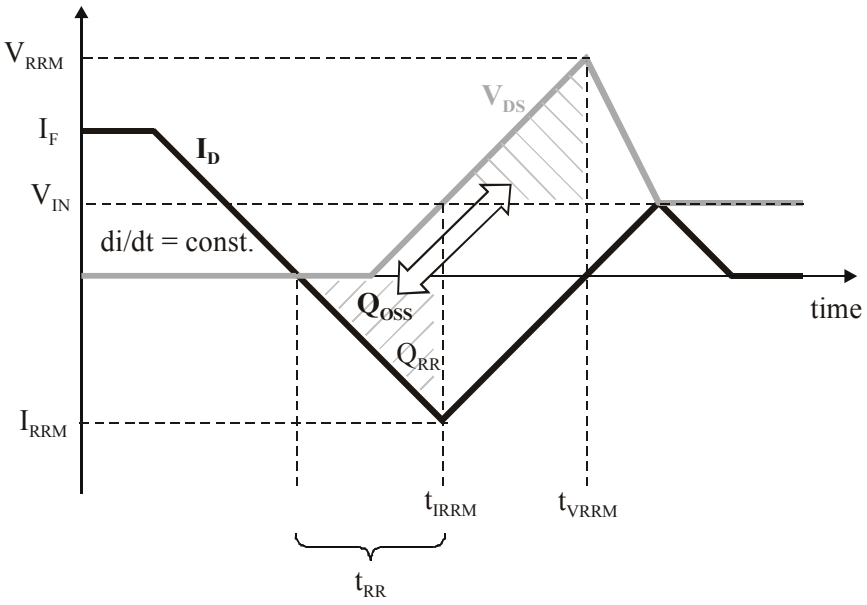

Fig. 1: Simplified model of the turn-off process of a Synchronous Rectification MOSFET

charge Q_{OSS}. The gate-source-capacitance C_{GS} needs to be charged up to the gate driving voltage at each turn-on and will be discharged to ground at each turn-off.
Considering the turn-off process, the stored charge Q_{RR} of the body diode must be removed and the output capacitance C_{OSS} has to be charged up to the secondary side transformer voltage, the input voltage of the SR stage as explained in Fig. 1. This process results in a reverse current peak I_{RRM} which is linked to the overall inductance of the commutation loop. The energy stored in this inductance is transferred to the output capacitance as soon as the drain-source-voltage of the MOSFET V_{DS} exceeds the input voltage V_{IN} with the voltage spike carrying this energy. The amount of energy is defined by the reverse-recovery charge stored in the body diode Q_{RR} and the charge stored in the output capacitance Q_{OSS} up to the transformer voltage V_{IN} and is lost every switching cycle.
A high output capacitance C_{OSS} does not only generate power losses but also causes a large reverse current peak as shown schematically in Fig. 1. The higher the reverse current peak I_{RRM}, the higher the rate of voltage rise dv/dt, and thus the turn-off voltage spike, will be. This high dv/dt can also trigger a dynamic re-turn-on of the MOSFET by raising the gate voltage above the threshold voltage due to the capacitive voltage divider C_{GD}/C_{GS}. To prevent this a small output capacitance C_{OSS}, a non-critical ratio C_{GD}/C_{GS} and a narrow tolerance of all MOSFET capacitances are essential.

Optimization towards highest efficiency

To optimize the SR MOSFET for the highest efficiency, a well balanced ratio between switching losses and conduction losses must be found. At low output loads the conduction losses only play a minor role while switching losses are dominant. For higher loads the weighting of the losses is the other way around. To calculate the losses and to get an indication how the technology will perform in the system, different figures-of-merit (FOM) need to be considered [2,3]. The FOM_G is the product of the $R_{DS(ON)}$ and the Q_G, while the FOM_{OSS} is the product of $R_{DS(ON)}$ and Q_{OSS}. As the capacitances of a MOSFET are inverse proportional to the $R_{DS(ON)}$, this product is fixed over the whole $R_{DS(ON)}$ range of a given technology. As illustrated in Fig. 2 the conduction losses increase linearly with higher $R_{DS(ON)}$. On the other hand switching losses increase substantially at low $R_{DS(ON)}$ values. Considering the total power losses, a local minimum is found. At precisely this point, marked with a black dot in Fig. 2, the MOSFET generates the lowest losses in a given system and therefore the highest efficiency is found. Further optimization of an SR system cannot be done with this given MOSFET technology. Consequently, the main goal of the new SR MOSFET generation development was to move this point of minimum losses to the bottom left corner in Fig. 2. This can be achieved by a further massive decrease of the FOM_G, which means a reduction of switching losses and a reduction of conduction losses at the same time. This measure can raise the whole system efficiency both at low output power and at high output power, making it easier to meet the new energy efficiency requirements.

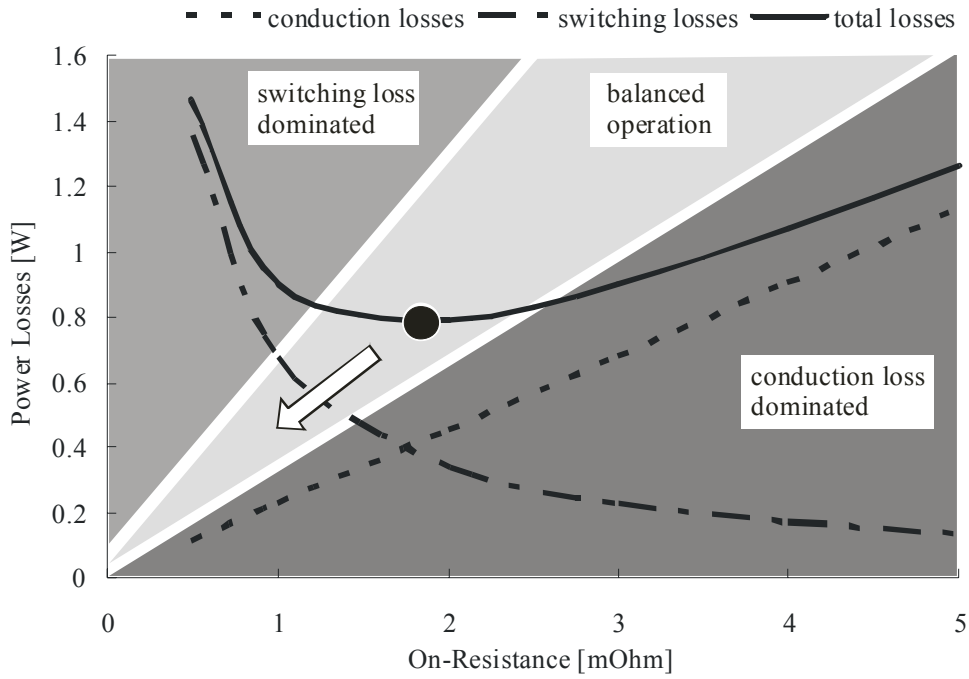

Fig. 2: Power losses per device vs. on-resistance in synchronous rectification for a given MOSFET technology (V_{IN} = 30 V, V_{GS} = 10 V, I = 15 A f = 125 kHz)

Device design optimization

Device Concept

Several years ago, the first generation of power MOSFET employing the compensation principle based on a field-plate concept was introduced [4]. The basic principle to realize an area-specific on-resistance well below the 1D silicon limit is similar to the charge-compensation in super-junction devices like the CoolMOS™, as schematically shown in Fig. 3a. Here the compensation of n-drift region donors is realized by acceptors located in p-columns. In field-plate type devices, an isolated field-plate provides the mobile charges required to compensate the drift region donors under blocking conditions as indicated in Fig. 3b. Compared to a device using a simple planar pn-junction, the electric field now also has a component in the lateral direction. Fig. 4 indicates the basic differences in the electric field for a simple pn-junction and for the case where a field-plate compensates the donors in the drift region. As can be seen the field-plate principle leads to an almost constant field distribution in vertical direction, thereby reducing the necessary drift region length for a given breakdown voltage. In addition, the drift region doping can be increased. Both measures, the formation of a super-junction as well as a field-plate structure, can significantly reduce the on-state resistance.

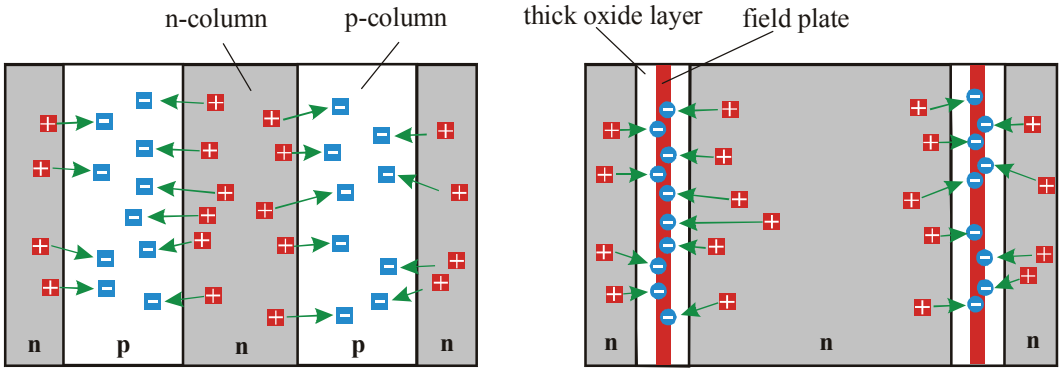

Fig. 3: a) Compensation by p-and n-columns b) Compensation using a field-plate

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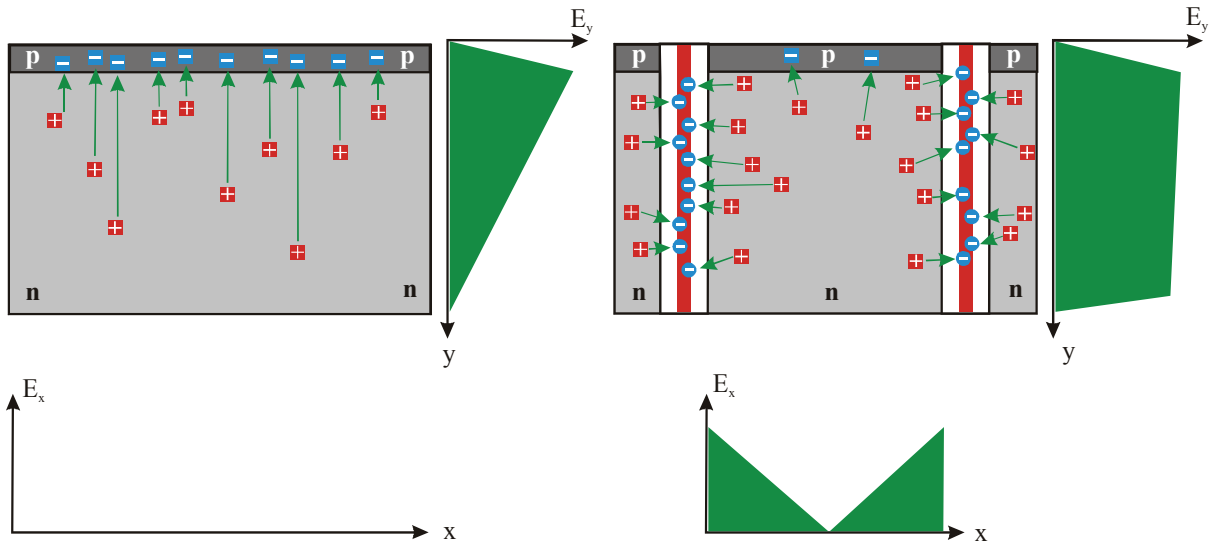

Fig: 4 a) Electric field for a pn-junction b) Electric field for a field-plate structure

Furthermore, the field-plate electrode is connected to the source electrode of the MOSFET and the gate is formed by a separate electrode. Therefore such a device structure not only offers an outstanding area-specific on-resistance, but also a low gate-charge.
Fig. 5 indicates the reduction of the on-resistance which can be achieved. It compares the resistance of the drift region, currently the major part contributing to the total conduction losses of the device, for the case of an ideal pn-junction and for a compensation device using field-plates. The values for the compensation device are either estimated using a simplified 1D model or calculated using 2D device simulation [5].

Improvement of output charge and on-resistance

Despite all the advantages the introduction of charge-compensation is inevitably linked to an increase of the output capacitance C_{OSS} and the output charge Q_{OSS} due to the increased doping density compared to a standard MOSFET. Here it is useful to consider the previously defined Figure-of-Merit $FOM_{OSS} = Q_{OSS} \times R_{DS(ON)}$ since from an application point of view the output charge for a given on-resistance is of interest. A simple optimization towards the lowest possible area-specific on-resistance by using a smaller cell pitch will lead to a degradation of the FOM_{OSS}. Alternatively, a reduction of the Q_{OSS} is obviously possible by a further reduction of the drift region length and a lower drift region doping, and/or a decrease in the cell density (i.e. increasing the trench width etc.). Unfortunately, most

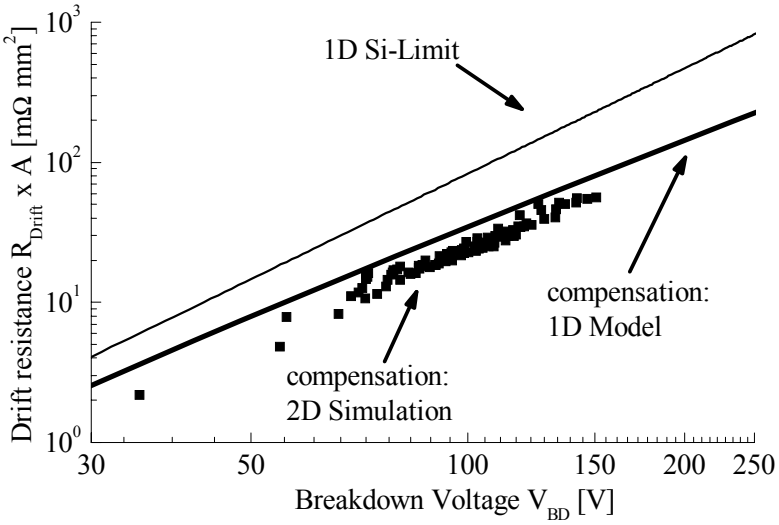

Fig. 5: Drift region resistance vs. breakdown voltage

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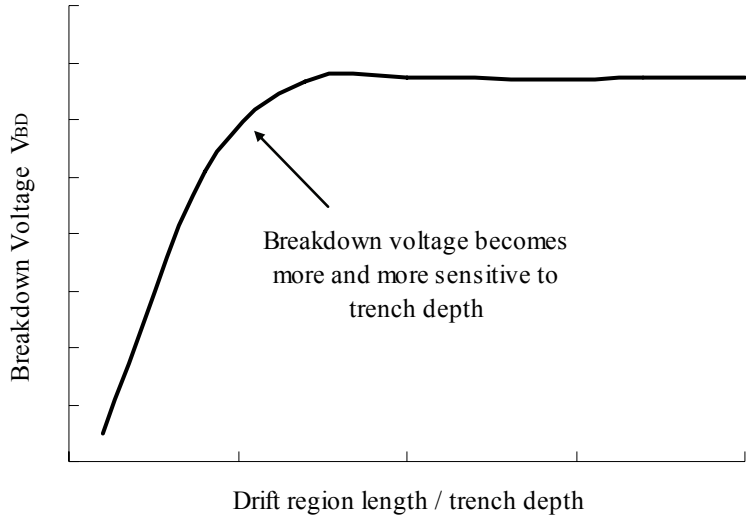

Fig. 6: Breakdown voltage dependence on trench depth / drift region length for constant doping level

of these measures will lead to a degradation of the area-specific on-resistance and will also affect the breakdown voltage of the device within a given technology. Fig. 6 shows the fundamental dependency between the breakdown voltage and the trench depth and the linked drift region length at a constant drift region doping. As can be seen the realized breakdown voltage remains almost constant until the trench depth falls below a certain limit. Further reduction of trench depth and drift region length results in an increasing degradation of the breakdown voltage. It is clear that process-related deviations of the trench depth must be appropriately considered and that for the highest yield in manufacturing within a given technology it looks best to chose a target design which always stays on the constant branch of the shown dependency.
However, the key for further improvement of the MOSFET towards the previously indicated requirements is to realize a design left of the constant branch of the breakdown voltage dependency depicted in Fig. 6. Due to the increased sensitivity of the breakdown voltage on trench depth and drift region length, the main measure for being able to not only reduce the FOM_{OSS} but also the area-specific on-resistance and the gate-charge for faster switching is the use of more advanced manufacturing processes. New manufacturing tools and better lithography allow for smaller structures and, essentially, lower tolerances through an improved process control.
As an example, the reduction of process-related deviations in the trench depth from ±15% to only ±5%

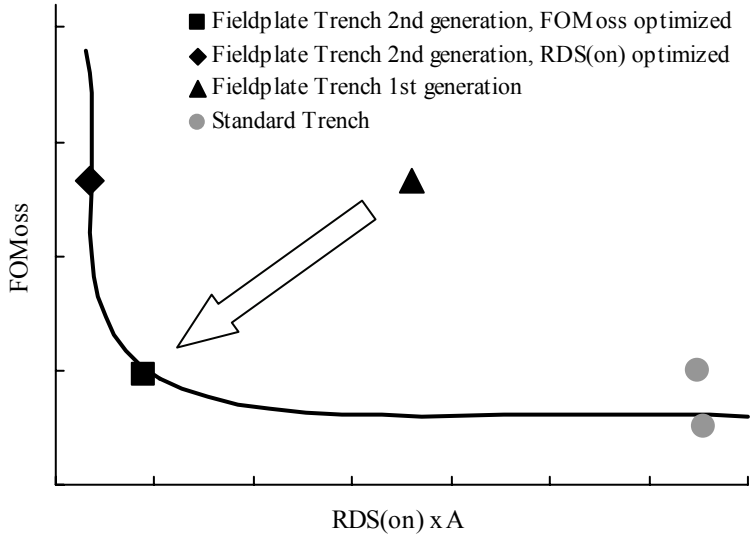

Fig. 7: Comparison of device performance of 1st and 2nd generation of field-plate trench MOSFET and standard trench MOSFET devices in the 60 V class

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allows a reduction of the target trench depth of 10%. Consequently the output charge is reduced by 10% while the FOM_{OSS} becomes even smaller since the on-resistance is also lower due to the shorter drift length. Of course, the applicable measures are not limited to the control of the trench depth. The use of the improved manufacturing setup also allows the reduction of the channel length, which further contributes to an improved on-resistance. On the other hand, better control of the trench width results in smaller variation of the mesa width, and therefore the doping-related charge shows fewer fluctuations. Since this charge must be compensated by the field-plate, this leads to a better control of the breakdown voltage, giving more room to move to the left of the dependency shown in Fig. 6.
In summary, improvements in the manufacturing tools and a consequent optimization of the important manufacturing processes allows for a clear reduction of the FOM_{OSS}. The area-specific on-resistance and the gate charge can also be further reduced at the same time.
Fig. 7 gives a comparison of the FOM_{OSS} vs. $R_{DS(ON)}$ x A of the upcoming new device generation with the predecessor generation and devices employing a standard trench concept. Despite the clear improvement towards both, FOM_{OSS} and $R_{DS(ON)}$ x A, compared to the predecessor generation there are two particularly interesting facts to note. Firstly, the strong reduction of the output-charge results in only a minor increase in the area-specific on-resistance compared to what would be achieved by a straightforward reduction of the on-resistance. Secondly, the FOM_{OSS} of an optimized field-plate compensation device is as good as that of devices employing a standard trench.

Switching performance and avoidance of dynamic turn-on

As the proposed device technology is intended for use in fast switching applications, the absolute value of the gate-drain-charge Q_{GD} and its variation is also important. The gate-drain charge Q_{GD} (also known as the Miller charge) and the overall gate resistance R_G are the main factors controlling the switching speed of the device. A small gate-drain-charge Q_{GD} is therefore advantageous, but the variation of this parameter over the whole manufacturing process should also be small. This is especially important where devices are connected in parallel with each other, but a small range of the Q_{GD} value also allows the minimization of safety margins. Here the performance of the new technology also benefits from the previously discussed improvements to the manufacturing process and equipment. The better process control and the optimized device geometry results in a much smaller range of the Q_{GD} compared to the predecessor technology as indicated in Fig. 8.
However, the use of power MOSFETs for fast switching applications comes with additional risks. The most typical one is the dynamic turn-on. Observed mainly, but not exclusively, in hard-switching topologies, very large dv/dt-values from drain to source may occur when the device starts to block. This dv/dt couples to the gate via the capacitive voltage divider C_{GD}/C_{GS} and could result in a dynamic turn-on of the device as explained in Fig. 9. In this case, a short circuit forms. Consequently, this leads to largely increased losses in the MOSFET and also in other affected devices, such as the transformer

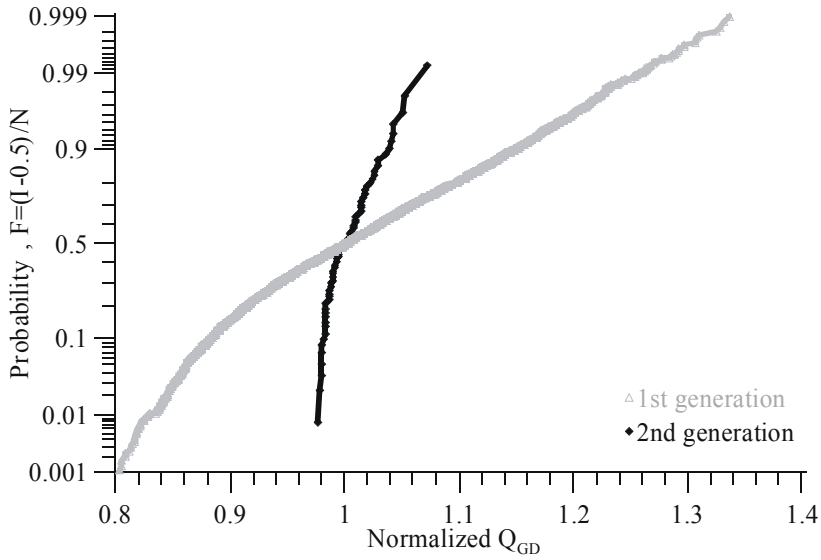

Fig. 8: Comparison of the range of the gate-drain charge Q_{GD} for 1st and 2nd device generation

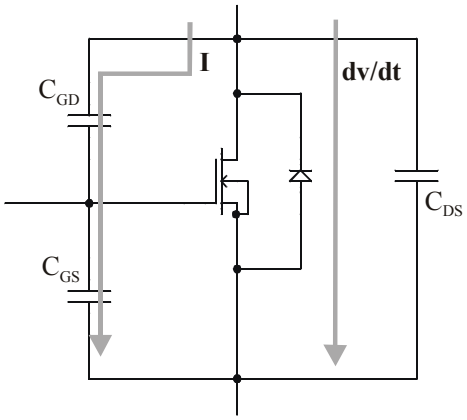

Fig. 9 : Dynamic turn-on of a MOSFET by large dv/dt

in a synchronous rectifier. The vulnerability of a given MOSFET technology to dynamic turn-on can be estimated using the following condition:

$$\frac{Q_{GD,crit}}{V_{TH,min}\ C_{GS}} < 1 \tag{1}$$

with

$$\int_0^{V_{DS,max}-V_{TH,min}} C_{GD}\ dV_{GD} = Q_{GD,crit} \tag{2}$$

Here, $V_{TH,min}$ is the smallest specified threshold voltage, $V_{DS,max}$ is the maximum drain-source-voltage during switching (e.g. the voltage peak) and $Q_{GD,crit}$ refers to the critical gate-drain-charge. Consequently, the gate-drain-charge of the MOSFET should be lower to avoid this effect.
As in the case of the predecessor technology, the necessary care was taken that the condition given by Eq. 1 is safely fulfilled and that no dynamic turn-on is found even for the very high dv/dt which might occur in optimized, low-inductance circuits.

Device performance in target applications

Simulation and measurement setup

To verify if the theory discussed above is applicable in a real application, a test measurement was done in a laboratory setup. To obtain meaningful results, a 750W / 12V server power supply unit with secondary side synchronous rectification, commercially available on the market, was taken for verification. The topology is a phase-shift, full-bridge rectifier on the primary side [6] with hard-switched, center-tapped synchronous rectification stage on the secondary side as schematically shown in Fig. 10. To get comparable results it is essential always to have the same external laboratory conditions, such as constant temperature and use of the same measurement instruments for minimized tolerances. For the measurement of the AC input of the power supply, a Siemens power analyzer type B6040 was used. The output voltage was measured with a precision data acquisition unit type Agilent 34970A, the current was logged using a high-current shunt resistor. To correctly analyze the voltage overshoot of the SR MOSFET, it is important to measure the signal as near to the package as possible, but not on the PCB. This avoids any influence of the parasitic stray inductances which can heavily affect the voltage signal due to the high di/dt environment.
Since it is essential in the development of a new technology to know as early as possible how the new device behaves in the target application, a simplified synchronous rectification stage was implemented in a mixed-mode simulation circuit using Medici™ [7]. Both SR MOSFETs in this circuit as shown in Fig. 10 are modeled by their full 2D structures. The input voltage V_{IN} reflects the voltage of the secondary side of the transformer. A safe dead-time of 250ns was chosen for the gate voltages V_{GS1}

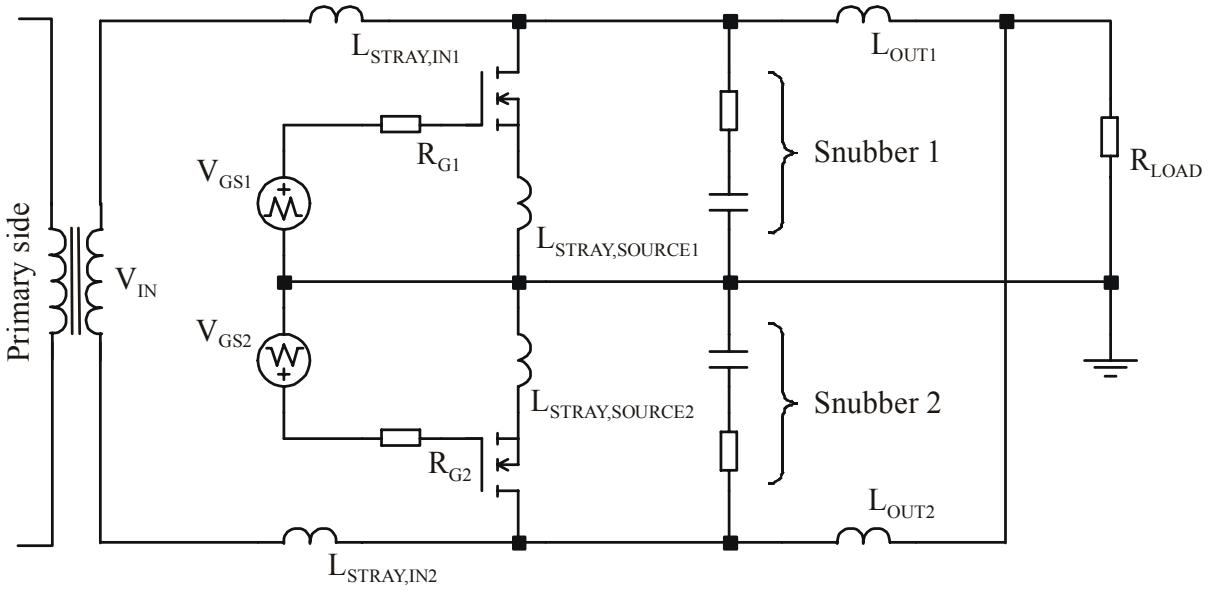

Fig. 10: Basic circuit for a hard-switched, center-tapped synchronous rectification stage

and V_{GS2}. The simulations carried out reproduced the situation for a given operating point. The following parameter values were used in the simulations: $R_{G1/2} = 2\ \Omega$, $L_{OUT1,2} = 10\ \mu H$, $L_{STRAY,IN1,2} = 20$ nH, $L_{STRAY,SOURCE1,2} = 2$ nH, $R_{Snubber1,2} = 2.7\ \Omega$, $C_{Snubber1,2} = 10$ nF.

Simulation of voltage overshoot

Fig. 11 compares the voltage overshoot (absolute values) in a synchronous rectifying stage for the new 60 V MOSFET and the predecessor device as a result of simulations and measurements in a real test circuit. Due to the lower output charge of the new device generation the voltage overshoot was clearly reduced over the full output current range. These results confirm the previously discussed measures to improve the device performance.
While the reduction in the overvoltage is equal in the measurement and the simulation, the absolute values show a marked difference. The reasons are most likely caused by the simplifications done for the simulation circuit, i.e. the incomplete consideration of all parasitic elements in the real circuit.

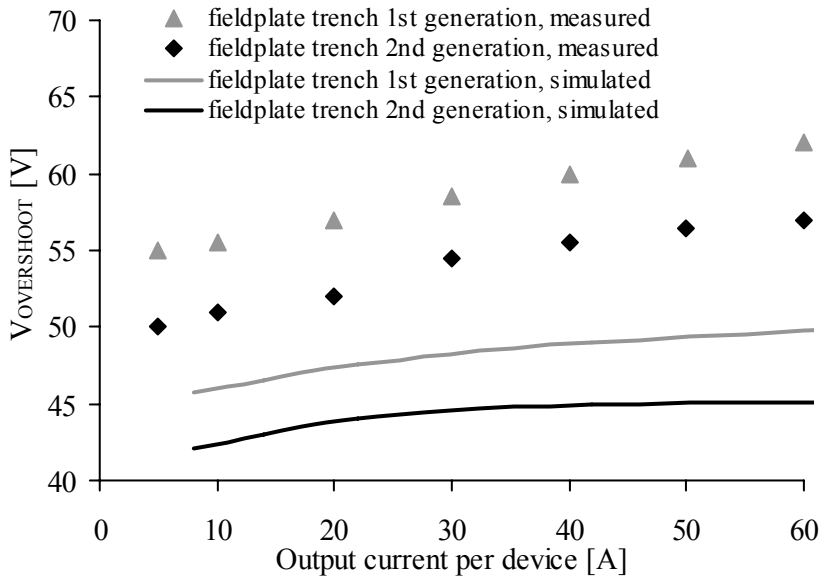

Fig. 11: Comparison of the simulated and measured voltage overshoot of the MOSFET in a SR stage

Measured device performance

In the measurement shown in Fig. 12 the efficiency is compared to the predecessor device and a clear performance improvement was gained over the whole power range. The high-load efficiency is improved by 0.3 %, while at the same time the low-load efficiency is 0.2 % better. This result was achieved by the previously discussed improvement of the FOM_G. Not only the $R_{DS(ON)}$ but also the switching charges like Q_G and Q_{OSS} are much lower than in the first generation device. Considering an efficiency level between 98 % and 99 % of the synchronous rectification stage, an improvement of 0.3 % clearly helps the designers of SMPS to reach their performance targets.

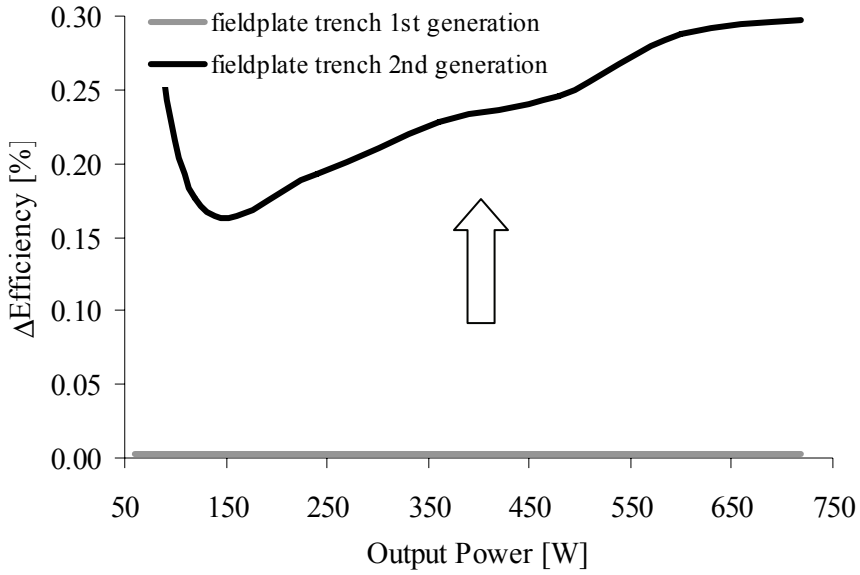

Fig. 12: Measured device efficiency in synchronous rectification

As indicated before, voltage overshoots at turn-off of the SR MOSFET are a big challenge, especially for hard switched topologies. Designers need to ensure that the level of this peak does not exceed the maximum rating of the device. This often requires the use of a snubber network which is costly and furthermore typically decreases the performance of the SMPS [8]. The snubber in its easiest version

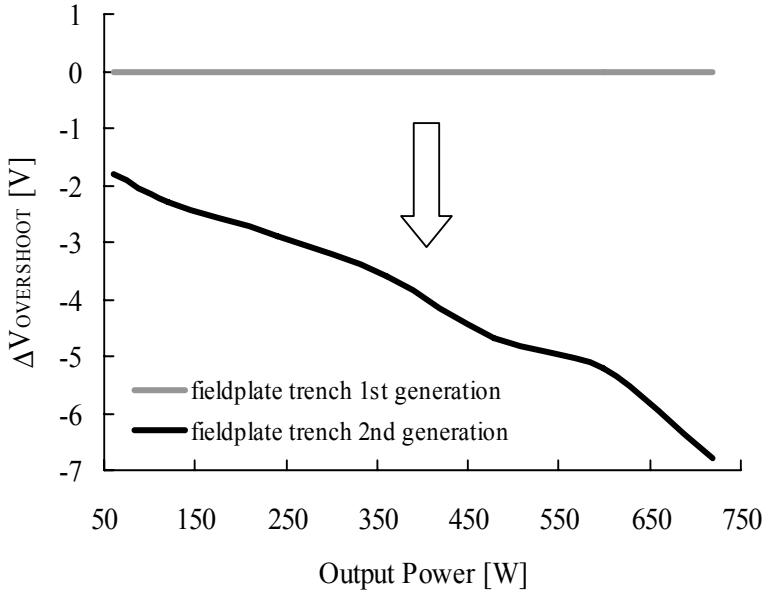

Fig. 13: Measured voltage overshoot in synchronous rectifier

consists of a series-connected resistor and capacitor, connected in parallel to the drain and source of the MOSFET as shown in Fig. 10, and is a significant source of power losses. Any reduction of the capacitance value improves the efficiency of the circuit.
The measurements of the spiking behavior in the PSU showed the clear improvement of the new MOSFET generation compared to its predecessor technology over the full output power range. This comparison is shown in Fig. 13. A peak voltage reduction of up to 7 V at high output power is achieved. This on the one hand reduces the stress for the MOSFET itself leading to improved reliability, and on the other hand reduces the efforts involved in designing the snubber network.

Conclusion

This paper presents a new generation of MOSFETs designed to be used for synchronous rectification. To improve the overall efficiency it is clearly not enough to go for products with low $R_{DS(ON)}$. As the new efficiency targets also require high levels of low load performance, the switching losses need to be minimized at the same time. To fulfill these needs, the FOM has to be dramatically decreased. By using improved manufacturing set-ups this step is now possible, as proven by the first application measurements. The efficiency level can be raised by up to 0.3 % while at the same time the turn-off voltage overshoot is reduced by up to 7 V. These improvements allow an easy design-in process with less effort for the designers of SMPS.

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