A New Simulation Approach to Investigate Avalanche Behavior

I. Pawel, R. Siemieniec
Infineon Technologies Austria AG
Siemensstr. 2, A-9500 Villach, Austria
ilja.pawel@infineon.com
ralf.siemieniec@infineon.com

***Abstract*— Experiments revealed a dependence of sustained avalanche current on epitaxial layer structure, ambient temperature and chip size. With higher on-resistance, the avalanche current normally increases as well. A new mixed-mode simulation model proposed before explained the dependencies of avalanche current on device structure due to inherent instabilities. In this work, the simulation model was extended to explain found dependencies of avalanche current on chip size and therefore the chip layout and chosen external gate resistance.**

I. Introduction

There is an ongoing demand for low-voltage power MOSFET with low on-state resistance and good switching behavior. These devices are used for example in DC-DC power supplies, AC-DC adapters, Class-D amplifiers and motor drives. In all these applications, atypical switching conditions can occur, particularly during high voltage peaks, driving devices into the avalanche mode due to the presence of a small parasitic inductance.

Previous work was done to predict, by means of numerical simulations, the maximum avalanche current I_{as} that the transistor is able to sustain. It was possible to realistically simulate the strong dependence of avalanche current on process variations, especially for small values of the parasitic inductance [1].

Under such conditions the devices were usually destroyed at current values lower than the expected limit for the case of thermal destruction. Here, the device finally fails because the dissipated energy due to the large but homogenous current flow leads to a temperature at which the carrier concentration becomes too large and the device behaves intrinsic. In difference, avalanche events triggered by a small inductance often result in earlier destruction of the device due to the formation of current filaments, which is known as non-thermal destruction [2].

The developed model could be used to explain the avalanche behavior in dependence on process variations and therefore of the device structure. Of course, there are other effects taking influence on the avalanche ruggedness of a device. One is the often found dependence of the normalized avalanche current ($I_{as}/I_{nominal}$) a device is able to sustain on the chip size and external gate resistance. Thus, a larger chip shows a reduced avalanche current at lower gate resistance value compared to a smaller chip although the device structure is identical. If the external gate resistance value is higher, both devices are able to sustain a multiple of their respective nominal current.

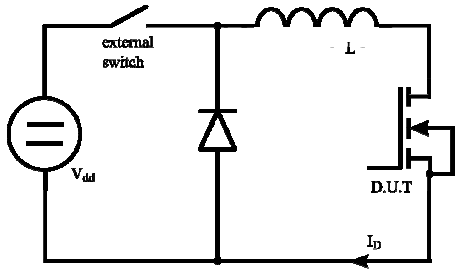


Fig. 1: Circuit to determine the UIS behavior of a MOSFET

Smaller values of the resistor correspond with smaller avalanche currents. In this work the model is extended to account for such effects. It can be used to predict the influence of switching behavior on avalanche ruggedness due to effects of inhomogeneous switching on the chip which commonly occur immediately after or even during the switching process with the transistor not yet fully switched off.

II. Experimental Findings

To determine the maximum avalanche current the device is able to sustain under defined conditions, the UIS (Unclamped Inductive Switching) test is used. Fig. 1 shows the basic circuit as used for these measurements.

Typical current and voltage waveforms of an avalanche measurement are shown in Fig. 2. The current ramps up in proportion to the inductance in the circuit and the applied voltage. After turning off the device, the energy stored in the inductance must be dissipated in the transistor.

Since the current continues to flow through the inductance and cannot change instantaneously, the transistor is forced to maintain the current. Thus the voltage over the device increases until the stationary breakdown voltage is exceeded and the device enters the avalanche mode. In case of thermal destruction, the device fails before the current flow has ceased. In difference to that, non-thermal destruction occurs earlier during an avalanche event as shown in Fig. 3. In this example, the device is destroyed almost immediately and the voltage waveform just shows a peak. Non-thermal destruction is often

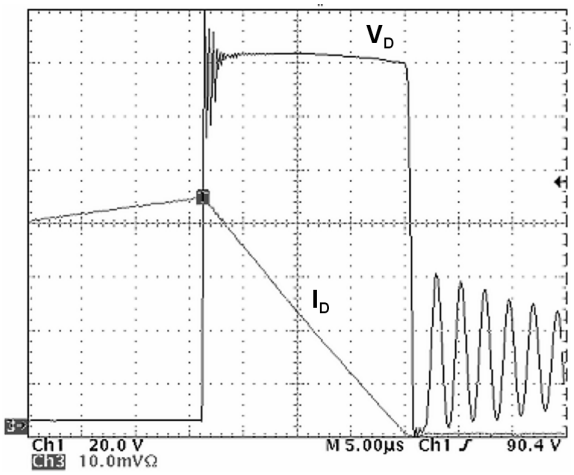


Fig. 2: Current and voltage waveform for a typical avalanche event

found in case of small values of the inductance L, which corresponds to large rates in current change di/dt as well as in relatively large current values itself.

Fig. 4 illustrates the dependence of avalanche current on chip area and value of the external gate resistor. While the small chip shows only a slight dependence on the value of gate resistor, the large chip degrades significantly.

To better understand the nature of these effects the chip layout must be taken into consideration. Fig. 5 shows the most important items of a typical chip layout.

We assume the cells are arranged in stripes (dark grey in the figure). Each stripe represents a trench in which a gate contact is included. In our example the gate stripes are filled with highly doped silicon and are contacted to a metal runner at the trench ends. These metal runners are connected to the gate pad which represents the interface to the external circuitry. Considering this layout one can assume that not all parts of the chip experience the same internal gate resistance. In our example, the region (2) sees a gate resistance R_{G2} consisting of the poly silicon R_{Poly2}, the metal runner R_{Metal2}

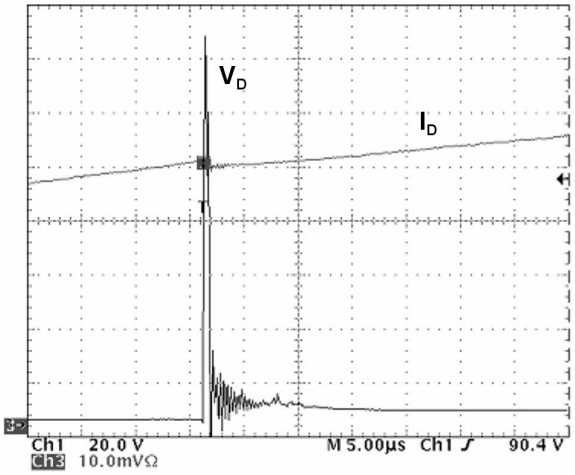


Fig. 3: Example for non-thermal destruction during avalanche mode

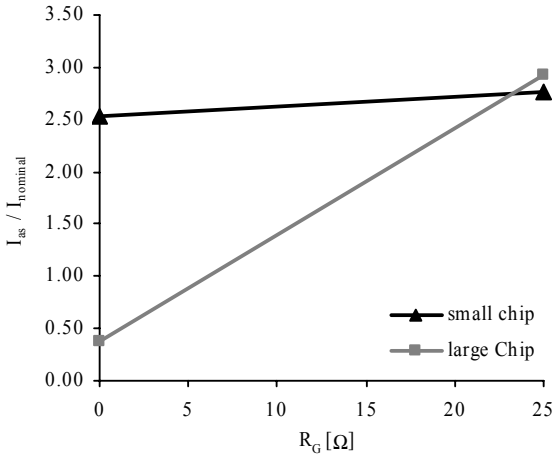


Fig. 4: Avalanche current in dependence of chip size and value of external gate resistor for small value of load inductance.

and the metal runner R_{Metal1}. Region (1), on the other hand, has a reduced gate resistance consisting only of R_{Metal1}. In case of a switching event, Region (1) may respond faster compared to Region (2).

III. Simulation Model

A. Generalized Approach

Three general approaches in 2D simulations can be distinguished. For some effects, single cell simulations proved to be sufficient [1],[3]- [6]. It is also possible to model effects of filaments by means of multi-cell approaches, that is incorporating cell entities into one structure [7]. Additionally, simulation models using the mixed-mode simulation approach have been reported, e.g. [8]-[10]. They typically use two or more cells varying in size with one cell exhibiting a weakness in structure or other design parameters, e.g. higher body resistance or different geometry.

Based on the model presented in [1] and [11], we propose a new generalized model shown in Fig. 6. It consists of N basic

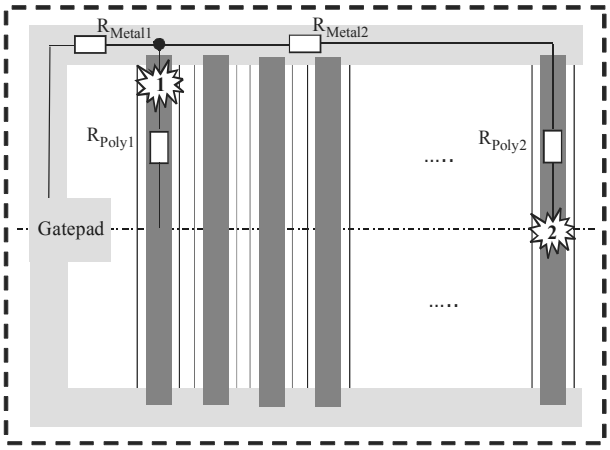


Fig. 5: Simplified model of chip layout

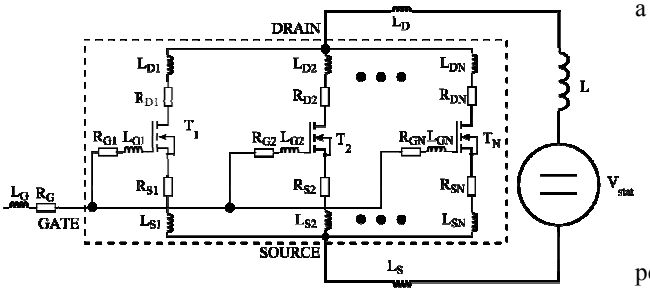


Fig. 6: Generalized simulation approach along with external circuitry

cells that may or may not be identical and various external and internal elements. A dashed rectangle symbolically separates the external circuitry from internal elements. External elements are related to the external circuitry including parasitic elements of the testing environment. Internal elements are introduced to model different effects related to the behavior of different parts on the chip as described before.

The internal resistive elements must be scaled according to the size of the cells to get similar results. We define the area ratio vector $\vec{Y} = (y_1 \quad y_2 \quad \cdots \quad y_N)$:

$$\vec{A} = \vec{Y} \cdot A_{chip}, \tag{1}$$

with

$$\vec{Y} \bullet \vec{1}^T = \sum_{i=1}^{N} y_i = 1, \tag{2}$$

meaning the sum of all cells is identical to the chip size. Then we can define the internal elements of cell i:

$$\vec{R}_i = \frac{1}{A_i} \cdot (R_{Di} \quad R_{Si} \quad R_{Gi}) \tag{3}$$

$$\vec{L}_i = \frac{1}{A_i} \cdot (L_{Di} \quad L_{Si} \quad L_{Gi}) \tag{4}$$

Another feature is the current inhomogeneity vector $\vec{X} = (x_1 \quad x_2 \quad \cdots \quad x_N)$:

$$\vec{J} = \vec{X} \cdot J_{total}, \tag{5}$$

with

$$\frac{1}{N} \cdot \vec{X} \bullet \vec{1}^T = \frac{1}{N} \sum_{i=1}^{N} x_i = 1 \tag{6}$$

It can be treated as a disturb signal imposed on the system. If instabilities exist they should become apparent in the cells with a (slightly) higher current density.

If all internal resistances and inductances are electrically equal:

$$R_{Xi} = R_{Xj} \quad \forall X, i, j \tag{7}$$

$$L_{Xi} = L_{Xj} \quad \forall X, i, j \tag{8}$$

then all cells show identical switching behavior. If this is not the case then asymmetries in the switching behavior are apparent.

Differences in the time response of the different cells can also lead to current inhomogeneities in this model. We assume a generalized dependency for the current density in cell i:

$$J_i = \frac{1}{A_i} K_i \cdot f_i (V_{DS_i}, V_{GS_i}), \tag{9}$$

with

$$K_i = \mu_n C_{ox} \frac{w_{ch,i}}{l_{ch,i}} \tag{10}$$

Here, μ_n is the electron mobility, C_{ox} the oxide capacity per device area, $w_{ch,i}$ the channel width and $l_{ch,i}$ the channel length of device i. (Note that $l_{ch,i}$ is also a function of V_{DSi}.)

Then the normalized current density of the m^{th} cell calculates to:

$$\frac{J_m}{J_{total}} = \frac{1}{y_m} \cdot \frac{K_m \cdot f_m}{\sum_{i=1}^{N} K_i \cdot f_i}. \tag{11}$$

In every cell the maximum temperature T_{max} is extracted separately. Destruction is defined, if any T_{max} exceeds a defined critical temperature T_{crit} as discussed e.g. in [12]. In our analysis we considered a system of N = 2 cells according to Fig. 7 simplifying the generalized simulation model in Fig. 6 to focus solely on the influence of internal gate resistances.

The model elements defined in Eq. (1) to Eq. (6) are set to:

$$\vec{L}_i = \vec{0} \tag{12}$$

$$\vec{Y} = (1 - y_2 \quad y_2) \tag{13}$$

$$\vec{X} = (2 - x_2 \quad x_2) \tag{14}$$

$$\vec{R}_1 = \frac{1}{A_1} \left(\frac{\Delta V_{DS}}{(1 - y_2)(2 - x_2) J_{total} A_{chip}} \quad 0 \quad 0 \right) \tag{15}$$

$$\vec{R}_2 = \frac{1}{A_2} (0 \quad 0 \quad 0) \tag{16}$$

This model proved to be sufficient to clarify various effects. Device simulations were performed using the device simulation software package MEDICI [13].

B. Model Verification

Firstly, the influence of area ratio parameter $\vec{Y}$ and the current inhomogeneity factor $\vec{X}$ apart from internal resistance value variations will be shown.

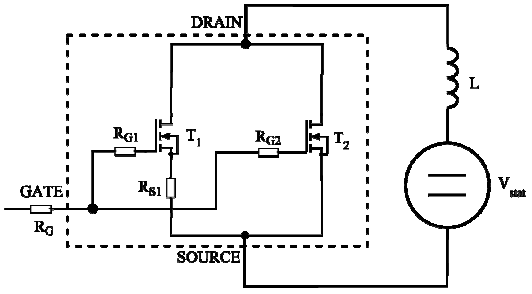
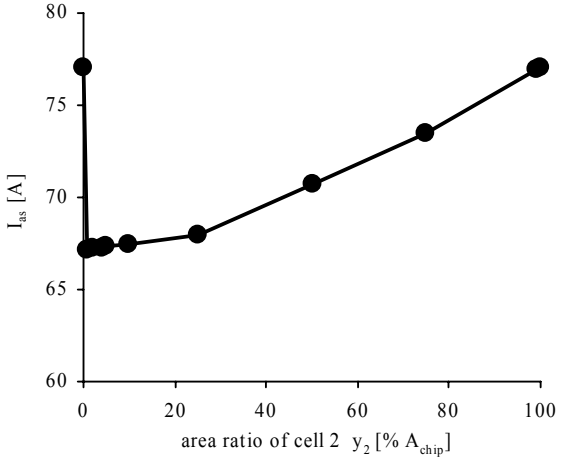
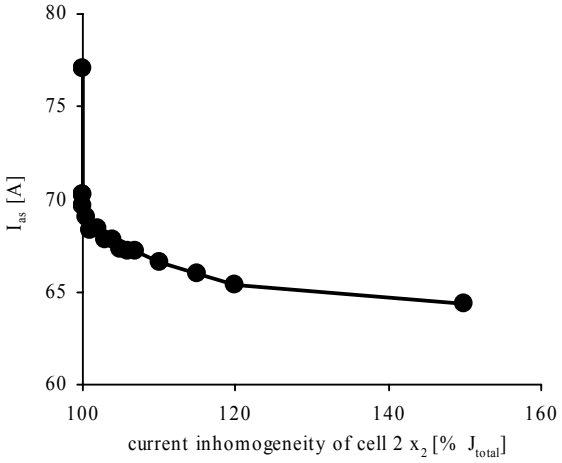


Fig. 7: Simplified simulation model

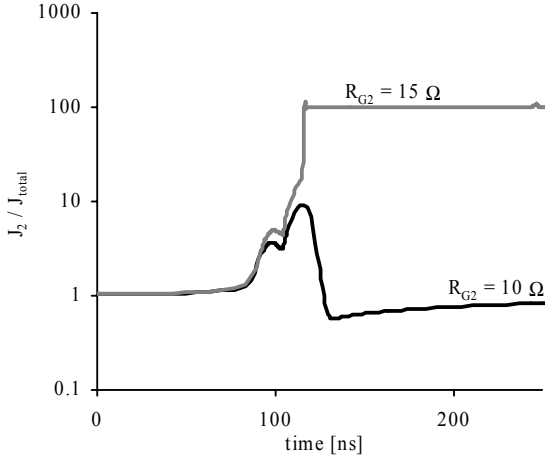


a)

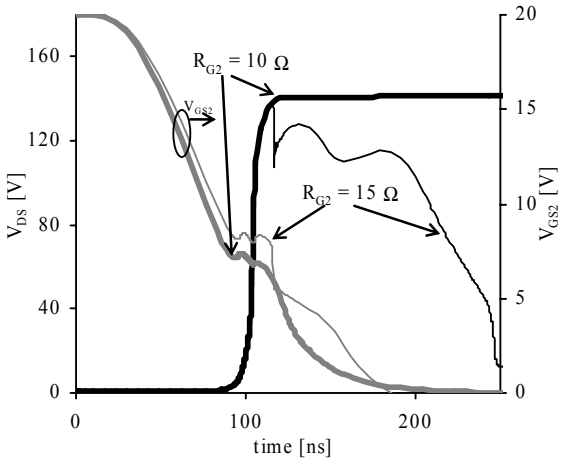


b)

Fig. 8: Influence on simulated I_{as}
a) of area ratio of cell 2 with $x_2 = 105\%$
b) of current inhomogeneity factor for cell 2 with $y_2 = 1\%$



a)



b)

Fig. 9: Simulated current density ratio J_2/J_{total} in cell 2 a) and drain source voltage V_{DS} (b) for two different values of R_{G2}.

with ΔV_{DS} representing the drain source voltage difference between cell 1 and 2 due to either current inhomogeneity or different on-state resistances.

The dependence on the area ratio vector $\vec{Y}$ is shown in Fig. 8(a). If y_2 approaches 1 (or zero) the obtained avalanche current I_{as} is identical with the result obtained by means of single cell simulation. As expected, the current values obtained for $y_2 = 0\%$ and $y_2 = 100\%$ are identical, representing the result of a single cell simulation. The influence is obviously strongest if the "weaker" cell has the lowest possible area since current concentration is highest. For that reason, we chose an area ratio vector $\vec{Y} = (0.99 \quad 0.01)$, supposing the "weaker" cell 2 to be small.

Secondly, a reasonable current inhomogeneity vector $\vec{X}$ needed to be identified. For our purposes, an inhomogeneity factor of $\vec{X} = (0.95 \quad 1.05)$ was acceptable. This value was chosen somewhat arbitrarily to see an influence according to Fig. 8b). A deviation of current in a small part of device of 5% seemed to be realistic and no qualitatively different behavior could be achieved with other values of current inhomogeneity factor $\vec{X}$.

IV. Simulation Results

We are now able to relate the internal gate resistances to the actual resistance values on the chip. Regarding Fig. 5 we can set R_{G1} and R_{G2} as follows:

$$R_{G1} = R_{Metal_1} \tag{17}$$

$$R_{G2} = R_{Metal_1} + R_{Metal_2} + R_{Poly_2} \tag{18}$$

All simulations are done with the parameters $\vec{X}$ and $\vec{Y}$ discussed in the previous section:

$$\vec{X} = (0.95 \quad 1.05) \tag{19}$$

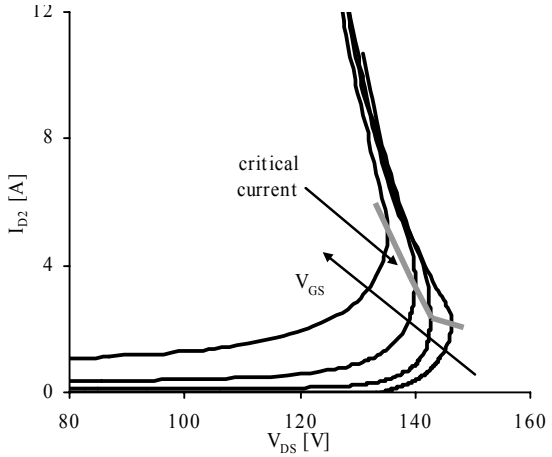


Fig. 10: Isothermal simulation (300 K) of drain current over drain voltage at varying gate voltages to extract the critical current. Grey line indicates the extracted critical current by connecting the snap back currents.

$$\vec{Y} = \begin{pmatrix} 0.99 & 0.01 \end{pmatrix} \tag{20}$$

Therefore, cell 2 is the smaller and "weaker" cell and should experience any existing instabilities.

To begin with, the effect of asymmetric switching will be presented. As already stated, different gate source voltages V_{GS} lead to different current densities on the chip. Fig. 9 depicts simulation results obtained for different internal gate resistances R_{G2} for a small constant value of R_{G1} = 1 mΩ.

Apparently, the switching asymmetry between the two cells increases as the internal gate resistance increases. If the current density exceeds a certain value as shown in Fig. 9(a) the device enters a critical region indicated by a sudden drop in drain source voltage shown in Fig. 9(b). A high value of current density ratio leads to destruction at lower total device currents since a small part of the device must sustain a very high current density and thus a very high temperature.

It is well known that devices with Negative Differential Conductivity (NDC) in their IV characteristics are prone to instabilities, e.g. oscillations or filaments [14]. This leads to a

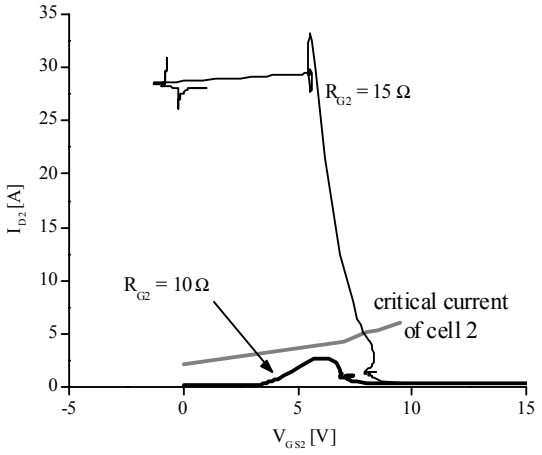


Fig. 11: Critical and actual current for different R_{G2} over gate source voltage. If actual current exceeds critical current a stable current filament develops.

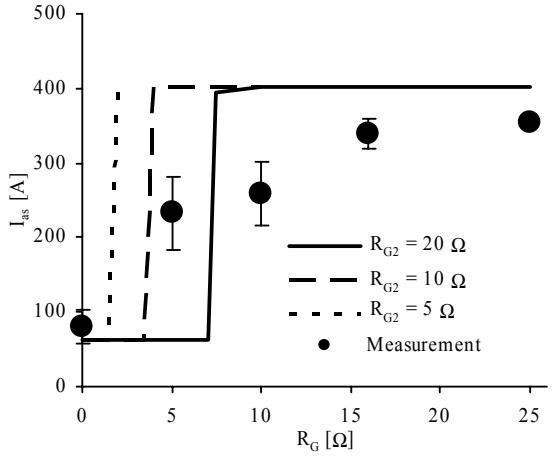


Fig. 12: Comparison of measurement and simulation of avalanche currents for a large chip. A larger (external) gate resistance leads to an improvement of avalanche behavior (L = 10 µH). R_{G1} was set to 1 mΩ

possible explanation of this effect: An applied gate voltage alters the blocking characteristics and hence the critical snap back current. For gate voltages far above the threshold voltage the channel is in strong inversion. This leads to additional impact ionization multiplication of saturation current in the space charge region [15]. The isothermal breakdown behavior can be determined if the blocking characteristics for different gate voltages are considered. In Fig. 10 the drain current I_{D2} of the small cell over drain source voltage V_{DS} is shown for various gate source voltages V_{GS2}. It can be seen that a certain drain current exists at which the drain source voltage starts to decrease for higher currents.

This current is defined as critical current since the drain source voltage reaches a maximum for this current and decreases for higher currents. This can be regarded as negative differential resistance leading to inherent instabilities. For a given device, it depends on gate source voltage and temperature. The grey line in Fig. 10 is the connection of the critical currents for different V_{GS} for a constant temperature of 300 K. This extracted critical current can be applied to determine the stability regime during transients. Considering again the switching transient in Fig. 9 we can depict the transient drain current over applied gate voltage thus eliminating the time dependency. This method is shown in Fig. 11. In the same graph, the critical current extracted as described above is shown. Thus, Fig. 11 provides a linkage between transient and quasi stationary simulations.

If the gate resistance of the small cell 2 is set to R_{G2} = 10 Ω, the current in cell 2 lies below the critical current, thus no destructive state can develop and the device safely turns off. If, on the other hand, R_{G2} is raised to a value of R_{G2} = 15 Ω, then the current I_2 in cell 2 continues to rise until all current flows through this cell thus leading to possible destructive temperatures.

This analysis was done for several chip currents and model settings. The results for a large chip, the potentially critical case, are shown in Fig. 12. Here, the external gate resistance

R_G was varied both in simulation and measurement. Measurements showed a strong degradation of avalanche current I_{as}. Simulations revealed the dependency of this degradation on internal gate resistance values.

Furthermore, a higher external gate resistance could remedy this effect. This in turn leads to slower switching behavior. Naturally, the effect was much stronger in simulation owing to the simplicity of the model. In experiment, no sudden drop in avalanche current I_{as} occurred for lower gate resistance values. The model nevertheless revealed the nature of this degradation.

V. Conclusion

Experimental results revealed a dependency of avalanche current on chip size and on external gate resistance.

A new model for the simulation of avalanche behavior was developed taking into account the influence of asymmetric switching on avalanche current. It was shown that this effect could lead to current concentration in small regions of the chip thus leading to destructively high temperatures even at current levels far below the thermal destruction limit.

This effect of asymmetric switching is especially apparent at high currents occurring at low load inductance values. It represents another destruction mechanism in the non-thermal regime compared to the well-known triggering of the parasitic bipolar transistor. A potential means to prevent the onset of destructive current concentration could be the enlargement of external gate resistance. In continuation we will study the influence of temperature and self-heating on this behavior. This also includes the consideration of other parasitic elements.

Acknowledgment

We thank D. Schleißer and A. Kaßmannhuber for the careful characterization of the devices.

References

[1] I. Pawel, R. Siemieniec, M. Rösch, F. Hirler, C. Geissler, A. Pugatschow and L.J. Balk "Design of Avalanche Capability of Power MOSFETs by Device Simulation", in *Proc. EPE 2007,* 2007

[2] R. Siemieniec, F. Hirler, A. Schlögl, M. Rösch, N. Soufi-Amlashi, J. Ropohl and U. Hiller "A new fast and rugged 100 V power MOSFET", in *Proc. EPE-PEMC 2006*, 2006

[3] K. Fischer and K. Shenai "Electrothermal Effects During Unclamped Inductive Switching (UIS) of Power MOSFETs" IEEE Transactions on Electron Devices, 1997, 44, 874-878,

[4] A.I. Deckelmann, G.K. Wachutka, F. Hirler, J. Krumrey and R. Henninger "Avalanche Breakdown Capability of Power DMOS Transistors and the Wunsch-Bell Relation" Microelectronics Reliability, 2003, 43, 1895-1900

[5] A. Vrbicky, D. Donoval, J. Marek, A. Chvala and P. Beno "Analysis of Electro-Thermal Behaviour of DMOS Transistor Structure during UIS Test" Proc. ISPS, 2006

[6] K. Chinnaswamy, P. Khandelwal, M. Trivedi and K. Shenai "Unclamped Inductive Switching Dynamics in Lateral and Vertical Power DMOSFETs" Proc. IAS, 1999

[7] V. Vaschenko, Y. Martynov and V. Sinkevitch "Simulation of Avalanche Injection Filamentation in MOSFETs and IGBTs" in Proc. ESSDERC, 1997

[8] P. Rossel, H. Tranduc, D. Montcoqut, G. Charitat and I. Pagès "Avalanche Characteristics of MOS Transistors" in Proc. MIEL, 1997

[9] A.I. Deckelmann, G.K. Wachutka, F. Hirler, J. Krumrey and R. Henninger "Failure of Multiple-Cell Power DMOS Transistors in Avalanche Operation" in Proc. ESSDERC, 2003

[10] G. Hurkx and N. Koper "A Physics-Based Model for the Avalanche Ruggedness of Power Diodes" in Proc. ISPSD, 1999

[11] K. Kawamoto, S. Takahashi, S. Fujino and I. Shirakawa "A No-Snapback LDMOSFET With Automotive ESD Endurance" IEEE Transactions on Electron Devices, 2002, 49, 2047-2053

[12] I. Pawel, R. Siemieniec, M. Rösch, F. Hirler and R. Herzer "Experimental Study and Simulations on Two Different Avalanche Modes in Trench Power MOSFETs", IET Circuits, Devices & Systems, in press

[13] Synopsys, Inc,. MEDICI™ User Guide, 2006

[14] M.P. Shaw, V. Mitin, E. Schöll and H. Grubin "The Physics of Instabilities in Solid State Electron Devices" New York, Plenum Press, 1992

[15] M. Denison "Single Stress Safe Operating Area of DMOS Transistors integrated in Smart Power Technologies", PhD thesis, University of Bremen, 2004