Multi-Cell Effects during Unclamped Inductive Switching of Power MOSFETs

I. Pawel, R. Siemieniec and M. Rösch

Abstract— **In this paper, we describe the crucial dependence of avalanche behavior on epitaxial layer thickness and gate resistance during unclamped inductive switching (UIS) especially for high currents for Power MOSFET devices employing field-plate compensation in the drift region. All transient simulations were performed using Medici's Mixed-Mode simulation approach including self-heating. A higher epitaxial layer thickness eventually resulted in a higher avalanche ruggedness but also in higher on-state resistance. Thus, a trade-off exists.**

I. Introduction

There is an ongoing demand for low-voltage power MOSFET with low on-state resistance and good switching behavior. These devices are used for example in DC-DC power supplies, AC-DC adapters, Class-D amplifiers and motor drives. In all these applications, atypical switching conditions can occur, particularly during high voltage peaks, driving devices into the avalanche mode due to the presence of a small parasitic inductance. A good alternative in the desired voltage range are transistors using the concept of field-plates for compensation to realize a low on-resistance $R_{DS(on)}$ [1], as shown in Fig. 1. Positive charges in the mesa region (drift region) are compensated by negative charges on field-plates. A thick oxide layer serves as insulator between these two charges. The breakdown capability is mainly determined by the thickness of this oxide layer and partly by the length of the drift region. In [2], a detailed analysis of compensation structures is provided. Previous work was done to predict, by means of numerical simulations, the maximum avalanche current I_{as} that the transistor is able to sustain. It was possible to realistically simulate the strong dependence of avalanche current on process variations, especially for small values of the parasitic inductance [3]. Under such conditions the devices were usually destroyed at current values lower than the expected limit for the case of thermal destruction due to the formation of current filaments, which is known as non-thermal destruction [4]. The UIS behavior has been studied thoroughly e.g. in [5–7]. Also the effect of filamentation during UIS was under investigation [8, 9]. The influence of gate resistors on switching behavior of paralleled devices with additional oscillation effects have been discussed previously [10–12]. Different gate resistors lead to unbalanced gate voltage and thus to unbalanced current distribution. We propose a simulation approach and possible explanation for unstable behavior leading to premature destruction in the event of UIS related to gate resistances.

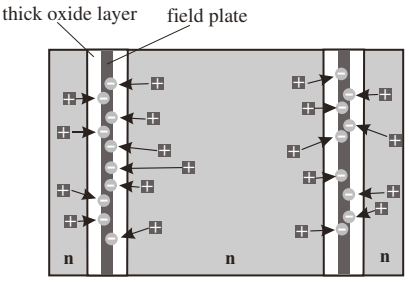

Fig. 1. Compensation of positive donor charges in the n-region by negative charges located on the field-plates

II. Experimental Results

Earlier work revealed a dependency of the maximum sustainable avalanche current on on-state resistance caused e.g. due to different epitaxial layer thickness [3]. Measurements on manufactured samples revealed the occurrence of very short time to destruction, leading to "needle-shaped" pulses in the drain voltage in the event of unclamped inductive switching. This effect seemed to aggravate for lower temperature. In order to understand this effect we considered a typical chip layout. Its most important items are shown in Fig. 2. We assume the cells are arranged in stripes (dark grey in the figure). Each stripe represents a trench in which a gate contact is included. In our example the gate stripes are filled with highly doped silicon and are contacted to a metal runner at the trench ends. These metal runners are connected to the gate pad which represents the interface to the external circuitry. Considering this layout one can assume that not all parts of the chip experience the same internal gate resistance. In our simple approach, the region (2) experiences a gate resistance R_{G2} consisting of the poly silicon R_{Poly2}, the metal runner R_{Metal2} and the metal runner R_{Metal1}. Region (1), on the other hand, has a reduced gate resistance consisting only of R_{Metal1}. In case of a switching event, Region (1) responds faster compared to Region (2). It is also worth

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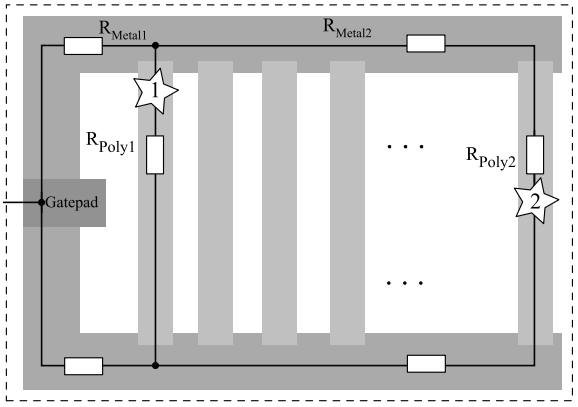

Fig. 2. Chip layout showing regions with different internal gate resistances, thus different switching speeds

noting that the main contribution to the gate resistance is from the used polysilicon.

III. Simulation

All simulations were performed incorporating the circuit shown in Fig. 3. It was first presented in [13]. It consists of two identical transistor cells as well as external and internal elements. A dashed rectangle symbolically separates the external circuitry from internal elements. The internal gate resistors are introduced to model the assumed chip layout of Fig. 2:

$$\begin{aligned} R_{G1} &= R_{Metal1} \\ R_{G2} &= R_{Metal1} + R_{Metal2} + R_{Poly2} \end{aligned} \tag{1}$$

The additional drain resistors are zero unless stated explicitly. All internal (resistive) elements must be scaled according to the size of the cells to get similar results. Furthermore, we made the "slower" cell 2 rather small compared to the total chip area. Thus we were able to simulate effects related to asymmetrical switching with this simple approach as discussed before.

IV. Results and Discussion

In all analysis we assume transistor T_2 to be "slower" as explained before. At first, we examined the influence of internal gate resistance R_{G2} on transient current density J_2 in cell 2 compared to total current density over the entire chip J_{total} for different epitaxial layer thicknesses d_{Epi}. The maximum of the current density ratio in cell 2 compared to the total current density $Max\,(J_2/J_{total})$ (concentration factor) occurs typically immediately after switching off the device with still some gate voltage applied. It was extracted from transient simulations (e.g. shown in Fig. 10). This procedure was repeated for different R_{G2} for each layer thickness and eventually resulted in curves shown in Fig. 4. A higher value of R_{G2} lead to an increase of concentration factor. If R_{G2} exceeded a certain value the current density in cell 2 rose steeply. This value depended on the thickness of the epitaxial layer d_{Epi}. High current density was considered potentially hazardous due to local self-heating effects. Small parts of the chip could reach destructively high temperatures in short range of time. With lower temperature the occurring current concentration was higher due to steeper transfer characteristic. If the current density in cell 2 exceeded a certain limit, the impact ionization generation center normally located at the trench bottom relocated to the nn^+ junction between epitaxial layer and substrate. This critical current density can easily be determined by extracting snap back currents for different gate voltages as done in [3] and shown in Fig. 5.

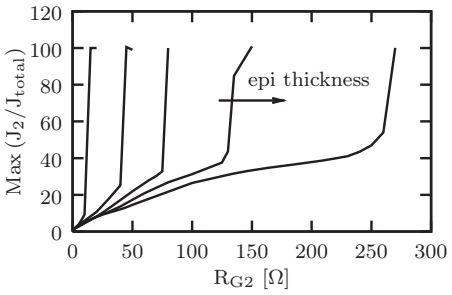

Fig. 4. Influence of internal gate resistance R_{G2} on $Max\,(J_2/J_{total})$ for different d_{Epi} including self-heating effects. $J_{total} = 15$ Amm^{-2}

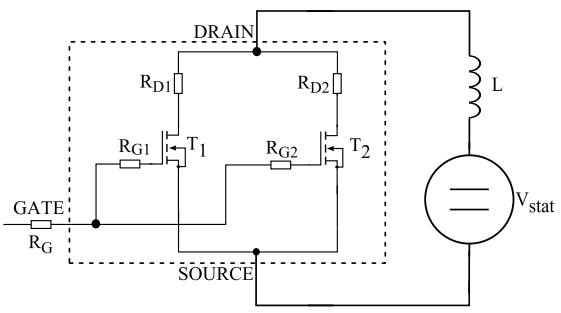

Fig. 3. Simulation model used in this paper

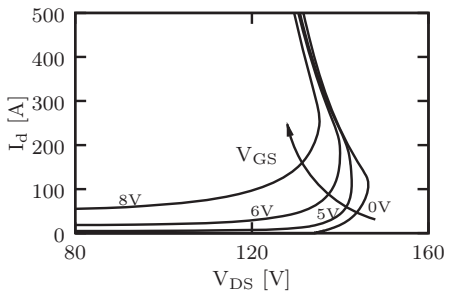

Fig. 5. drain current as function of drain voltage for various V_{GS} with $V_{th} \sim 3V$

TABLE I

INFLUENCE OF ADDITIONAL LAYER RESISTANCE ON CONCENTRATION FACTOR $Max\,(J_2/J_{total})$ WITH $R_{G2} = 15\ \Omega$ AND $J_{total} = 15\ \mathrm{Amm}^{-2}$

structure	d_{Epi1}	d_{Epi1} & ΔR_{Epi}	d_{Epi2}
$Max\,(J_2/J_{total})$	100	11.77	6.45

A higher V_{GS} leads to a higher snap back current.
A possible explanation for the influence of layer thickness is as follows. An additional epitaxial layer imposes a higher resistance due to increased layer thickness. This in turn could lead to a decreasing concentration factor. To verify this, we simulated two structures with a thin epitaxial layer d_{Epi1} and a thicker layer d_{Epi2}, respectively. Furthermore, we artificially modelled a higher layer thickness by setting the internal bulk drain resistance values R_{D1} and R_{D2} for simulation of the structure incorporating d_{Epi1} accordingly:

$$R_{D1} = R_{D2} = \Delta R_{Epi} = \frac{\varrho_{Epi} \cdot (d_{Epi1} - d_{Epi2})}{A}, \quad (2)$$

with ϱ_{Epi} the specific resistance of the epitaxial layer. Indeed, we found an influence on concentration factor with this simple approach. Table I summarizes the outcome of this experiment. A higher resistance value led to a lower concentration factor. Nevertheless, the effect was more pronounced for the process-simulated increase of layer thickness compared to the modelled increase due to additional bulk resistors. The additional drain resistance also led (mathematically) to a lower effective mobility [14]. To foster this assumption, we also varied the effective mobility in simulation and could indeed find a similar influence. With lower mobility, thus resulting in a higher resistance, the concentration factor decreased. The effect of current concentration showed only little dependency on doping concentration N_D below the onset of high current concentration. The critical resistance value was higher for higher N_D as depicted in Fig. 6. This could be explained by space-charge modulation due to current density J flowing through the space-charge region. With q, the electronic charge, and v_n, the saturation velocity of electrons, the effective net charge calculated to $\rho_{eff} \approx N_D - J/(q \cdot v_n)$. The steep rise of current density in cell 2 set in when the space-charge became neutral $\rho_{eff} \sim 0$. To better understand the nature of this effect, we also performed simulations without self-heating. A comparison using the same structure can be seen in Fig. 7. Both simulations showed qualitatively the same behavior. However, the effect was more pronounced, i.e. set in at a lower value of the internal gate resistor R_{G2}, if the self-heating was turned off. This was again an indication for the dependency on mobility. Mobility reduction led to a higher resistance and thus to a lower concentration factor.
The effect of applied total current density is shown in Fig. 8 - 9. For both current densities, the current density J_2 in cell 2 rises strongly. In case of a smaller total current density, J_2 drops to the overall current density of the chip after short time, see Fig. 8. For a larger total current density, as depicted in Fig. 9, cell 2 remains at high current density.
The influence of an external gate resistance R_G is shown in Fig. 9 and Fig. 10. With larger R_G the occurring current concentration factor is dramatically reduced thus leading to a safe switching behavior.

Under some circumstances oscillations developed. The nature of oscillations depended on the internal and external resistors and inductors. One possible cause could be found in the improper choice of differential gate resistors R_{Gi} [10]. Furthermore, if the external gate resistance R_G was increased the behavior was supposed to be more unstable [12]. In our example, however, an increasing R_G let the oscillations disappear, see Fig. 9 and Fig. 10, respectively. The frequency of oscillation didn't depend on the value of load inductance. We also varied the slope of the gate drive voltage dV_G/dt. A faster turn-off aggravated the tendency of oscillations.
A negative differential gate capacitance could also lead to oscillations [12]. Indeed, we could find a negative dif-

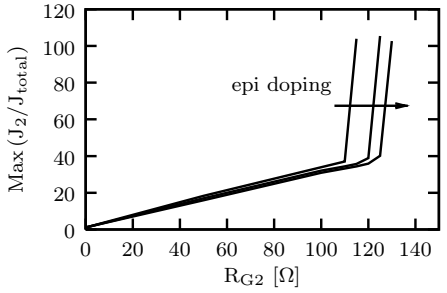

Fig. 6. Influence of internal gate resistance R_{G2} on $Max\,(J_2/J_{total})$ for different N_D including self-heating effects. $J_{total} = 15\ \mathrm{Amm}^{-2}$

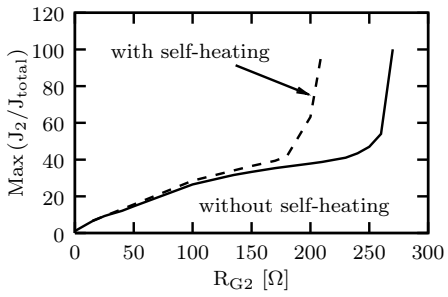

Fig. 7. Simulation of the effect of current concentration with and without self-heating for thick d_{Epi}. $J_{total} = 15\ \mathrm{Amm}^{-2}$

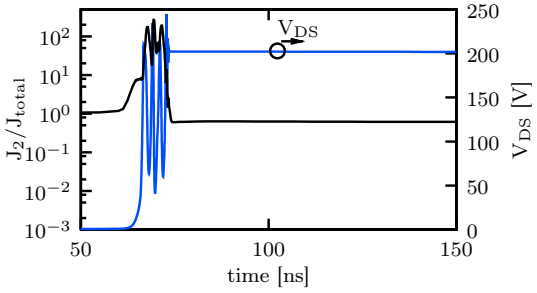

Fig. 8. Current density ratio of cell 2 and drain voltage for $R_{G2} = 4\ \Omega, R_G = 1\ \Omega$ and $I_{as} = 10$ A. High current concentration persisted only for short time.

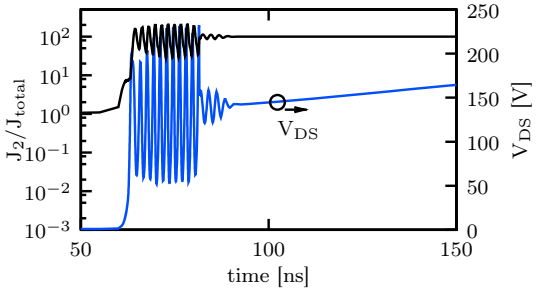

Fig. 9. Current density ratio of cell 2 and drain voltage for $R_{G2} = 4\ \Omega, R_G = 1\ \Omega$ and $I_{as} = 12$ A. High current concentration remained during switching.

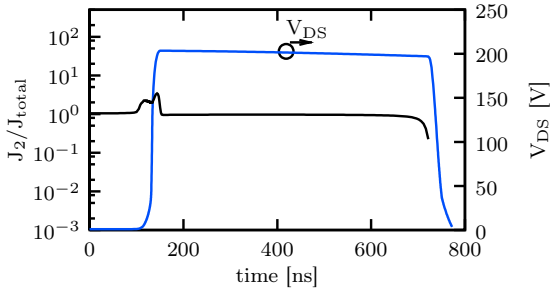

Fig. 10. Current density ratio of cell 2 and drain voltage for $R_{G2} = 4\ \Omega, R_G = 25\ \Omega$ and $I_{as} = 12$ A. No significant current concentration and no oscillations due to higher external gate resistance occurred

ferential gate capacitance for high drain voltages which is shown in Fig. 11.

V. Conclusion

We showed the influence of epitaxial layer thickness d_{Epi} on avalanche ruggedness for MOSFETs employing the field-plate compensation principle. Asymmetric switching of different parts on the chip due to different gate resistances, approximated with two cells, can lead to instable behavior during UIS, especially immediately after the switching. Our analysis showed that additional d_{Epi} increases the available margin for current concentration before instability sets in. This is due to

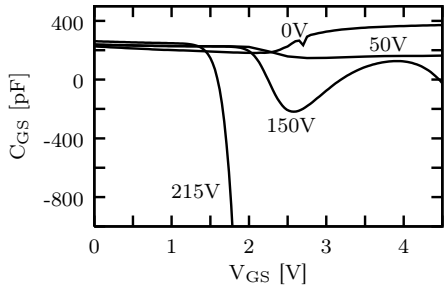

Fig. 11. Gate-Source capacitance as function of gate voltage for different drain voltages

the increased drain resistance. Thus, a trade-off exists between on-state resistance and avalanche ruggedness. Other dynamic parameters should also play a role in dimensioning the device, e.g. the reverse-recovery charge Q_{rr} which is important for some applications. Further work will be done to incorporate more distributed cells to gain further insight into device behavior.

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