A novel 650 V SiC Technology for high efficiency Totem Pole PFC topologies

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Abstract

This work introduces a new 650 V SiC Trench MOSFET technology tailored to address the needs of power supplies in the power range from several hundred watts to some tens of kilowatts including server and telecom switch-mode power supplies (SMPS), solar inverters, electric-vehicle chargers and UPS. The 650 V MOSFETs enable new, highly efficient topologies such as the full-bridge Totem Pole in the power-factor correction (PFC) stage with a peak efficiency of 99 %. The technology fulfills industrial application reliability requirements covering cosmic-ray ruggedness and gate oxide reliability.

1 Introduction

Power supplies consist of four main building blocks: the AC-DC conversion in the Power Factor Correction (PFC) stage, the primary side stage, the secondary side stage and the overall control block. Nowadays, soft-switching techniques as typically employed in LLC resonant topologies enable a significant improvement of the efficiency on the primary side [1,2]. The replacement of the traditionally used diode rectifiers by power MOSFETs acting as synchronous rectifiers (SR) dramatically reduces the rectification losses and enabled a further increase of the converter efficiency and the power density [3]. In this way the DC-DC conversion efficiency has been significantly improved, moving attention again to the AC-DC conversion of the PFC stage.

Power factor correction is one of the most important parts of an SMPS especially for the power range of 100 W and higher. In the past years, the worldwide power consumption has increased dramatically with power supplies for server and telecom applications being a substantial contributor to this increase. SMPS of highest efficiency are easily achievable by the use of wide bandgap power semiconductors in combination with different topologies than presently used. However, present PFC designs limit the achievable system efficiency to 98 %. Here, the traditional input bridge rectifier represents the biggest loss contributor (see Fig. 1). Alternative topologies solve this issue by using wide bandgap power semiconductors.

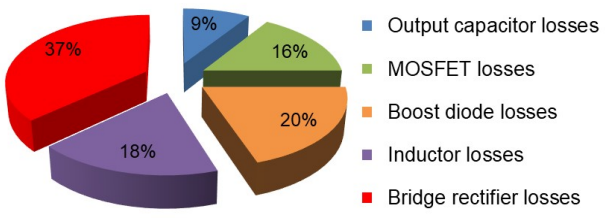

Fig. 1: Loss breakdown for a traditional Boost PFC

2 Application requirements

The power supplies discussed in this work are usually designed for a universal input voltage range of 85 – 265 VAC. The AC-DC part typically consists of an input bridge rectifier combined with a Boost PFC stage with an output voltage of typically 400 V. Fig. 2 depicts a typical schematic. As the input voltage covers a range of larger than 3:1, the RMS input current varies accordingly. Consequently, the I^2R conduction losses vary over a 10:1 range for just a single load condition, imposing a serious challenge for the optimization and selection of both the MOSFET P1 and the Schottky rectifier D1. The typical operating frequency is limited to 70 kHz to keep the fundamental and 2nd harmonic below 150 kHz due to EMI reasons. A higher operating frequency also clearly increases the switching

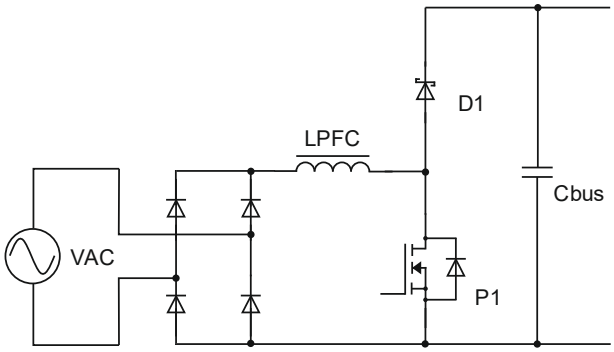

Fig. 2: Schematic of a typical Boost PFC stage

losses. The typical control mode is the Continuous Conduction Mode (CCM) as here the ripple current losses and switching losses are well balanced. The PFC stage may also be operated in Discontinuous Conduction Mode (DCM) or Critical Conduction Mode (CrCM) at the cost of a much higher ripple current while at the same time enabling quasi Zero Voltage Switching (ZVS) for reduced switching losses. However, the input bridge rectifier is in all cases the most dominant source of losses, causing an efficiency loss between 1 % and 2 %. Obviously, even a perfect zero loss MOSFET P1 would not be able to compensate for these losses as also clearly visible from the loss breakdown shown in Fig. 1. For a further increase in the absolute efficiency of the complete power supply it is therefore necessary to move to other topologies. One option is the Dual Boost PFC [4] as shown in Fig. 3. One can expect efficiencies of up to 98.8 % from this topology.

The full-bridge Totem Pole topology as shown in Fig. 4 works bridgeless and eliminates any diode-

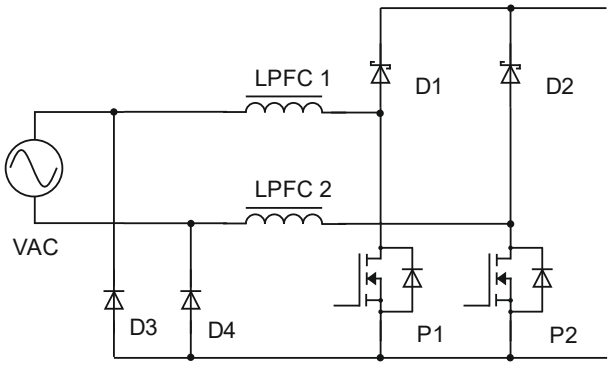

Fig. 3: Schematic of a Dual Boost PFC

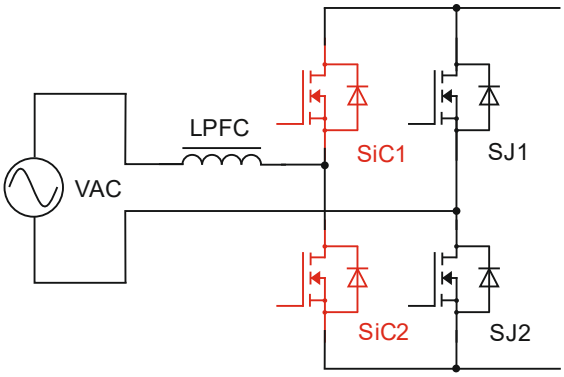

Fig. 4: Schematic of a full-bridge Totem Pole PFC

related losses [1]. This rather simple topology is intrinsically capable to provide a bi-directional power flow and provides the highest practically achievable efficiency. However, the topology imposes serious challenges to the power semiconductors. Fig. 4 indicates two SiC MOSFET in the first half-bridge of the PFC stage. It must be operated at high switching frequencies between 45 kHz ... 100 kHz with one transistor working as boost switch and the other one as synchronous rectifier.

Continuous Conduction Mode (CCM) operation requires switches with lowest-possible Q_{RR}. The output capacitance dependency on the drain voltage must avoid sharp drops as it is typically the case for superjunction (SJ) devices. It is also beneficial to have low output charge Q_{OSS}.

Wide-bandgap power transistors like the SiC MOSFET primarily covered in this work act as an enabler for this highly performant topology. Alternative device choices are represented by GaN HEMT like the CoolGaN™ E-mode GaN power transistor [5] or even latest silicon technologies like the 650 V TRENCHSTOP™ 5 IGBT [6].

Note that the second half-bridge runs only at the power grid frequency of 50 Hz. Here, SJ devices are a perfect choice due to the required low on-resistance.

3 Device concept and reliability

3.1 SiC MOSFET structure

The 650 V SiC MOSFET cell structure is widely identical to that of the already introduced 1200 V MOSFET [7]. Fig. 5 depicts an exemplary structure. The active channel is fabricated in a

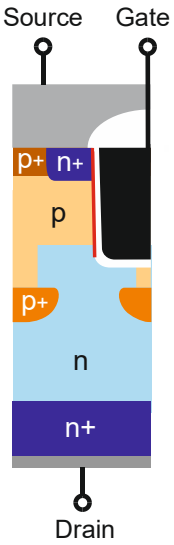

Fig. 5: Exemplary device structure

way that it is exactly oriented along the a-plane <11$\bar{2}$0> which gives the best channel mobility and lowest interface trap density [7]. Hence, the 2nd trench sidewall does not coincide with a crystal plane and, thus, is not used as an active channel. The gate oxide is protected by deep p-wells which are connected to the source electrode at the semiconductor surface. This leads to a very compact cell design and in combination with the high channel mobility of the a-plane to a low on-resistance.

3.2 Device Reliability

The challenge of the reliability of SiC MOS devices is to guarantee a maximum failure rate of less than 1 FIT under given operation conditions in industrial applications. To achieve the targeted reliability one needs to ensure appropriate on-state reliability, off-state reliability and robustness against cosmic ray induced failures.

3.2.1 Gate Oxide Reliability

On-state and off-state reliability are strongly linked to the gate oxide reliability of the device. Since the intrinsic quality and properties of SiO2 on SiC and on Si are almost identical, Si MOSFETs and SiC MOSFETs of the same area and oxide thickness can withstand roughly the same oxide field for the same time. Of course this is only valid if the devices do not contain defect-related impurities, i.e. extrinsic defects, that behave like small spots with a locally thinner oxide. Providing a reliable gate oxide of silicon carbide MOSFETs requires the reduction of the number of critical extrinsics from an initially high number at the end of process (e.g. 1 %) to an acceptable low number when the products are shipped to the customer (e.g. 10 ppm).

One well-established way to achieve this is to apply an electrical screening [9]. The efficiency of this electrical screening depends on the ratio of the screening voltage to the use voltage applied to the gate. The relation is derived from the established linear E-model [10-12]. To reduce the number of critical extrinsics, and thus the field-failure probability, by more than three orders of magnitude, e.g. from 1 % to less than 10 ppm, one has to screen devices with approximately three times the targeted use voltage. In this way Si-like gate oxide FIT rates can be achieved [13]. To be able to stress devices with equal to or more than three times the use voltage, the bulk gate oxide needs to have a certain minimum thickness. In case the gate oxide thickness is too low, devices either fail intrinsically during screening because of wear-out or show a degraded threshold voltage and channel mobility after screening. Screening with a value of “only” twice the use voltage is less efficient by more than two orders of magnitude [7]. Consequently, the enabler for an efficient gate oxide screening is a bulk oxide thickness that is much higher than is typically needed to fulfill the intrinsic lifetime targets.

We have experimentally tested the on-state reliability of electrically screened SiC MOSFETs for 100 days at 150°C and three different combinations of gate oxide process and screening conditions using three individual stress runs at different positive and negative gate stress biases [8]. Each sample group consisted of 1000 pieces. Fig. 6 indicates the results for different gate oxide generations available at different phases of the device development. Mathematically, one may use the linear E-model to extrapolate the result of an accelerated stress test and extract the failure probabilities for typical use conditions, e.g. 20 years and V_{GS} = +15 V, c.f. Fig. 6. After converting the observed failure probabilities at accelerated stress conditions to V_{GS} = +15 V, one obtains a benchmark low ppm failure rate for 20 y. This low number even enables the use of larger on-state gate voltages than 15 V, e.g. V_{GS} = + 18 V, especially for applications which do not require such low ppm

rates or which do not run in on-state for the full 20 y. The use of a higher on-state gate voltage is of course beneficial for the specific on-resistance and the overall performance of the device.

Now the best on-state reliability is worth nothing if devices fail with a much higher probability in the off-state. Since SiC devices allow much higher drain induced electric fields in the blocking mode compared to their Si counterparts, a limitation of the electric field in the gate oxide in the blocking mode is required. This is achieved by the buried p-regions which form JFET-like structures below the accumulation zone of the MOSFET as depicted in Fig. 5. To verify the off-state reliability, we have stressed more than 5000 pieces of 1200 V SiC MOSFETs for 100 days at 150°C at V_{GS} = -5 V and V_{DS} = 1000 V. The condition corresponds to the most critical point of the mission profile for industrial applications. The result was that none of the tested devices failed during this off-state reliability test [8]. As the 650 V technology follows the same design criteria as the 1200 V device, the same reliability is expected.

3.2.2 Cosmic Ray Robustness

As any other high-power device, SiC MOSFETs are also susceptible to single-event burnout (SEB) due to cosmic radiation. There is a certain chance that a power device gets destroyed under blocking conditions if it is hit by a highly-energetic particle which is produced by cosmic ray interactions in our atmosphere. The probability of

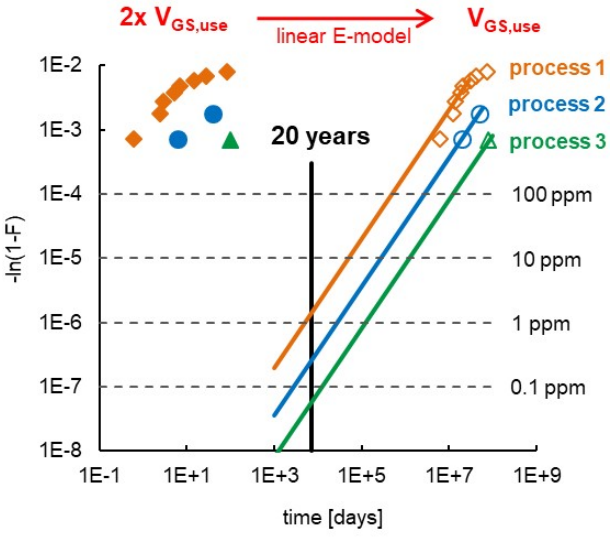

Fig. 6: Evaluation of on-state failure rate [8]

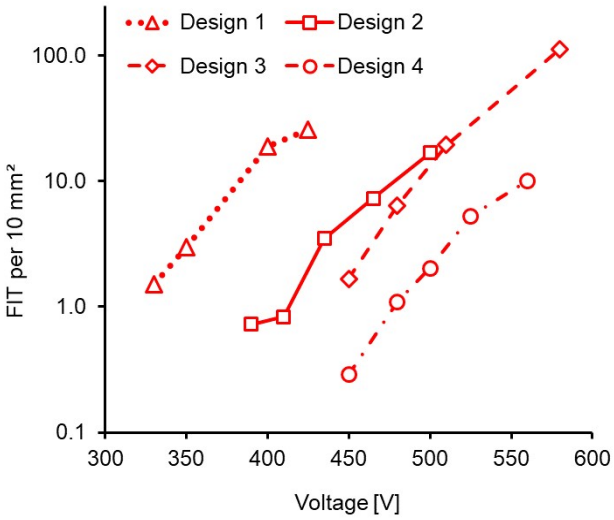

Fig. 7: Cosmic ray robustness of different designs

a failure mainly depends on the real device breakdown voltage, the applied blocking voltage, the time in operation, the operation temperature, and the altitude [14]. As such, cosmic ray robustness is a design parameter and is adjustable for any FIT rate depending on the application specification.

Fig. 7 gives test results for different designs. The FIT rates shown correspond to operation at sea level and room temperature. Design 2 and 3 are capable of fulfilling a typical industrial requirement profile with a failure probability of ≤ 1 FIT at VDS ≤ 420 V while this is not the case for design 1. However, design 1 would offer a clearly lower on-resistance while design 4 offers an even lower FIT rate. A careful optimization of the design helps to minimize the on-resistance increase and to meet the required cosmic ray robustness.

4 Device performance in the target application

4.1 Introduction of test board

A 3.3 kW CCM Totem Pole PFC test board was designed by Infineon. The board has a power density of 73.2 W/inch³ and is fully compliant with server power supplies with an input voltage range of 176 VAC to 264 VAC while the output voltage is 380 VDC. The PFC operates up to an output current of 8.7 A. In this test board, the PWM (pulse width modulation) for the boost stage of the PFC, equipped with the 650 V SiC MOSFET

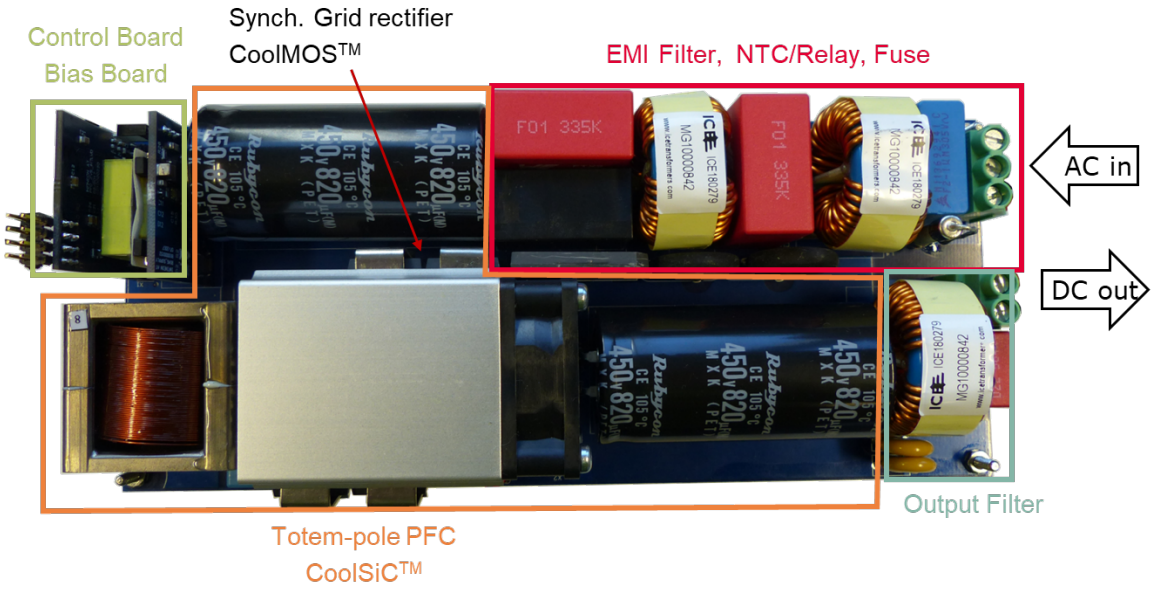

Fig. 8: The Totem Pole PFC test board

introduced in this work, operates at a switching frequency of 65 kHz.

In contrast, the grid rectifier and the return path are operating at the mains grid frequency of 50 / 60 Hz. This means the main requirement for these semiconductors is a low on-resistance, therefore the latest CoolMOS™ devices are a good choice here. Fig. 8 shows the introduced test board.

4.2 Choosing the right package

The choice of the correct package and on-resistance is essential for the achievement of the full device performance. Established standard packages like the TO-247 originate from a time where the switching speed of power devices was substantially lower as for today's wide bandgap devices.

This package contributes a comparatively large parasitic source inductance. This inductance counteracts the gate drive voltage as it is part of both the gate and the power loop, see Fig. 9. In consequence the transients during turn-on and turn-off are slowed down leading to reduced efficiency. In case of fast transients, the MOSFET might be even switched-on during the turn-off

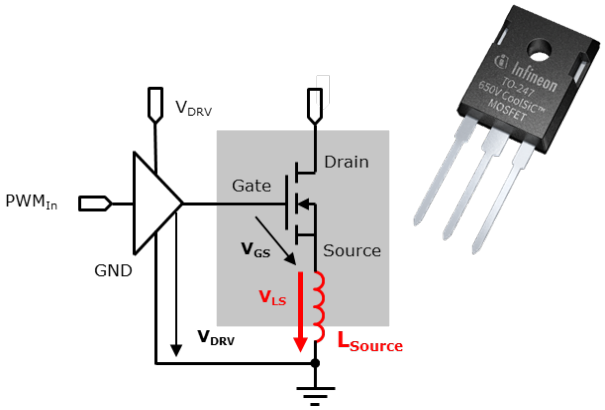

Fig. 9: Standard TO-247-3pin package

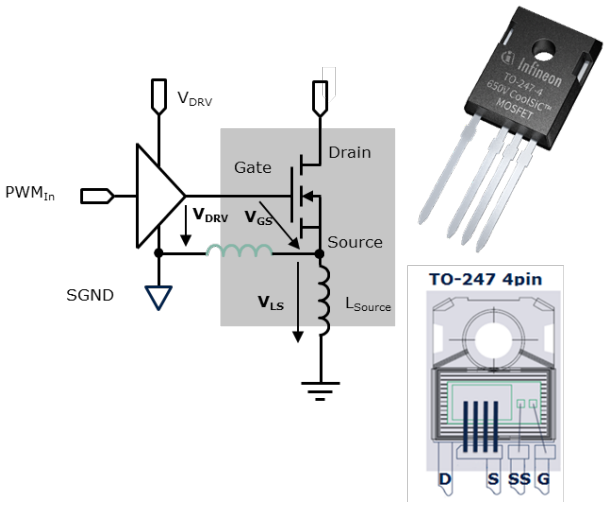

Fig. 10: Novel TO-247-4pin package

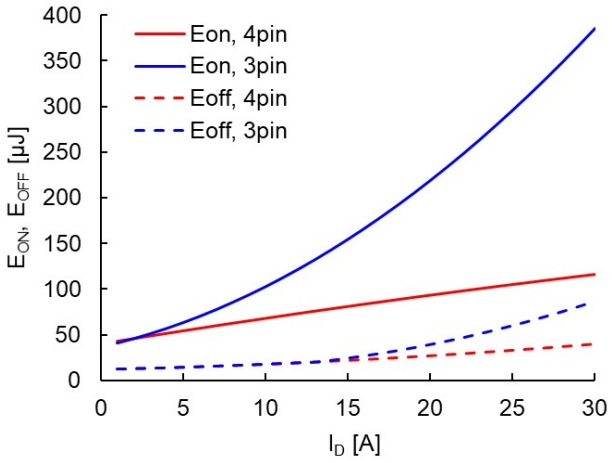

Fig. 11: E_{ON} (straight) and E_{OFF} (dashed) comparison TO-247 3pin (blue) vs. TO-247 4pin (red)

process which further increases switching losses.

Improved derivatives like the TO-247-4pin package, as depicted in Fig. 10, eliminate the feedback from the source inductance on the gate drive. This is gained by a separate source-sense (or Kelvin source) pin that ensures an undisturbed signal from the gate driver. Hence, the package enables a significant switching loss reduction of up to three times that enables a potential for cost reduction in the application. Fig. 11 gives proof of the reduced switching losses. These measurements compare the turn-on and turn-off losses for a device with an on-resistance of 48 mΩ.

Another aspect is a substantially reduced gate ringing as indicated for the turn-on in Fig. 12 and for the turn-off in Fig. 13 that will help to mitigate EMI issues.

4.3 Temperature dependence of $R_{DS(on)}$

Fig. 14 compares the temperature dependence of the on-resistance of a super-junction device with that of a 600 V GaN device, of the 650 V SiC MOSFET and of a 650 V TRENCHSTOP™ 5 IGBT. Note that in case of the IGBT, an equivalent $R_{DS(on)}$ is calculated from the $V_{CE(sat)}$ datasheet values and the current at turn-off for an AC phase angle of 90°.

The on-state resistance of the SiC MOSFET shows the lowest increase of all unipolar devices as the temperature rises. The IGBT owns an even more flat behavior. From an application point of view, a small increase of on-resistance with temperature offers an additional benefit. It means that if all devices come with an identical $R_{DS(on)}$ at the datasheet condition of 25 °C, the real on-state resistance in case of the silicon SJ device is more than 45 % higher and in case of the GaN device 25 % higher for the typical operation junction temperature of ca. 100 °C as in case of the SiC MOSFET. Based on these available characterization results one can now calculate the expected efficiency in the target application.

4.4 Efficiency measurement results

According to the evaluation of the on-resistance temperature dependency, calculations predict the need of a 27 mΩ device to achieve a peak

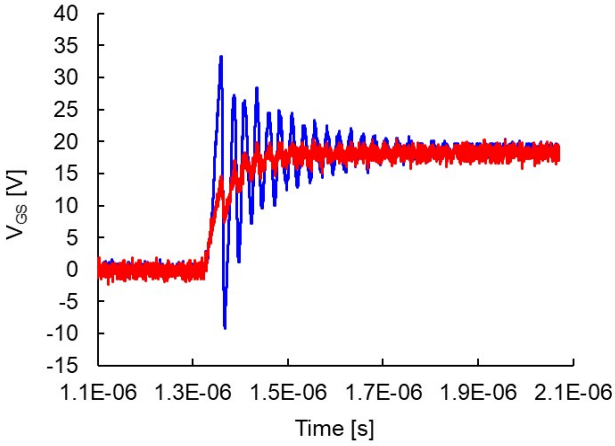

Fig. 12: V_{GS} at turn-on for TO-247 3pin (blue) vs. 4pin (red)

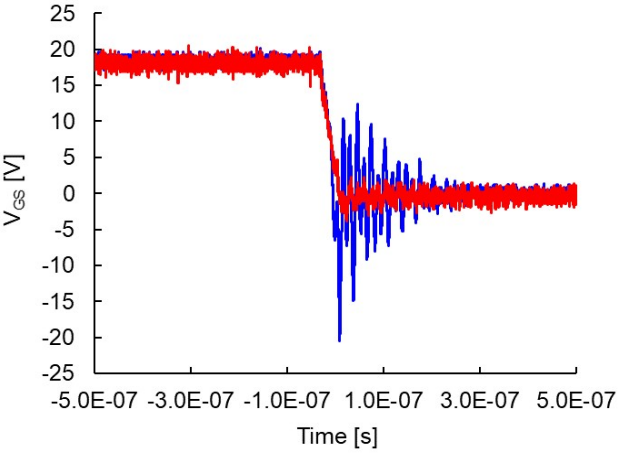

Fig. 13: V_{GS} at turn-off for TO-247 3pin (blue) vs. 4pin (red)

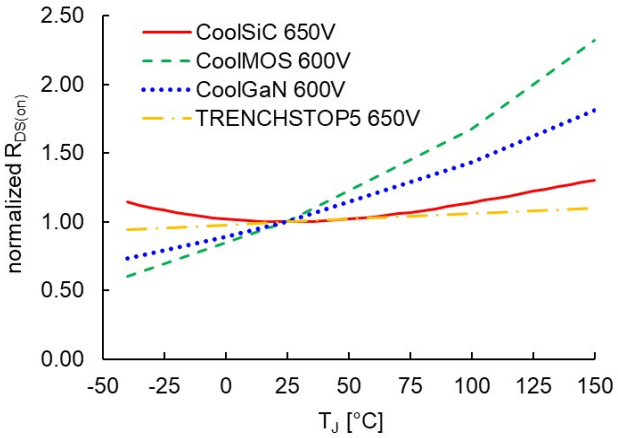

Fig. 14: Temperature dependence of normalized $R_{DS(on)}$ for the different device technologies

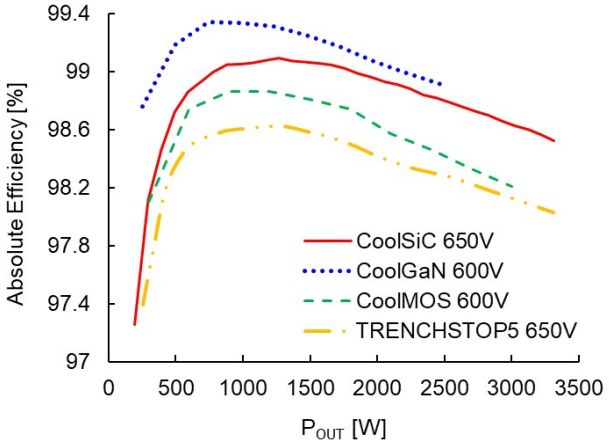

Fig. 16: Comparison of absolute efficiency of the different technologies

efficiency of 99 %. However, aside from efficiency one also needs to care about the overall system costs. In order to create competitive products it is necessary to optimize every SMPS design for the highest efficiency at the lowest system cost and the SiC MOSFET may have a significant impact on the system costs. Fig. 15 shows the efficiency measurements results for different SiC MOSFET devices with on-resistances of 48 mΩ, 72 mΩ and 107 mΩ. The 48 mΩ even exceeds the target value of 99 % while one can still obtain a peak efficiency of 99 % using the 72 mΩ device. This offers good options for SMPS designers to reduce system costs while maintaining a high efficiency. Beside it also indicates the need of appropriate measurements to verify the predicted values of the initial calculations.

Fig. 16 compares the measured efficiencies for

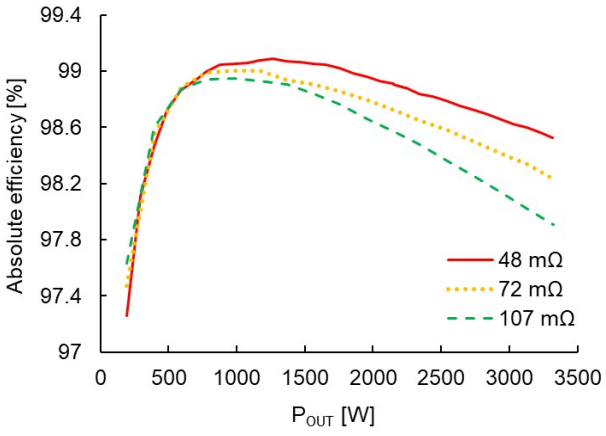

Fig. 15: Absolute efficiency at different $R_{DS(on)}$ of 650 V SiC MOSFET in the CCM Totem Pole PFC

the different devices technologies:

- CoolSiC Trench MOSFET with $R_{DS(on),typ}$ = 48 mΩ in a Totem Pole PFC
- CoolGaN E-mode HEMT with $R_{DS(on),typ}$ = 55 mΩ in a Totem Pole PFC
- TRENCHSTOP 5 IGBT 50 A, equivalent $R_{DS(on),typ}$ = 54 mΩ, in parallel with a 20 A CoolSiC G6 freewheeling diode [15] in a Totem Pole PFC
- CoolMOS P7 (2x) with $R_{DS(on),typ}$ = 26 mΩ in a Dual Boost PFC

Both wide bandgap devices clearly enable efficiencies higher than 99 %. The CoolGaN enables the highest peak efficiency but requires a significant more complex driving scheme. The CoolMOS SJ device used in a Dual Boost configuration delivers a peak efficiency of 98.8 % while the IGBT is still capable to deliver 98.6 %.

5 Conclusion

This work introduces a 650 V SiC MOSFET technology that addresses the needs of switch-mode power supplies targeting a wide range of applications from telecom rectifiers through servers to solar inverters or electric vehicle chargers. The reliability of the developed devices is proven by long-term tests using large device populations. Gate oxide reliability and cosmic ray ruggedness fulfill the requirements for industrial applications.

These devices enable the use of new topologies in the AC-DC conversion part of switch-mode power supplies that yield a higher efficiency. To

verify this improved performance, a 3.3 kW Totem Pole PFC test board design was equipped with the new SiC MOSFET devices and devices from competing technologies. Efficiency measurements yield a peak efficiency of 99.1 % for the SiC MOSFET. GaN HEMT are capable to deliver a higher efficiency of 99.3 % but require a substantially higher gate drive effort.

The low increase of on-resistance with temperature of the current SiC MOSFET device technology, comparable to the rather flat VCE(sat) temperature dependency of IGBTs, enables cost-efficient designs as designers can also choose parts with a higher on-resistance at room temperature.

6 Acknowledgements

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