The Next Step in Power MOSFET Technology Enables Further Increase in Power Supply Efficiencies

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Abstract

This work introduces the new 80 V voltage class of our latest trench power MOSFET technology released to the market. Based on the advantages of a revolutionary new cell design combined with the benefits of an advanced manufacturing technology, the new device technology family combines the benefits of low conduction losses and superior switching performances with an extended SOA and good ruggedness. These features make the devices an ideal fit especially for high switching frequency applications, supporting the trend towards significantly higher efficiency while enabling designs for higher power densities and cost effectiveness.

1 Introduction

Since their introduction, MOSFET technologies have been noted as excellent candidates to be used as switches in power management circuits. Vertical diffused MOSFET (VDMOS) structures, commercially available since the late seventies, first addressed the needs of a power switch [1]. The superior switching performance and the high input impedance placed the MOSFET as an appealing alternative to bipolar technologies. Still, the high on-state resistance limited the current-handling capabilities of the VDMOS and its applications in the power electronics industry. In a medium-voltage VDMOS, the major contributors to the total on-state resistance between drain and source are represented by the intrinsic channel resistance and by the JFET region limiting the channel current flow into the epitaxially-grown drift region (Fig. 1a). Overcoming this limitation required more than a decade of development in device design and process engineering, which culminated in the late 1980s with the commercialization of the first trench gate MOSFETs. The development of trench power MOSFETs was a milestone for the broad adoption of field-effect transistors in the power electronics industry [1-3]. By moving the channel to the vertical direction, this device concept allowed a reduction in cell pitch without adversely affecting the current spreading by virtually removing the JFET region, hence dramatically reducing the on-state resistance (Fig. 1b). The achieved ultralow specific channel resistance no longer prevented low on-state resistances, although as a result the substrate and package resistances became significant contributors.

However, the remarkable increase in cell density, besides finally establishing the trench MOSFET as a competitive alternative to the planar technology, has also brought to light significant disadvantages.

The gate-drain capacitance (related to trench gate penetration in the epi drift region) and gate-source capacitance (overall capacitance between trench gate and source diffusion) increase linearly with the number of trenches, i.e. with the cell density.

Together with a sublinear scaling in the on-resistance $R_{DS(on)}$, this significantly impacts the technology figure-of-merit $FOM_g = R_{DS(on)} \times Q_g$. Since the MOSFET is uniquely controlled through its gate terminal, the gate driver circuitry has to provide the total gate charge Q_g required to turn on the transistor. In the case of high switching frequency applications, like switched-mode power supplies (SMPS), the lowest gate charge is

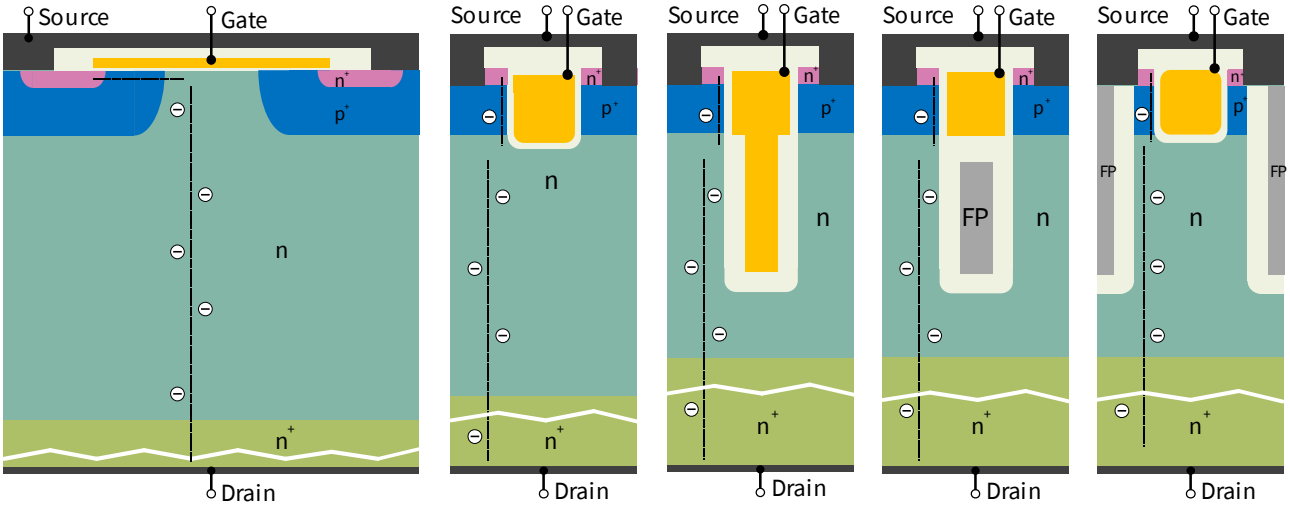

Fig. 1 Exemplary device structures depicting the evolution of power MOSFET:
a) VDMOS structure with lateral channel and planar gate
b) Trench MOSFET structure with vertical channel
c) Trench MOSFET with lateral charge-compensation by a gate-connected field plate
d) Trench MOSFET with lateral charge-compensation by an insulated field plate connected to source
e) Trench MOSFET with lateral charge-compensation by an insulated field plate and separated gate trench

desirable since it proportionally reduces the driving losses. A part of the total gate charge is associated with the gate-to-drain charge Q_{gd}, which governs the drain voltage transient. A higher Q_{gd} impacts the transient speed, increases the switching losses, and forces the use of longer dead-times. It became evident that specific measures were needed to reduce the overall gate and gate-drain charge. Additionally, another constraint is imposed by the Miller charge ratio: $Q_{gd}/Q_{gs(th)}$ must be lower than one in order to guarantee the intrinsic robustness against parasitic turn-on of the MOSFET under fast drain voltage transients [4].

A new era started with the introduction of charge-compensated structures, exploiting the same principle as super junction devices. The introduction of devices which use an insulated deep field plate as an extension of the gate electrode enabled the lateral depletion of the drift region in the off state (Fig. 1c) [5]. The lateral depletion alters the electric field distribution throughout the structure, allowing the same voltage to be blocked within a shorter length. Since the electric field can be supported by a thinner and more heavily doped drift region, a substantial reduction in the on-state resistance can be achieved. It is worth noticing that the field plate (as an extension of the gate electrode) leads to both a significant increase of the reverse-transfer capacitance C_{gd} (hence also Q_{gd} and Q_g) and a nonlinear dependence on the drain voltage. In fact, the transfer capacitance drops abruptly as soon as the mesa region completely depletes. These disadvantages were soon overcome by the use of a field plate, which was isolated from the gate electrode and instead electrically connected to the source potential (Fig. 1d). While the charge compensation principle operates as before, the buried field plate does not introduce any additional contributions to the gate-drain capacitance. Instead, the field plate shields the gate electrode from the drain potential, which reduces the gate-drain capacitance C_{gd} and related charges. These devices, at the time of their introduction to the market, showed best-in-class performance with low gate charge and gate-drain charge characteristics, high switching speeds and good avalanche ruggedness [6]. Still, the presence of the field plate comes with the disadvantage of an increased output capacitance C_{oss} and output charge Q_{oss} - a consequence of the lateral charge-compensation. However, careful device optimization enabled field plate-based power technologies with FOM_{oss} comparable to those of the standard trench MOSFET [7,8]. These attributes made them even more suitable for a wide variety of switched-mode power supply (SMPS) applications.

2 Novel cell concept

New MOSFET devices are required to provide improvements across all figures of merit, as this is

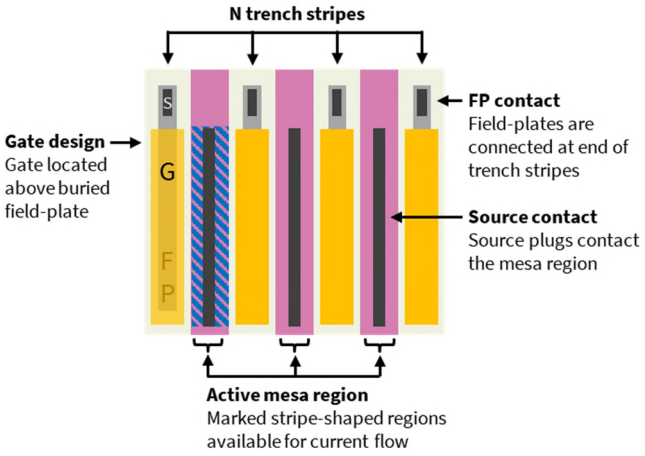

Fig. 2 Typical Trench MOSFET with commonly employed stripe layout approach in the chip design

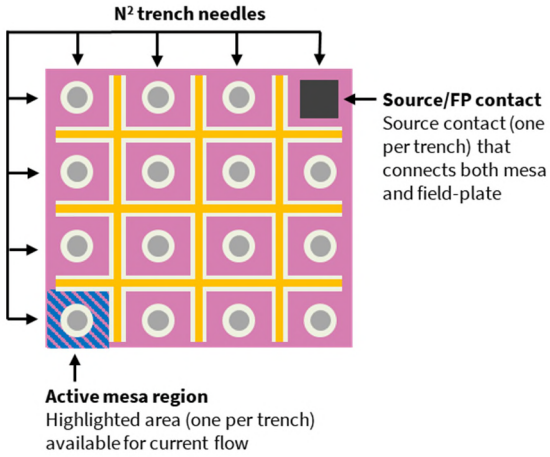

Fig. 3 Trench MOSFET structure with the new grid-like layout approach in the new chip design

needed to enable high-frequency SMPS operation where losses are associated both with charges (switching) and on-state resistance (conduction). To meet these requirements, a novel cell-design approach was developed, which explores a true three-dimensional charge compensation.

State-of-the-art MOSFET technologies currently use an insulated deep field plate underneath and separated from the gate electrode. These employ a stripe layout as depicted in Fig. 2. The new generation separates the field plate trench, which is formed with a needle-like structure, from a grid like gate trench which surrounds the needles [9]. Fig. 3 depicts this changed layout, while Fig. 1e shows the schematic cell cross section. This increases the silicon area available for current conduction, allowing for a further reduction in the overall on-resistance [9]. In order to further reduce the $FOM_g = R_{DS(on)} \times Q_g$ and $FOM_{gd} = R_{DS(on)} \times Q_{gd}$ values, the gate trench underwent a complete redesign to minimize its lateral extension.

However, the substantially smaller dimensions of the gate impose a new challenge, as the use of polysilicon as gate material would result in unacceptably large internal gate resistances. This issue is usually solved by the introduction of gate fingers but these reduce the active area available for current conduction, as shown in Fig. 4. To avoid this rather significant loss of active area, a metal gate system has been introduced that not only reduces the internal gate resistance, but also significantly improves the gate resistance uniformity over the chip [9]. Together with a direct connection of the field plates to the source metal, a device set-up is realized that not only ensures a very fast and homogeneous transition at turn-on and turn-off that minimizes switching losses, but also reduces the risk of an unwanted, dv/dt induced parasitic turn-on of the MOSFET.

Fig. 5 summarizes the improvements in the main parameters.

3 Benefits in application

3.1 1 kW, 4:1 IBC for datacenters

The first test platform is represented by a 1 kW 4:1 open-loop LLC DC-DC intermediate bus converter

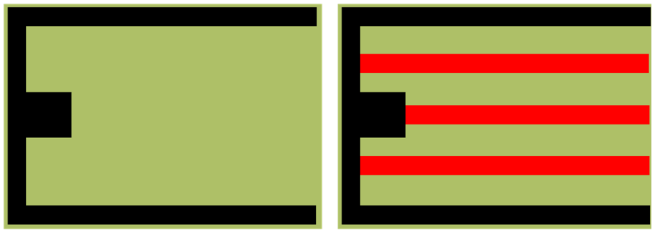

Fig. 4 Illustration of active area loss on a MOSFET chip due to the introduction of gate fingers (red)

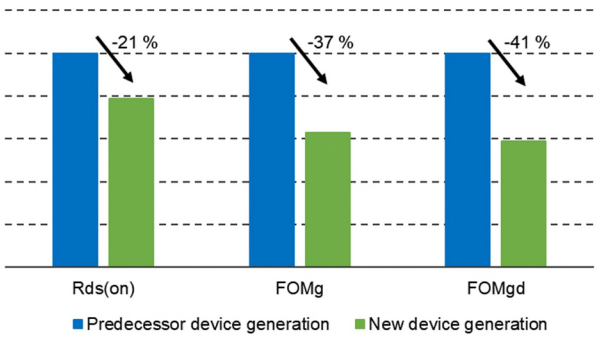

Fig. 5 Gained improvements in device performance for a best-in-class 80 V device in PQFN 5x6 package

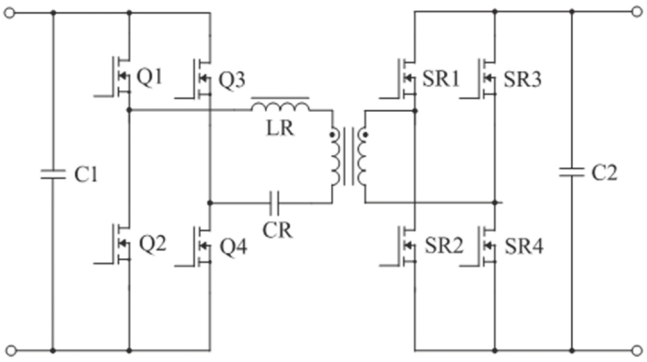

Fig. 6 Basic schematic of the LLC DC-DC test boards

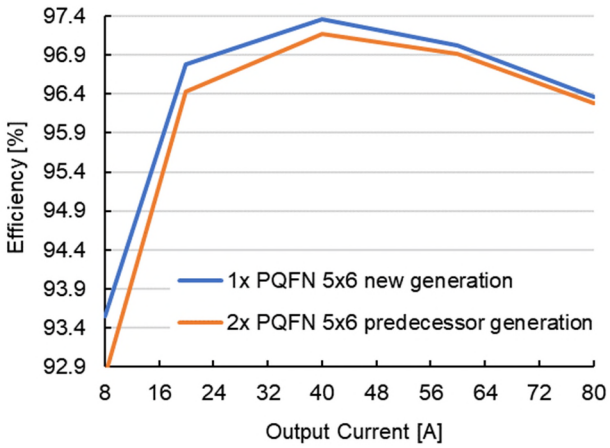

Fig. 8 Comparison of the gained efficiency improvement in the 1 kW 4:1 LLC DC-DC converter (V_{IN} = 54 V)

(IBC), operating as a DC transformer from an input which may vary from 42 V to 60 V. Soft-switching techniques as employed in the LLC resonant topology allow a significant efficiency improvement in telecom and server power supplies [10-12]. While these techniques reduce losses on the primary-side, secondary-side rectification-related losses can be dramatically reduced by the use of power MOSFETs acting as synchronous rectifiers (SR) [13]. As for any switched power device, the SR MOSFET switching losses contribute to the overall losses, so improving the switching performance of new technologies is the key for increasing the overall efficiency.

Here, two 80 V MOSFETs in PQFN 5x6 mm^2 are paralleled on the primary-side full-bridge, while four 25 V, PQFN 3.3x3.3 mm^2 source-down devices are used in parallel on the secondary-side, arranged in a full-bridge configuration (Fig. 6). The turns ratio of the transformer is 4:1. The resonant frequency of the LLC converter is 310 kHz. The switching frequency is fixed, so that the converter operates at resonance over the whole input voltage and load range. ZVS (zero voltage switching) for the primary-switches and ZVS / ZCS (zero current switching) for the SR switches are achieved by design. Fig. 7 gives a view of the board which spans over a standard quarter-brick form factor.

The use of different device generations on the primary-side calls for the use of different dead-times. For running comparable tests, the dead-times are adjusted so that the effective body diode conduction time is the same for both devices under investigation. The significantly improved device parameters of the new technology generation not only improves the overall efficiency of the converter, but also allows two paralleled PQFN 5x6 mm^2 MOSFETs ($R_{DS(on)}$ = 3 mΩ) on the primary side to be replaced by a single device ($R_{DS(on)}$ = 1.5 mΩ). Fig. 8 compares the efficiency in this case, revealing an efficiency improvement over the full load range, with up to 0.8 % better

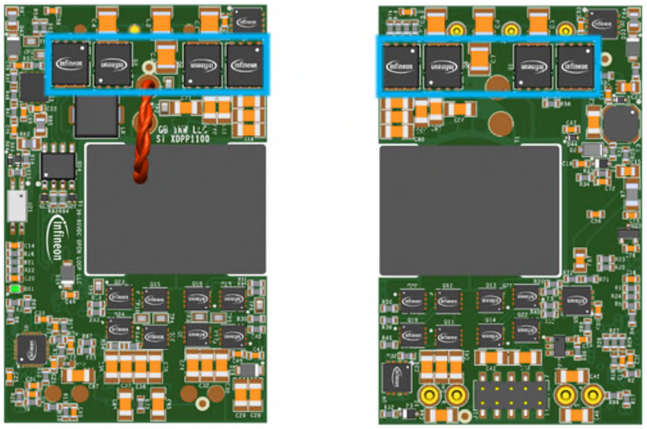

Fig. 7 Top and bottom view of the 1 kW LLC DC-DC board with the primary side MOSFET marked in blue

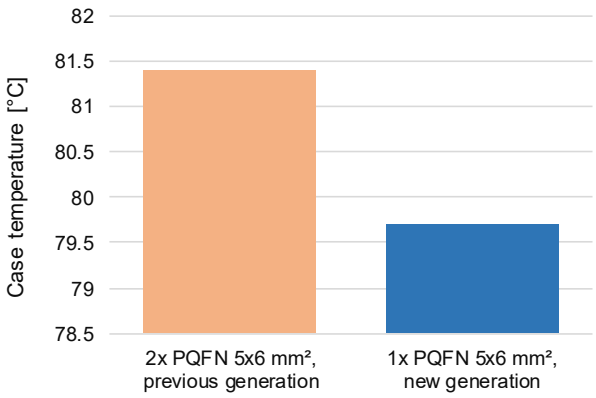

Fig. 9 Case temperature for the different devices in the 1 kW LLC converter at maximum output current

values using the latest device technology. Fig. 9 even indicates a lower case temperature for the single die of the new generation compared to the two from the previous generation.

3.2 600 W IBC for telecom applications

The second test platform served for studying the device behavior and efficiency under hard-switching conditions. Such DC-DC converters are widely used in telecom and datacom power systems, typically as isolated DC-DC intermediate bus converters in the overall conversion chain with a nominal - 48 V input (overall range from - 36 V to - 75 V) and a 12 V output voltage bus for the downstream point-of-load converters [14]. The fully regulated converter operates at a switching frequency of 250 kHz and can deliver an output current of maximum 50 A.

The test board employs a full-bridge topology on the primary side and a center-tapped full-wave rectifier on the secondary side as depicted in Fig. 10. Turns ratio is 3:1. To enable an assessment of the efficiency, the investigated 80 V devices are used as synchronous rectifiers on the secondary side.

Fig. 11 shows the top and bottom view of the converter. As depicted, the converter originally employed four paralleled 80 V MOSFETs in PQFN 5x6 mm^2 on the secondary side. The advantages reached with the new device technology enables a replacement with four PQFN 3.3x3.3 mm^2 packages. This allows a shrink in the design saving 64 % in PCB area allocated for the SR switches.

Fig. 12 compares the measured efficiency values. Low-load efficiency improves by ~1% while the mid- to full-load efficiency also improves up to 0.3 %. The thermal images, shown in Fig. 13, reveal that the smaller devices of the latest technology even operate at 2°C lower temperature at full load.

This remarkable improvement is mainly attributed to the lower gate- and gate-drain charges Q_g and Q_{gd}, and from a lower reverse-recovery charge Q_{rr}. As can be seen from Figs. 2 and 3, the new device structure inherently offers a larger area for the current flow when compared to the predecessor device structure. The body diode current density reduces for the same current level in the application, and with it the reverse-recovery charge. Consequently, by replacing two devices with a single device operating at a higher current density, the negative effects of an increased Q_{rr} are avoided.

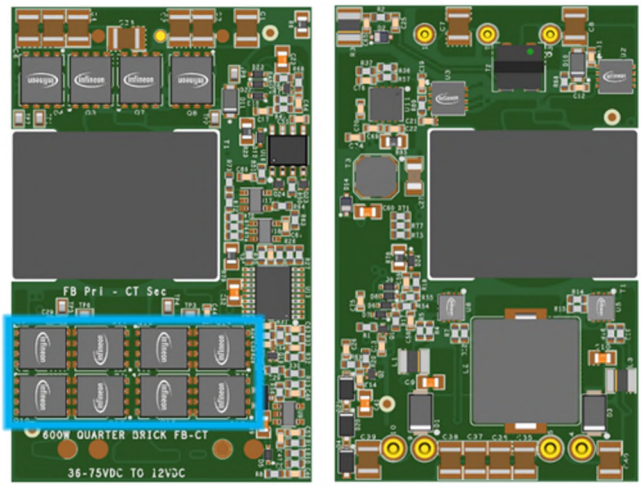

Fig. 11 Top and bottom view of the 600 W IBC board with the secondary side MOSFET marked in blue

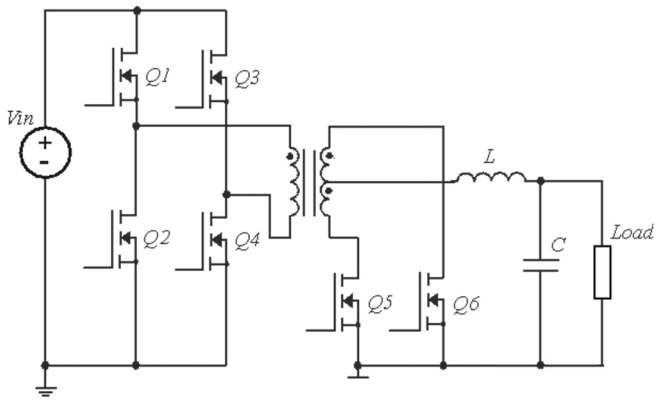

Fig. 10 Basic schematic of the 600 W DC-DC IBC test board

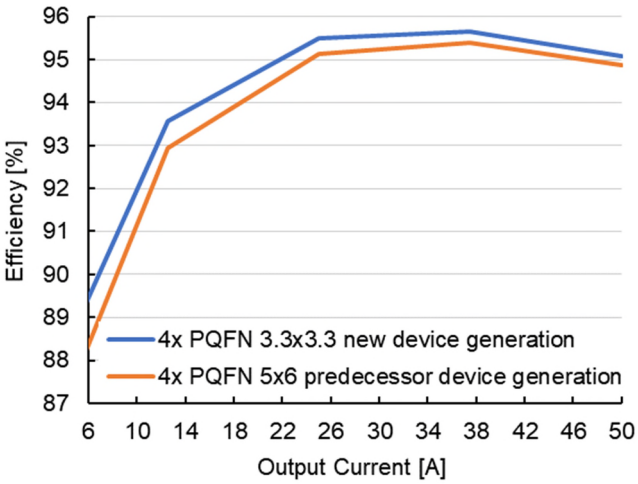

Fig. 12 Comparison of the gained efficiency improvement in the 600 W IBC (V_{IN} = 54 V)

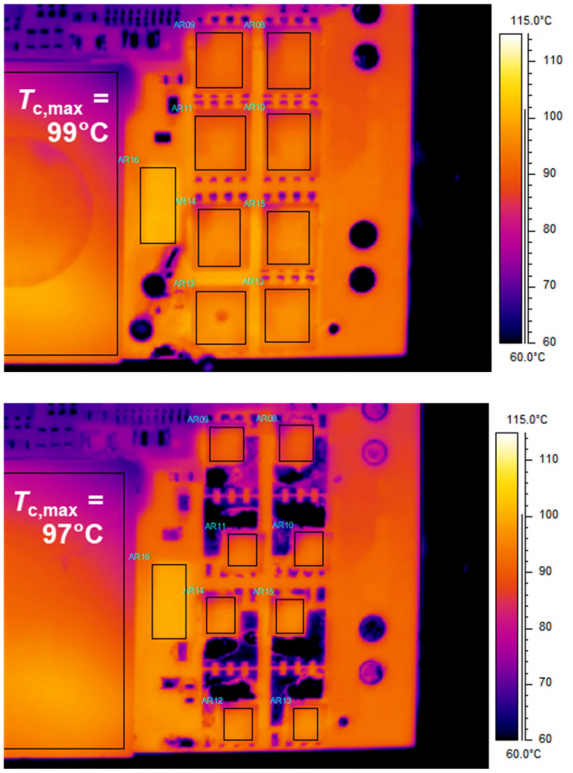

Fig. 13 Temperature for the use of 4x PQFN 5x6 mm² devices of predecessor generation (top) with 4x PQFN 3.3x3.3mm² devices of the new generation (bottom)

3.3 3.6 kW LLC DC-DC converter

Finally the device behavior is also studied on the secondary side, i.e. as synchronous rectifier, of a 3.6 kW LLC DC-DC converter which converts an input voltage of 360…400 V to a regulated output of 52.5 V. To regulate the output voltage, the control board varies the switching frequency, with the resonant frequency being 350 kHz.

Fig. 6 depicts the basic schematic of the LLC converter, while Fig. 14 shows the assembled system. Devices of roughly the same $R_{DS(on),max}$ of

Fig. 14 View of the employed 3.6 kW LLC DC-DC test board

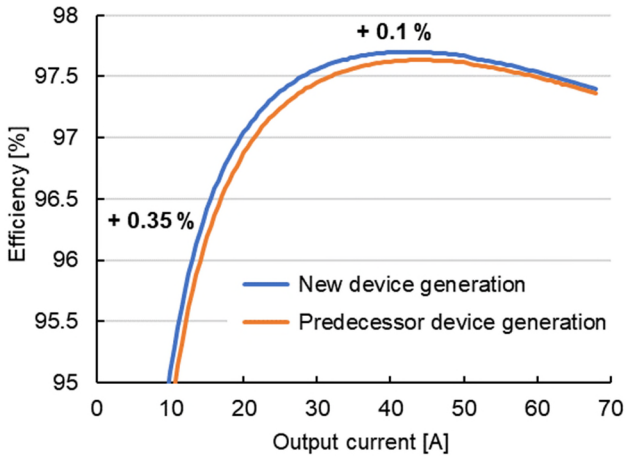

Fig. 15 Comparison of gained efficiency in the 3.6 kW LLC DC-DC test board (V_{IN} = 385 V, f_{SW} = 350 kHz)

about 3 mΩ from previous and new generations, in PQFN 5x6 mm², are compared in this converter.

Fig. 15 compares the efficiency in the converter using the new 80 V device with the one reached by using the previous device generation. Especially at light-load, where the efficiency improves by 0.35 %, the effects of the improved FOMs become visible.

4 Summary

This work introduces the new 80 V voltage class that extends our latest power MOSFET technology family. The new technology shows improvements in all important device parameters and combines the benefits of low on-state resistance with a superior switching performance. The new technology is specifically optimized for high switching frequency applications such as telecom SMPS and solar.

This remarkable jump in the overall device performance is enabled by substantial improvements at the device technology level. This has culminated in a unique device structure, which is the first to employ a three-dimensional charge compensation combined with the first ever use of a metal gate in a trench power MOSFET.

The reduction achieved in the on-resistance, the dramatically-lowered gate charge and gate-drain charge, together with a low output charge and improved switching homogeneity across the device area, enhance the system efficiency in the tested applications across all load conditions. The new device structure is also beneficial for the internal body diode of the MOSFET. Because the silicon area conducting current is increased, the

body diode current density is decreased which, for the same current level, means a decreased reverse recovery charge.

Efficiency measurements in several SMPS applications under hard- and soft-switching conditions confirm the findings at the semiconductor device level. Efficiency improvements of up to 1 % are possible, depending on the topology and load condition. It is verified that the much better device performance allows a reduction of up to halve the number of required devices, or alternatively the use of smaller footprints, without having a negative impact on the temperature of the devices.

Overall, these improvements offer a significant improvement for the demanding requirements of the telecom power arena and other application fields.

5 Acknowledgements

We thank Marco Kuenstel for performing the various efficiency measurements in the test boards, Cedric Ouvrard for his contributions to TCAD simulations, Jeff Malmrose and Yevgeniy Trosman for the test platforms development, and Mark Stem for the board layouts. We also want to thank Adrian Finney for carefully editing this article.

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