Evolution of reverse recovery in trench MOSFETs

A. Ferrara, R. Siemieniec, U. Medic,
M. Hutzler, O. Blank
Infineon Technologies Austria AG
Siemensstrasse 2, 9500, Villach, Austria
E-mail: alessandro.ferrara@infineon.com

T. Henson
Infineon Technologies Americas Corp.
101 N. Pacific Coast Highway
El Segundo, CA 90245 USA

***Abstract*—The interaction between the reverse recovery charge and the output charge in trench power MOSFETs is discussed. As the trade-off between the on-resistance and the gate charge improves, the output capacitance has more impact on the reverse recovery losses. The evolution of reverse recovery with trench technology is investigated by double-pulse measurements and TCAD simulations.**

Keywords—reverse recovery; body diode; output capacitance; trench MOSFET; split-gate; RESURF; lifetime killing

I. INTRODUCTION

Medium voltage MOSFETs have evolved in recent years by the introduction of the split-gate technology, resulting in improved specific on-resistance $R_{ds(on)} \cdot A$ (Fig. 1) [1]. The gate charge Q_g has also been reduced by shrinking the channel length and using thicker gate oxides. As the figure of merit (FOM) $R_{ds(on)} \cdot Q_g$ improves, the static and gate switching losses are reduced, and in many applications a significant loss contribution comes from the body diode reverse recovery charge Q_{rr} and the output charge Q_{oss}. The aim of this paper is to investigate the impact of this technology evolution on the reverse recovery behavior of the body diode. Great emphasis is put on the interaction between Q_{rr} and Q_{oss}, which plays a significant role in modern trench MOSFETs.

By analyzing the datasheets of 80V and 100V trench power MOSFETs in PFQN 5x6 packages, it is found that the ratio between Q_{rr} and Q_{oss} decreases as the FOM $R_{ds(on)} \cdot Q_g$ improves (Fig. 2). Despite the wide spread on the data, it is evident that the latest generation MOSFETs with the lowest $R_{ds(on)} \cdot Q_g$ populate the bottom left corner of the chart in Fig. 2.

Before investigating this trend further, it is useful to recall the JEDEC definition of recovered charge Q_{rr} [2]:

The total amount of charge recovered from a diode, including the capacitive component of charge, when the diode is switched from a specified conductive condition to 1) a specified nonconductive condition, or 2) an unspecified nonconductive condition with the measurement ending after a specified integration time, t_I, with other circuit conditions as specified.

Based on this definition, the ratio Q_{rr} / Q_{oss} should always be larger than one – becoming exactly one when the reverse recovery is purely capacitive, meaning that $Q_{oss} = Q_{rr}$. However, some data points in Fig. 2 show $Q_{rr} / Q_{oss} < 1$, which can be attributed to two different reasons: (1) Q_{oss} is subtracted from the measured Q_{rr} value, or (2) a measurement setup is used where the drain voltage spike during reverse recovery is suppressed to minimize the Q_{oss} contribution. Since the JEDEC standard does not specify to which voltage the output capacitance should be charged in a Q_{rr} measurement, the method (2) is a perfectly legitimate way to minimize the Q_{rr} value on datasheets. As a result, a simple datasheet analysis of Q_{rr} and Q_{oss} is not sufficient to draw conclusions, and a more detailed investigation is needed.

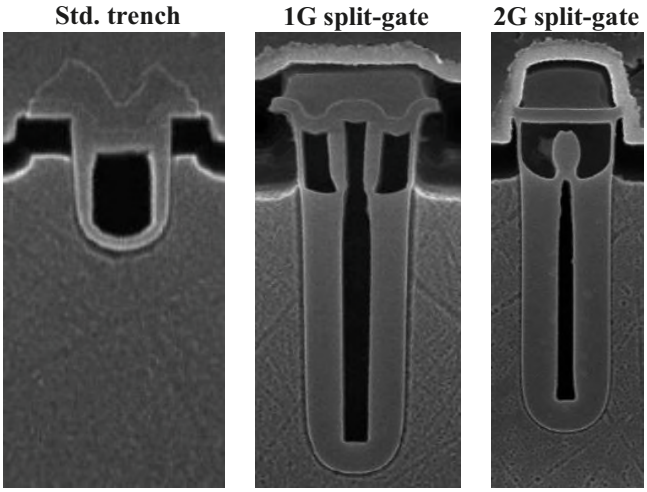

Fig. 1. Evolution of 100V trench MOSFETs: ***left)*** standard trench MOSFET, ***center)*** 1st generation split-gate, ***right)*** 2nd generation split-gate. The 2G split-gate has a narrower pitch and a shallower trench compared to 1G [1].

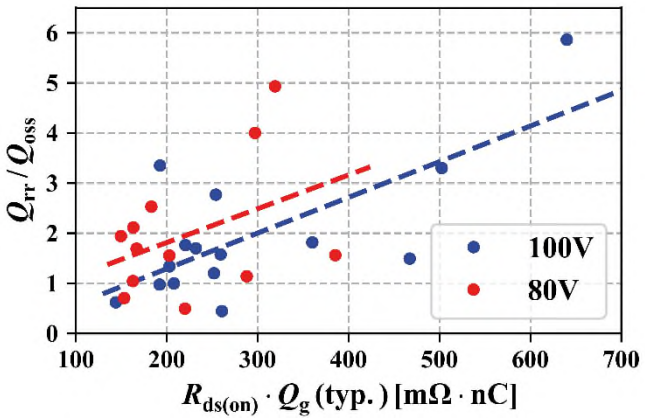

Fig. 2. Ratio between reverse recovery charge (Q_{rr}) and output charge (Q_{oss}) as a function of the figure of merit (FOM) $R_{ds(on)} \cdot Q_g$ for 80V and 100V power MOSFETs from different manufacturers. Data points are datasheet values for best-in-class devices in PQFN 5x6 package. When not specified in the datasheet, Q_{oss} was extracted by integrating the output capacitance C_{oss} up to half of the breakdown voltage.

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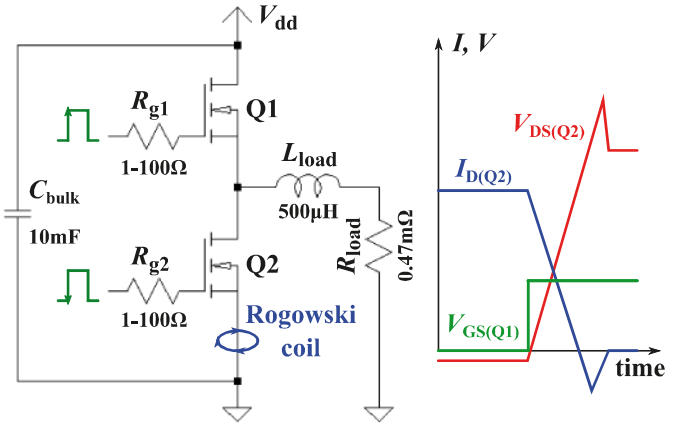

Fig. 3. Schematic of the double-pulse setup for Q_{rr} characterization (half-bridge). The drain current of Q2 $I_{D(Q2)}$ is measured with a Rogowski coil.

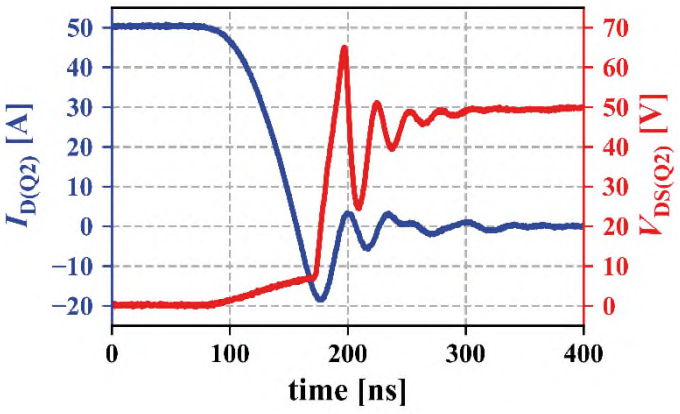

Fig. 4. Measured reverse recovery waveforms for a 2G split-gate 100V MOSFET in PQFN 5x6 package on the setup in Fig. 3. The drain current $I_{D(Q2)}$ is shown on the left axis (blue), the drain voltage $V_{DS(Q2)}$ on the right axis (red). Measurement conditions are V_{dd} = 50V, I_D = 50A and di/dt = 1000A/µs, achieved with a gate resistance R_{g1} = 93Ω.

II. Experimental Setup

The evolution of Q_{rr} and Q_{oss} with technology generation is investigated on three 100V MOSFETs: standard trench MOSFET, first generation (1G) split-gate and second generation (2G) split-gate. An exemplary cross-section of the devices under test is shown in Fig. 1 [1].

Q_{rr} is measured on a double-pulse setup (Fig. 3) as a function of the load current and the current roll-off di/dt. Q_{oss} is measured in both the time and the frequency domains. The time domain value is extracted from a double-pulse measurement at zero current, by disconnecting the load. The frequency domain value is obtained by integrating the output capacitance C_{oss} measured vs. the drain-to-source voltage V_{ds} on a frequency analyzer at 200kHz.

A. Double-pulse setup

A schematic of the double-pulse setup is shown in Fig. 3. The device under test (DUT) is placed on both the high-side (Q1) and low-side (Q2) of a half-bridge configuration, while the reverse recovery is measured on Q2.

When Q1 is off, the current on the inductor L_{load} is freewheeling on the body diode of Q2. When Q1 is turned on, the charge stored in the body diode of Q2 has to be recovered before the MOSFET can turn off. The slope of the current roll-off di/dt is determined by the variable gate resistance R_{g1}, which affects the turn-on time of Q1. Since R_{g1} is much larger than the internal gate resistance of Q1, the gate time constant of Q1 is $\tau_{g1} \approx R_{g1} \cdot C_{iss}$(Q1) and the d$i$/d$t$ is determined by the linear-mode current of Q1, operating as a gate-controlled current-source:

$$I_D(\mathrm{Q1}) \approx g_m \left\{ V_{gs} \left[1 - \exp\left(-\frac{t}{R_{g1} \cdot C_{iss}} \right) \right] - V_{th} \right\}, \qquad (1)$$

where V_{th}, g_m and C_{iss} are the threshold voltage, transconductance and input capacitance of Q1, respectively. Notice that Eq. (1) is non-linear resulting in a non-constant di/dt over time. In practice, Eq. (1) is difficult to apply since it requires a preliminary characterization of the MOSFET gate charge and transfer curves. For these reasons, the di/dt is set by trial and error by adjusting the value of R_{g1}.

B. Experimental results

An example of the measured drain current and voltage waveforms for a 2G split-gate 100V device is shown in Fig. 4. The drain current of Q2 $I_{D(Q2)}$ is measured with a Rogowski coil on the device source. Q_{rr} is extracted by integrating the total area under the current waveform where $I_{D(Q2)} \leq 0$, up to the first zero-crossing (thus excluding oscillations).

The measured Q_{rr} and Q_{oss} values on the three DUTs are multiplied by the typical $R_{ds(on)}$ and plotted in Figs. 5-6. In Fig. 6, it can be seen that a good agreement is achieved between the time and frequency domain measurements of Q_{oss}.

The 2G split-gate has the lowest $R_{ds(on)} \cdot Q_{rr}$, with a ~2x improvement over the previous generations. Split-gate MOSFETs are RESURF technologies [3, 4] with a higher $R_{ds(on)} \cdot Q_{oss}$ than a standard trench MOSFET because of the extra field-plate capacitance and higher drift doping concentration. Nevertheless, the 2G split-gate improves the $R_{ds(on)} \cdot Q_{oss}$ of the first generation by reducing the field-plate depth thanks to better tolerances in the trench etch process [5].

III. TCAD Analysis

A. Simulation method

The TCAD setup is similar to the double-pulse schematic in Fig. 3, but a simplification has been made. To avoid the trial and error di/dt adjustment by fine-tuning R_{g1}, the high-side switch Q1 is replaced by a SPICE level-1 MOSFET model, only defined by the parameters K_p and V_{to}. This allows to control the drain current waveform – and therefore di/dt – by applying a well-defined V_{gs} signal on the gate of Q1:

$$V_{gs}(t) = V_{to} + \sqrt{\frac{2I_D(t)}{K_p}}. \qquad (2)$$

B. Separation of displacement and stored charge

In TCAD, it is possible to look at the composition of the reverse recovery current during the turn-off of Q2. As discussed by Hossain *et al.* in [6], this current is the result of different

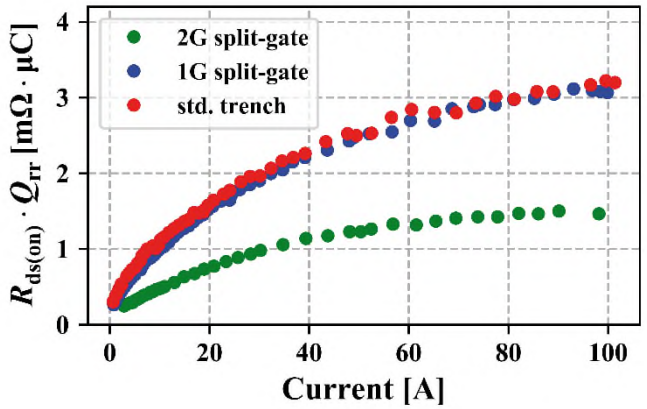

Fig. 5. Measured $R_{ds(on)} \cdot Q_{rr}$ vs. current for three generations of 100V MOSFETs. Q_{rr} is measured on the setup in Fig. 3 with di/dt = 1000A/μs, and the values are multiplied by the typical $R_{ds(on)}$ for comparison.

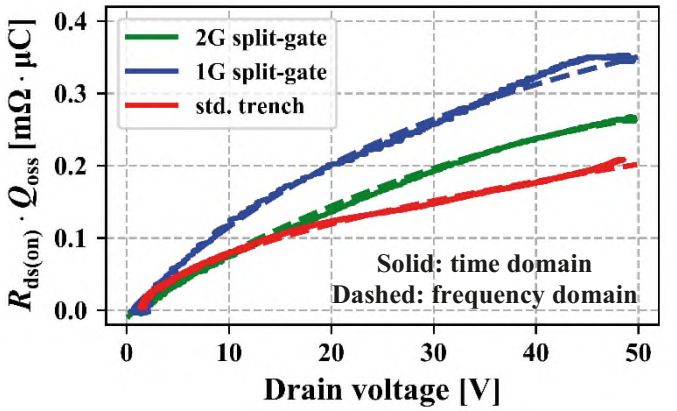

Fig. 6. Measured $R_{ds(on)} \cdot Q_{oss}$ vs. drain voltage for three generations of 100V MOSFETs. The solid curves are time domain measurements on the setup in Fig. 3 – with the load disconnected to achieve zero output current. The dashed curves are measured with a frequency analyzer at a frequency of 200kHz.

contributions: the gate-to-drain, drain-to-field-plate and drain-to-source capacitance currents and the *p/n* junction current. These currents are here distinguished as displacement (capacitive) current and *p/n* junction current. The time integral of the displacement current is the output charge Q_{oss}, while the time integral of the *p/n* junction current is the stored charge Q_s that has to be recovered from the diode. The total Q_{rr} is the sum of Q_{oss} and Q_s (Fig. 7).

Notice that the capacitive current flowing during reverse recovery is affected by the presence of charge carriers in the drift region – *i.e.*, the stored charge Q_s due to the *p/n* junction current. When Q_{oss} is measured on a time or frequency domain setup (Fig. 6), the *p/n* junction current is *not* flowing into the diode. As a result, the measured Q_{oss} is not exactly the same as the displacement current flowing *during* reverse recovery. While this difference does not affect the outcome of this work, it certainly needs further investigation for an accurate separation of Q_{oss} and Q_s directly from double-pulse experiments.

C. TCAD results

The simulated reverse recovery waveforms on the three generations 100V MOSFETs are shown in Fig. 7. In the standard trench MOSFET, Q_{oss} is a small fraction of Q_{rr} and only appears towards the end of the reverse recovery. In the split-gate MOSFETs, Q_{oss} appears from the beginning of the reverse recovery, with a magnitude comparable to Q_s. The split-gate introduces an additional Q_{oss} component due to the field-plate displacement current, but at the same time reduces Q_s resulting a lower Q_{rr} / Q_{oss} ratio, as discussed in the next section.

IV. Evolution of Reverse Recovery

In standard trench MOSFETs, the hole injection efficiency of the body diode is high because of the low drift doping concentration, determined by the 1D silicon limit. The large amount of stored charge Q_s causes high reverse recovery losses during switching. On the other hand, Q_{oss} is low because of the absence of charge compensation (RESURF). In split-gate MOSFETs, the high drift doping concentration reduces the hole injection efficiency and lowers Q_{rr}, at the expenses of a higher Q_{oss} [7]. Therefore, as the specific on-resistance $R_{ds(on)} \cdot A$ and the FOM $R_{ds(on)} \cdot Q_g$ are improved, the ratio Q_{rr} / Q_{oss} reduces, as shown in Figs. 7-8. Both experimental and TCAD results support the noisy datasheet trend in Fig. 2.

It is worth noting that the Q_{rr} / Q_{oss} ratios in Fig. 7 (TCAD) and Fig. 8 (double pulse experiments) are larger than most datasheet values in Fig. 2. This is due to the difference in the

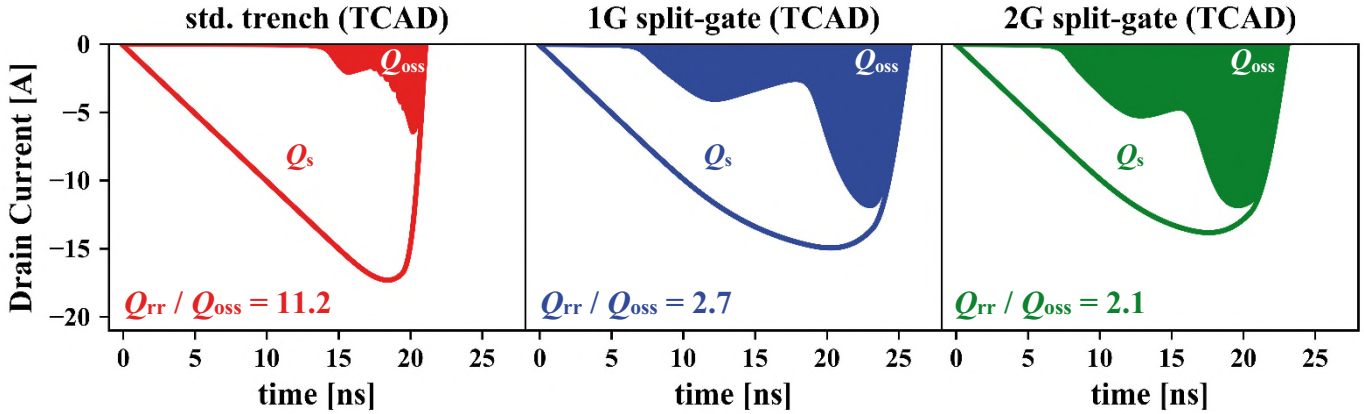

Fig. 7. TCAD simulated reverse recovery current for three generations of 100V MOSFETs. The output charge Q_{oss} of the device under test (Q2) is extracted by integrating the source, gate and field-plate displacement currents, represented by the solid colored areas [6]. The difference between Q_{rr} and Q_{oss} represents the charge Q_s stored in the drift region. TCAD simulations confirm the experimental trend that the ratio Q_{rr} / Q_{oss} reduces as the technology evolves (Fig. 8).

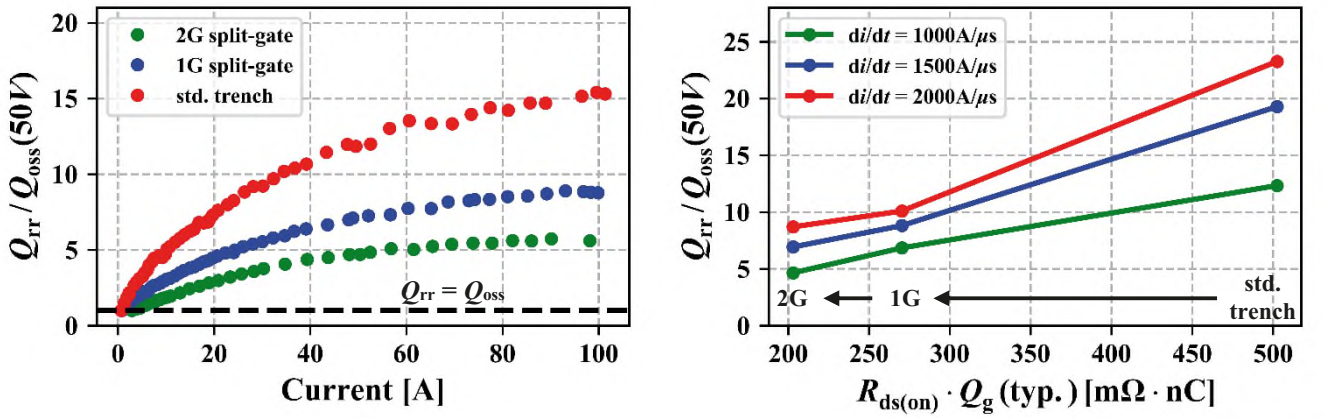

Fig. 8. Evolution of Q_{rr} / Q_{oss} ratio with trench technology for 100V MOSFETs. ***Left)*** $Q_{rr} / Q_{oss}(50V)$ vs. current for di/dt = 1000A/μs, extracted by taking the ratio of the plots in Figs. 5-6. At zero current, the reverse recovery is only due to the output charge, meaning that $Q_{rr} = Q_{oss}$. ***Right)*** $Q_{rr} / Q_{oss}(50V)$ vs. $R_{ds(on)} \cdot Q_g$ for three different di/dt values and I_D = 50A. As the technology evolves and the FOM $R_{ds(on)} \cdot Q_g$ is lowered, the ratio Q_{rr} / Q_{oss} is reduced, confirming the trend in Fig. 2.

current roll-off di/dt. While most datasheets report Q_{rr} values with di/dt < 1000A/μs (typically 100A/μs), the experiments and simulations in this work are performed with di/dt ≥ 1000A/μs, which is more typical in MOSFET applications.

V. Lifetime Killing

The reverse recovery losses can be further reduced by lifetime reduction techniques [8]. As shown in Fig. 9, lifetime reduction on the 2G split-gate 100V technology allows an improvement of $R_{ds(on)} \cdot Q_{rr}$ by a factor ~2x. In addition, the slope of Q_{rr} vs. di/dt is reduced, meaning that the reverse recovery losses vary less with the switching speed. Lifetime killing slightly reduces the electron mobility in the drift region causing a ~3% increase in $R_{ds(on)}$ for the same active area. Nonetheless, the improved reverse recovery outweighs the $R_{ds(on)}$ penalty in critical applications. For instance, the efficiency of a full-bridge converter improves by ~0.07% at full load when lifetime killing is applied to a 2G split-gate 100V MOSFET (Fig. 10).

VI. Conclusion

The reverse recovery losses of trench MOSFETs reduce with the evolution of RESURF technology as a consequence of the higher drift doping concentrations, allowing lower specific on-resistance $R_{ds(on)} \cdot A$ and FOM $R_{ds(on)} \cdot Q_g$. The consequent increase in output capacitance is mitigated by better process control allowing a shallower trench depth over generations. In this way, the FOM $R_{ds(on)} \cdot Q_{oss}$ is also improved. Lifetime killing techniques allow a further reduction of the reverse recovery losses with efficiency improvement in target applications.

VII. References

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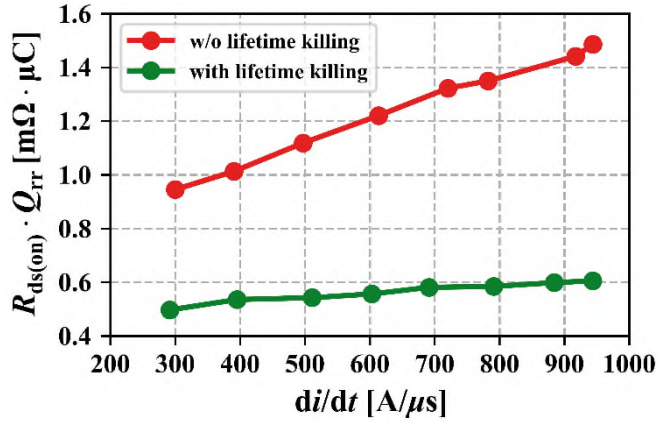

Fig. 9. Impact of lifetime killing on the reverse recovery of a 2G split-gate 100V MOSFET. Measurement shows $R_{ds(on)} \cdot Q_{rr}$ vs. di/dt for a current I_D = 50A and a supply voltage V_{dd} = 72V.

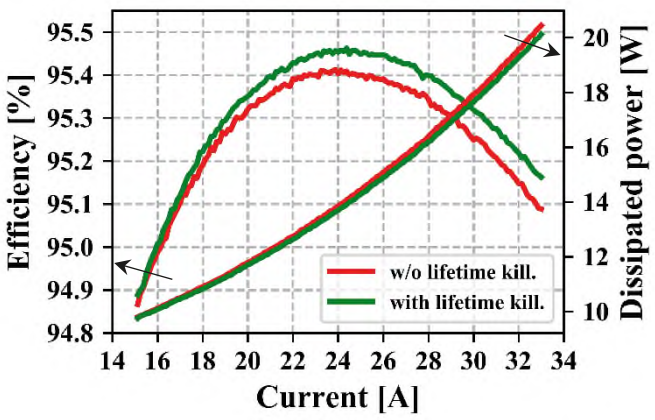

Fig. 10. Impact of lifetime killing on the efficiency of a full-bridge converter based on a 2G split-gate 100V MOSFET. The left y-axis shows the efficiency vs. current, and the right y-axis shows the corresponding power dissipation. Lifetime killing improves the efficiency a full-bridge converter by ~0.07%.