Extending the OptiMOS™3 Power MOSFET Family – performance for an energy-efficient world

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INTRODUCTION

Today, developments within the power conversion sector are driven by customer requirements for energy saving and physically smaller designs. Continual development of converter topologies for AC/DC and DC/DC has resulted in improved efficiency at converter-level. Power MOSFETs are the core component of power converters in this market sector and are fundamental in producing an efficient design. Improvements in the MOSFET designs allow the circuit designers to utilize the improved device level performance. Increases in switching frequency and other critical parameters allow the converter design to operate more efficiently. In some cases this may allow circuit design modifications that would not be possible without these improved MOSFET designs.

In 2006, the OptiMOS™2 100 V MOSFET was introduced by Infineon Technologies in response to these requirements [1]. It was the first power MOSFET device, within this voltage range that was based on charge compensation techniques. This resulted in a significant reduction of the MOSFET on-resistance over traditional designs whilst retaining excellent switching behavior.

The release of the OptiMOS™3 series improves the design further and allows higher voltage devices to benefit from these technologies. OptiMOS™3 devices not only have best in class performance in the 150 V to 250 V sector but combines this with several key parameters. The new devices exhibit low gate-charge characteristics, high switching speeds and good avalanche ruggedness. These attributes make them suitable for a wide variety of switch-mode power supply (SMPS) applications. These include high-efficiency AC/DC SMPS and DC/DC converters for telecommunication and server based applications, Class-D amplifiers and motor-control driver applications.

DEVICE CONCEPT

The compensation principle for power MOSFETs was introduced in 1998 in commercially available products with the 600 V CoolMOS™ Technology [2]. The basic principle behind the drastic $R_{DS(on)} \times A$ reduction compared to conventional power MOSFETs is the compensation of n-drift region donors by acceptors located in p-columns as depicted in Fig. 1.

For lower breakdown voltages, trench field-plate MOSFETs are an excellent alternative. The application of a field-plate clearly improves the device's performance. The device comprises of a deep trench penetrating through most of the n-drift region. An insulated deep source electrode, separated from the n-drift region by a thick oxide layer, acts as a field-plate and provides mobile charges required to balance the drift region donors under blocking conditions as it is schematically shown in Fig. 1. Standard MOS structures exhibit a linearly decreasing vertical electric field having the maximum field-strength at the body/drift region pn-junction. Such devices do not show a lateral component of the electric field. In a field-plate device,

there is also a lateral component of the electric field and the space-charge region expands mainly in lateral direction. Consequently, an almost constant vertical field distribution is gained and the necessary drift-region length for a given breakdown voltage is significantly reduced. Simultaneously, the drift-region doping can be increased. Both techniques also result in a major reduction in on-state resistance.

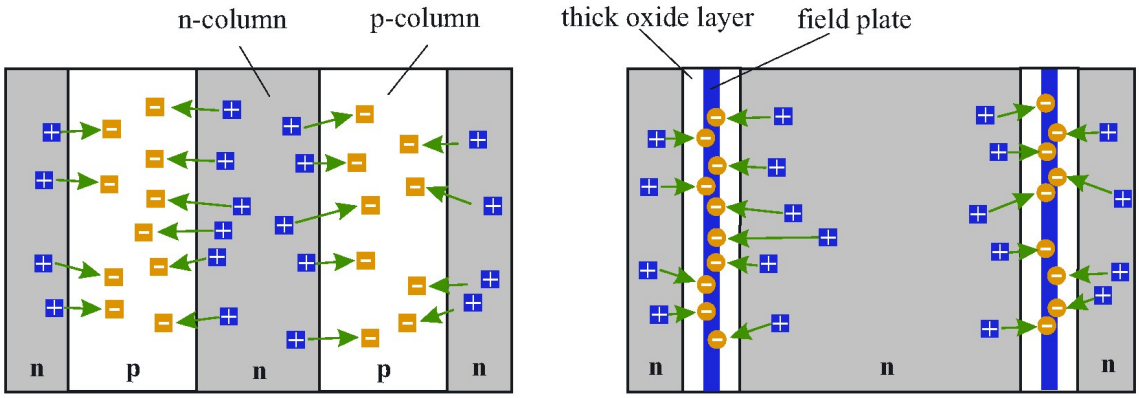

Fig. 1: Compensation of drift region by p-doped columns (left) and by a field-plate (right)

EXTENDING THE DEVICE FAMILY TOWARDS HIGHER BLOCKING CAPABILITY

The development of a new, space-saving and efficient edge-termination structure allows the OptiMOS™3 family to extend the benefits of this technology to devices up to 250 V [3].

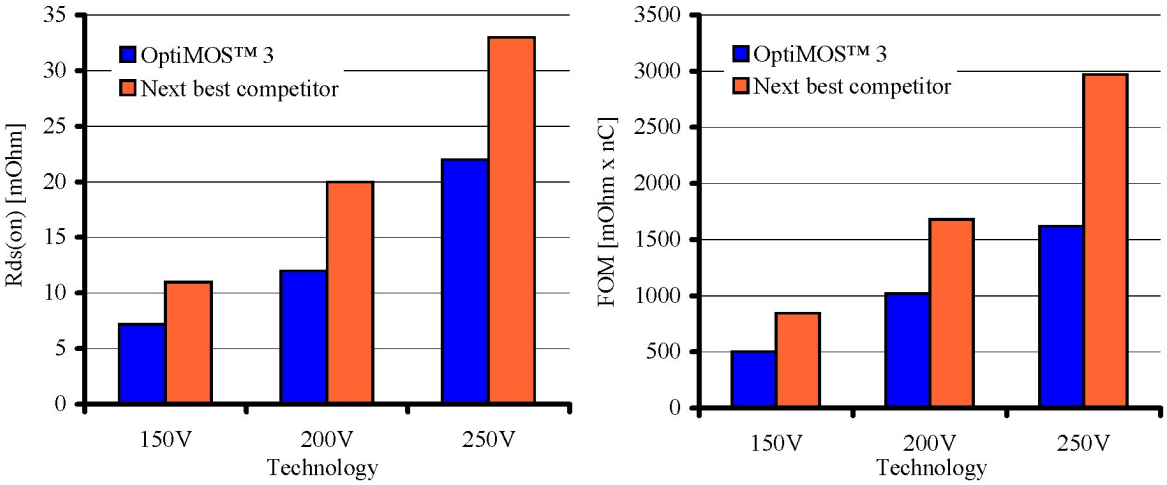

Fig. 2: OptiMOS™3 150 V, 200 V and 250 V Benchmark in $R_{DS(on)}$ and FOM

The combination of the termination structure and charge compensation technologies results in exceptionally low $R_{DS(on)}$ and results in an excellent figure-of-merit FOM = $R_{DS(on)}$ x Q_G. A comparison to the next best competitor device currently available is given in Fig. 2, clearly indicating the benefits of these technologies in terms of improved device performance. The culmination of these technological advances is a device that offers superior solutions for a wide range of system requirements. In high-current applications like motor-control, lowest-ohmic devices in D²-Pak and TO-220 minimize conduction losses and reduce the number of

paralleled devices in the system. In fast switching applications, the very low gate-drain-charge Q_{GD} and $FOM_{GD} = R_{DS(on)} \times Q_{GD}$ cuts down on the switching losses and improves the overall efficiency. Devices available in SuperSO8 packages are therefore the perfect choice for applications like DC/DC converters or Class-D amplifiers. Furthermore, the very low on-resistance $R_{DS(on)}$ often allows for a package shrink. TO-247 packages can be replaced by TO-220, a D²-Pak or TO-220 can often be replaced by a SuperSO8. The net result is a very compact, space saving solution, which delivers significantly better switching performance.

Another important issue is paralleling, especially in case of high-current applications such as motor-control. To meet the application requirements it is often advantageous to make use of complete power modules. This allows for improved heat management and lower parasitics, both boosting the overall performance. Here, the device count can be noteworthy reduced using the new device generation. Fig. 3 gives an example of the switching waveforms of large OptiMOS™3 150 V chips paralleled in a power module. Here, a three-phase, full-bridge configuration was realized having eight chips in parallel on one DCB substrate with again two DCB's in parallel. Fig. 3 shows the switching behavior of one phase leg at a supply voltage of 80 V and a switched current of 500 A. The waveforms indicate a smooth switching behavior with an acceptable overshoot voltage during the turn-off phase, no problems were observed.

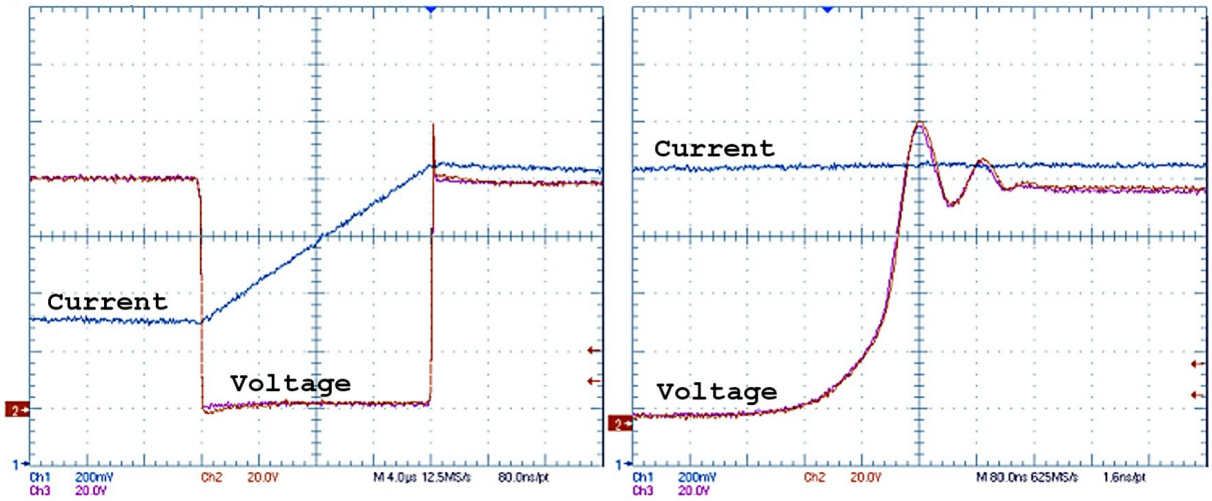

Fig. 3: Switching waveforms of paralleled OptiMOS™3 150 V chips in a power module at a duty-cycle of 13%.
Left: full pulse showing turn-on and turn-off (200A/div, 20V/div, 4µs).
Right: detailed turn-off slope (200A/div, 20V/div, 80ns) [4].

CHOOSING THE RIGHT POWER PACKAGE

With silicon technology moving rapidly forward the package becomes an important part for low-voltage MOSFETs. Especially the package inductance can play a major part in loss generation and for the overall device and application performance. Moreover, the on-resistance of the latest device technologies has become remarkable low, thus driving the need for low ohmic packages to avoid a limitation of the device by the package characteristics.
30 V technologies from most vendors today allow for MOSFET dies in a TO-220 with a lower on-resistance than the package resistance. Latest 60 V technologies on the market allow for devices with a package contribution of below 30% and even for 100 V technologies the package can already account for more than 20%, given a package resistance of 1 mOhm. Therefore, the package resistance clearly limits the minimum on-resistance achievable.

Additionally, a larger die is required for a given on-resistance which also increases the gate charge and thus slowing down the device switching.
Package contributions for devices with maximum die-size for the most common low-voltage MOSFET classes are shown in Fig. 4. To follow the route towards denser and more efficient power converter designs, new package types, such as the SuperSO8, S3O8 or the DirectFET/ CanPAK, are needed to replace the leaded SMD or through-hole devices for low-voltage MOSFETs.

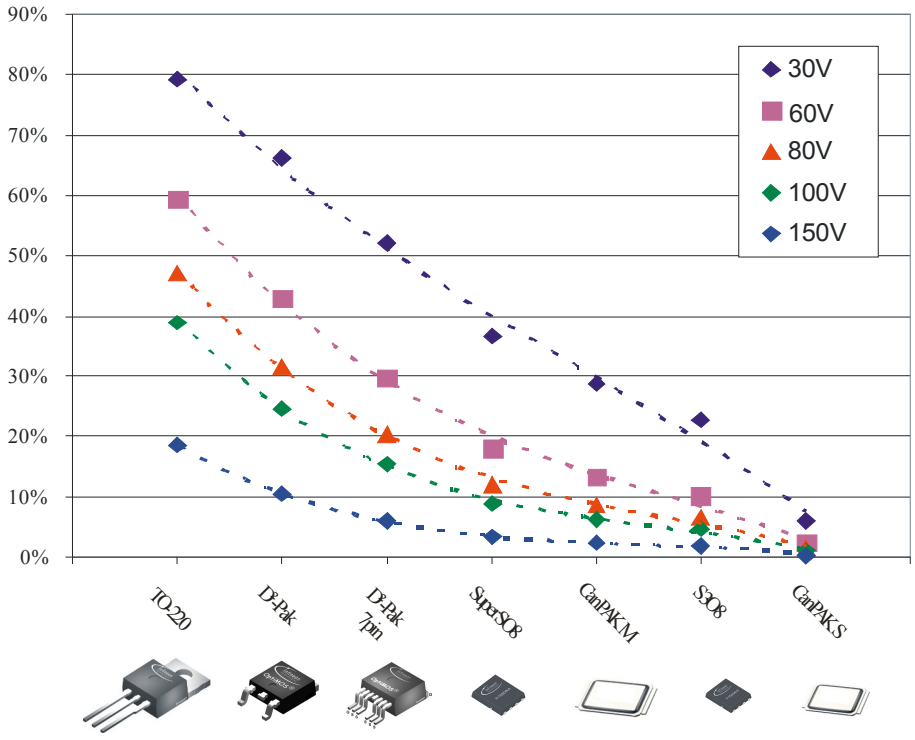

Fig. 4: Package contribution to overall device resistance for devices with maximum die-size for several state-of-the-art technologies

It is easily possible to estimate the losses due to package inductance for the turn-off. As example, a buck-converter with an output current of 30 A, operating at 250 kHz, generates 0.7 W of losses in a D-Pak design due to the total package inductance of 6 nH. With a low inductive package like the SuperSO8, showing an inductance of just 0.5 nH, the losses drop below 0.1 W. The lower package inductance also helps to avoid an unwanted turn-on of the MOSFET due to the source pin inductance in case of fast transients.

Another package-related topic is heat-spreading which can be improved by either using an improved standard package or by completely shifting to newer package types. As shown in Fig. 5, the use of a D²Pak with 7 pins instead of a standard D²Pak already results in the avoidance of hot spots and a lower overall temperature. More advantages are gained if SuperSO8 packages are used. Fig. 6 gives the comparison between D²Pak-7pin devices and the same amount of active silicon area packaged in SuperSO8 devices. Not only is the temperature behavior improved and a smaller PCB area is occupied, but the SuperSO8 packages also offer the chance to apply topside cooling for further improvements.

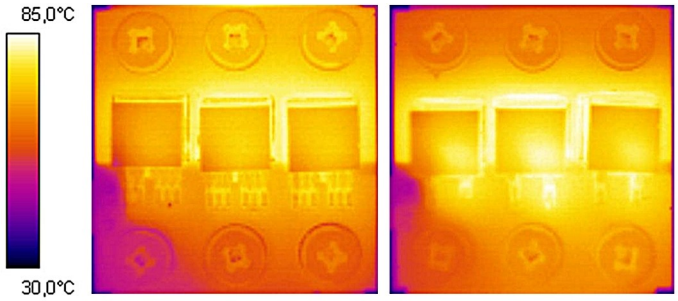

Fig. 5: Thermal comparison between a D²-Pak-7pin (left) and a standard D²Pak (right)

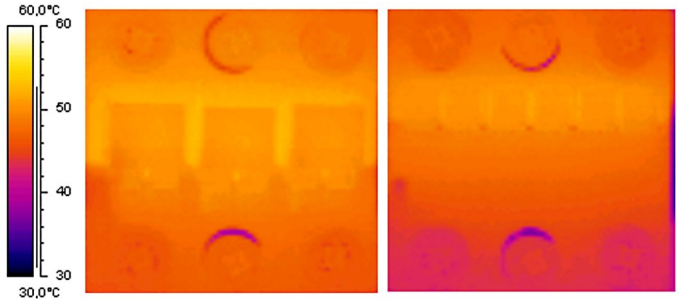

Fig. 6: Thermal comparison between a D²-Pak-7pin (left) and SuperSO8 devices (right) containing equivalent silicon area (right)

SUMMARY

With the actual release of its OptiMOS™3 technology in the voltage classes 200 V and 250 V Infineon Technologies now covers the full voltage range from 25 V to 250 V. With OptiMOS™3 being best-in-class for every single voltage class with respect to static and dynamic losses enables customers to deliver future power converters with unprecedented efficiencies and power densities for a wide range of topologies.

www.infineon.com/mosfets

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